NS5S1153MUGEVB

DPDT USB 2.0 High Speed / Audio Switch with Negative Swing Capability Evaluation Board User's Manual

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Overview

The NS5S1153 is a DPDT switch for combined true−ground audio and USB 2.0 high speed data applications. It allows portable systems to use a single port to pass either USB data or audio signals from an external headset; headset; the two channels being compliant to USB 2.0, USB 1.1 and USB 1.0.

The switch is capable of passing signals with negative voltages as low as 2 V below ground. The device features shunt resistors on the audio ports. These resistors are switched in when the audio channel is off and provide a safe path to ground for any charge that may build up on the audio lines. This reduces Pop & Click noise in the audio system. The NS5S1153 is also equipped with V_{BUS} detection circuitry to immediately switch to USB mode in the event that a voltage is detected on V_{BUS}.

The NS5S1153 is housed in a space saving, ultra low profile 1.4 x 1.8 x 0.5 mm 10 pin μQFN package.

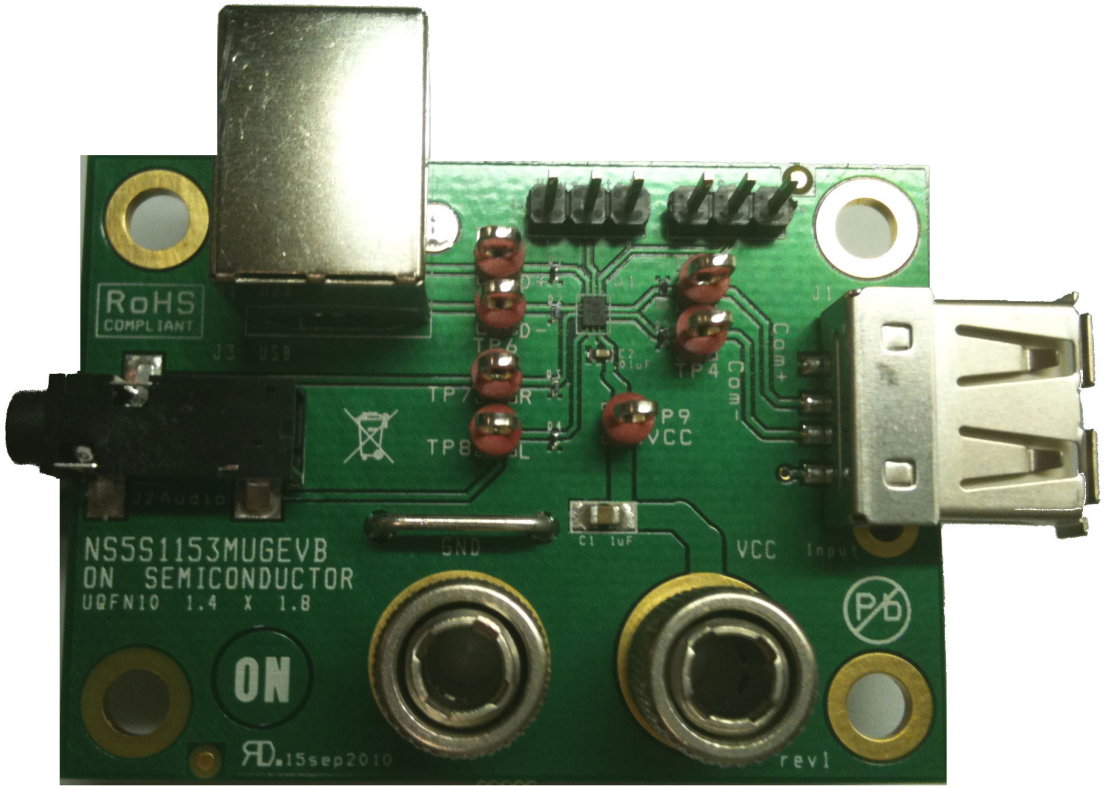

Figure 1. Board Picture

NS5S1153 – BOARD SCHEMATIC

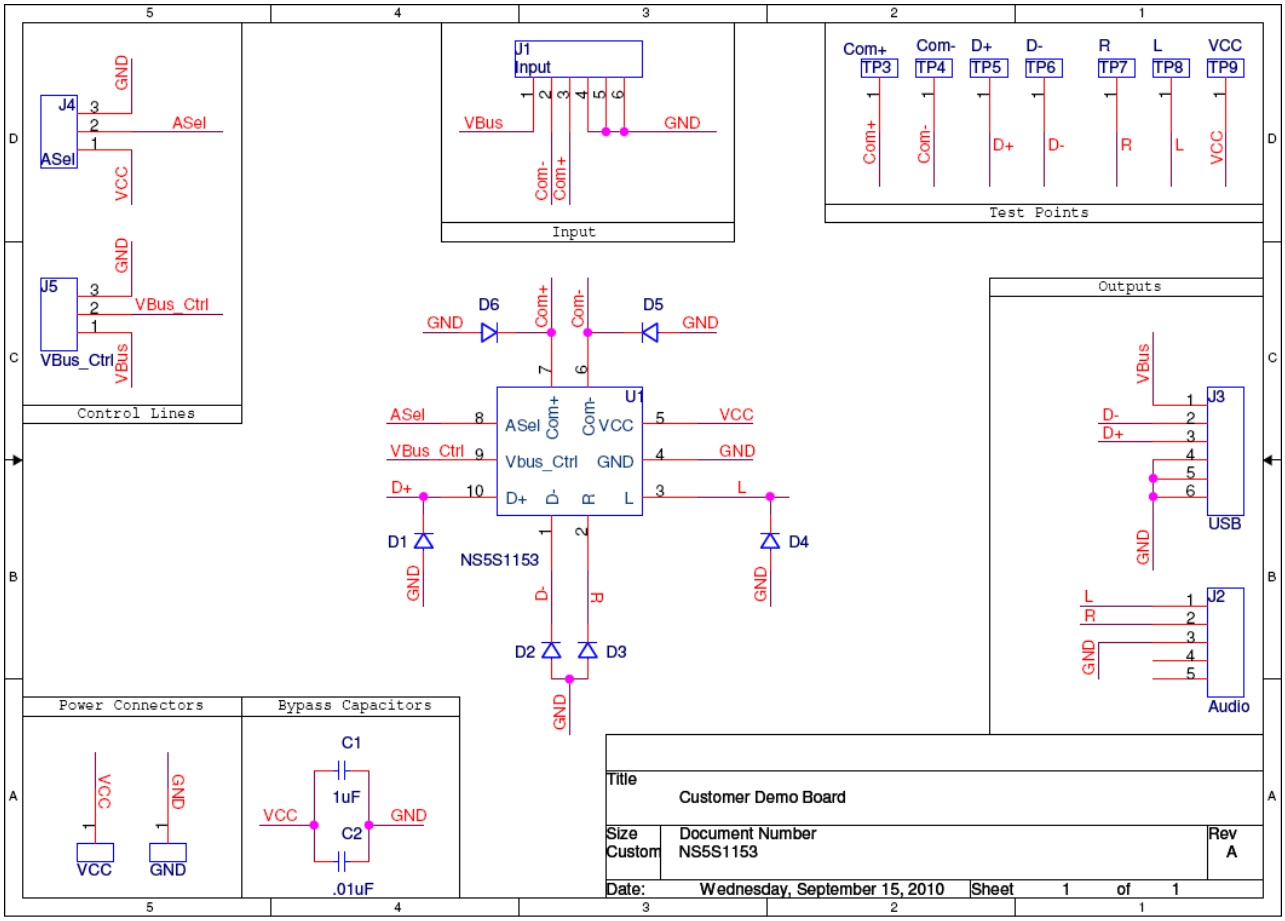

Figure 2. Board Schematic

Table 1. NS5S1153 – BOARD CONNECTIONS

Symbol	Description
SUPPLY	
V_{CC}, GND	This is the positive and the return connection for power supply.
SETUP	
J4 – ASEL	This is the line selection header.
J5 – VBUS_CTRL	This is VBUS comparator input.
SIGNALS	
J1 – INPUT	This USB connector Male A type is the common data and audio lines.
J2 – AUDIO	This connector is a 3.5 mm Stereo Jack Connector.
J3 – USB	This USB connector Male B type is the high speed USB signaling path.

NS5S1153 – TEST PROCEDURE

Equipment needed

- Power Supply
- Digital Ohm Meter
- Desktop or Laptop with Windows XP or higher
- USB Memory Stick
- USB Type A to USB Type B

Table 2. BACKGROUND: ASEL AND VBUS TRUTH TABLE

A_{SEL}	V_{BUS}	L, R	D+, D−	L, R Shunt
Low	Low	ON	OFF	OFF
Low	High	OFF	ON	ON
High	X	ON	OFF	OFF

Test

1. Connect ASEL to ‘0’ (J4) and VBUS_CTRL to ‘1’ (J5).
2. Connect the power supply at 3.6 V from VCC to GND. The supply current should be around 20 μA.
   The impedance measured from COM+ (TP3) to D+ (TP5) is over 10 MΩ.
   The impedance measured from COM− (TP4) to D− (TP6) is over 10 MΩ.
   The impedance measured from COM+ (TP3) to R (TP7) is close to 3 Ω.
   The impedance measured from COM− (TP4) to L (TP8) is close to 3 Ω.
3. Insert a USB cable from USB terminal (J3) to the laptop or desktop.
   The impedance measured from L (TP8) and R (TP7) to GND is closed to 118 Ω.
4. Place a USB Memory Stick connected to USB terminal (J1). The device is being recognized.

NS5S1153 – COMPONENTS SELECTION

Input Capacitor

A 0.1 μF X5R ceramic capacitor or larger must bypass V_{CC} input to the ground. This capacitor should be placed as close as possible to this input.

ESD Diode

In order to protect the device against transient voltages, an external bi−directional ESD / IEC diode is recommended on COM+ and COM− pin. The ESD11N is designed to protect voltage sensitive components that require ultra−low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

Table 3. NS5S1153 – BILL OF MATERIAL

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
U1	1	NS5S1153	n/a	n/a	UQFN10	ON Semiconductor	NS5S1153
C1	1	Ceramic Capacitor SMD	1 μF	10%	0805	Murata	GRM155R60J105
C2	1	Ceramic Capacitor SMD	0.01 μF	10%	0402		
D1, D2, D3, D4, D5, D6	6	5V Bi−Directional TVS	n/a	n/a	DSN2	ON Semiconductor	ESD11N5
TP3, TP4,TP5, TP6, TP7, TP8, TP9	7	Test Point PC Multi Purpose	n/a	n/a	TP1	Keystone Electronics	5010
VCC, GND	2	Banana Connector	n/a	n/a	7 mm Hole	Johnson Components	111−2223−001
Vbus_Ctrl, Asel	2	50pin Modular 2pin header	n/a	n/a	Header3	Tyco Electronics	5−826629−0
Input J1	1	USB TypeA Connector	n/a	n/a	USB TypeA	Mill−Max	896−43−004−00−000000
USB J3	1	USB TypeB Connector	n/a	n/a	USB TypeB	Adam Tech	USB−B−S−RA
Audio J2	1	Stereo Audio Jack Connector	n/a	n/a	PHONO_SJ3523	CUI Inc	SJ−3523−SMT
GND Bar	1	PCB Shorting Link	n/a	n/a	GND_Strap	Harwin	D3082−46
PCB	1	55 x 40 mm 2 Layers	NA	NA	NA	Any	NS5S1153MUGEVB

NS5S1153 – PCB LAYOUT GUIDELINES

Electrical Layout Considerations

Implementing a high speed USD device requires paying attention on USB lines and traces to preserve signal integrity. The demonstration board serves as layout example and can support the design engineers to preserve high speed performances.

Electrical layout guidelines are:

- Bypass capacitor must as closed as possible to the Vcc input pin for noise immunity
- The characteristics impedance of each High Speed USB segment must be 45 Ω.
- All corresponding D+ / D− line segment pairs must be the same length.
- The use of vias to route these signals should be avoided.
- The use of turns or bends to route these signal should be avoided.
- The ground plane of the PCB will be used to determine the characteristics impedance of each line.

NS5S1153 – EVALUATION BOARD PCB LAYOUT

Board Reference: NS5S1153MUGEVB

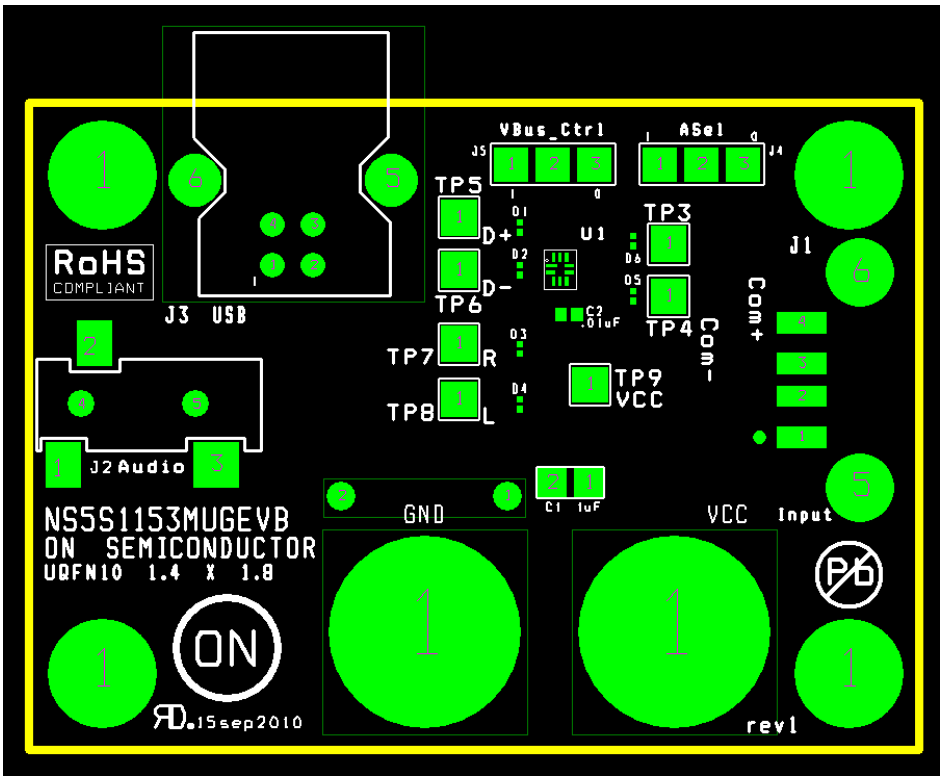

Figure 3. Assembly Layer

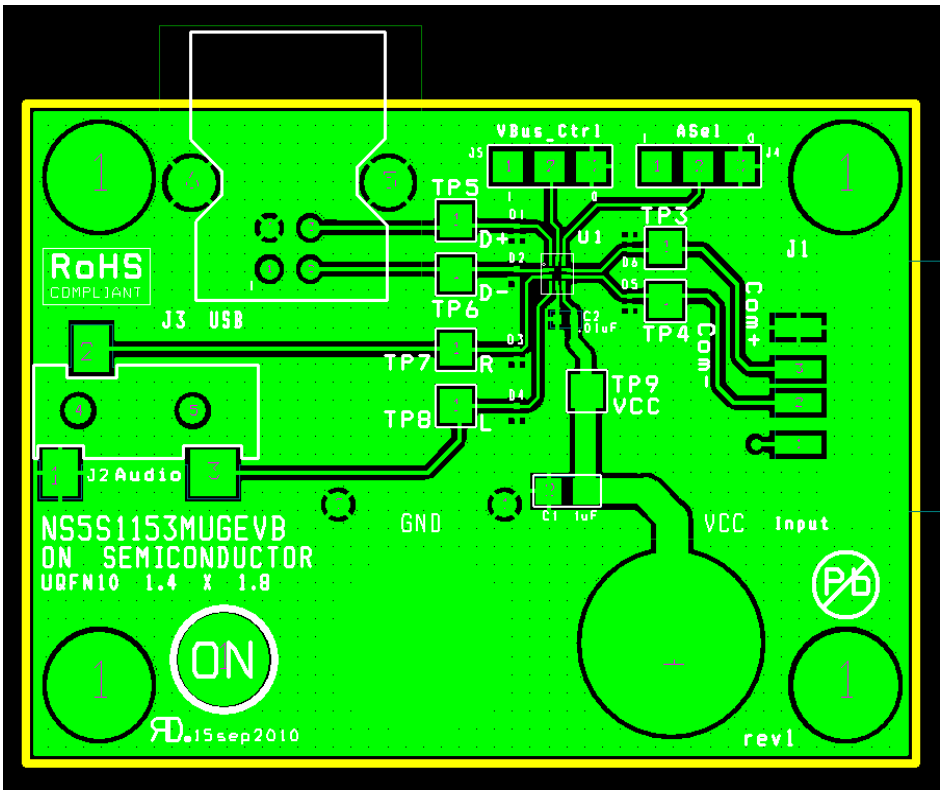

Figure 4. Top Layer Routing

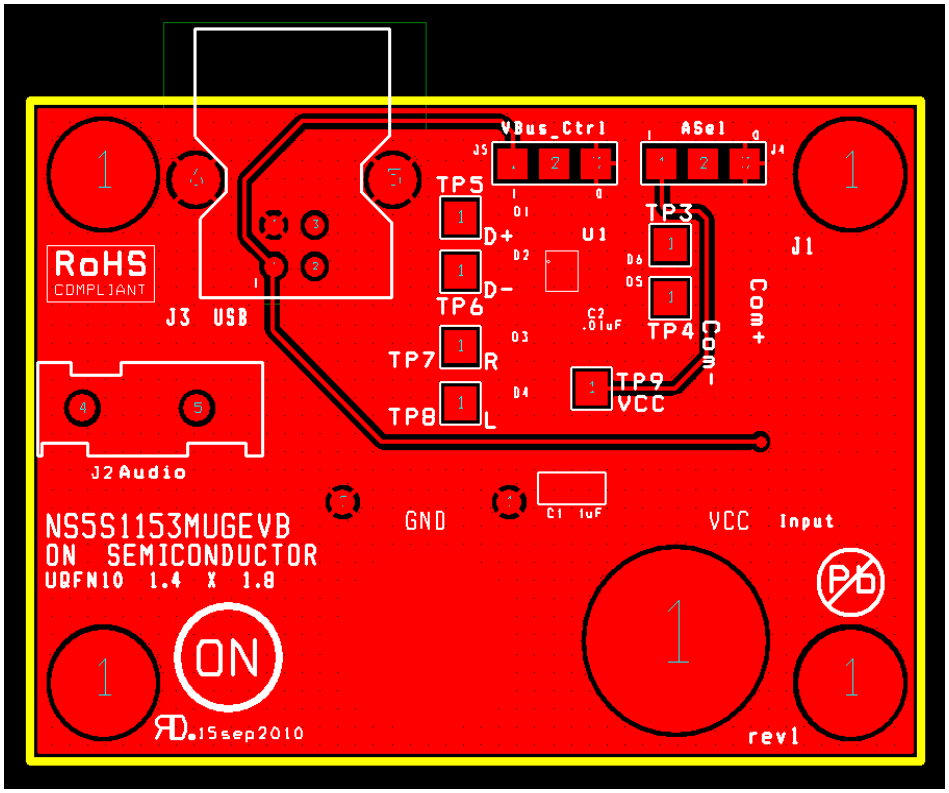

Figure 5. Bottom Layer Routing

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