NB4N855SMEVB

Evaluation Board User's Manual for NB4N855S

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Description

ON Semiconductor has developed an evaluation board for the NB4N855S device as a convenience for the customers interested in performing their own device engineering assessment. This board provides a high bandwidth 50 Ω controlled impedance environment. The pictures in Figure 1 show the top and bottom view of the evaluation board, which can be configured in several different ways.

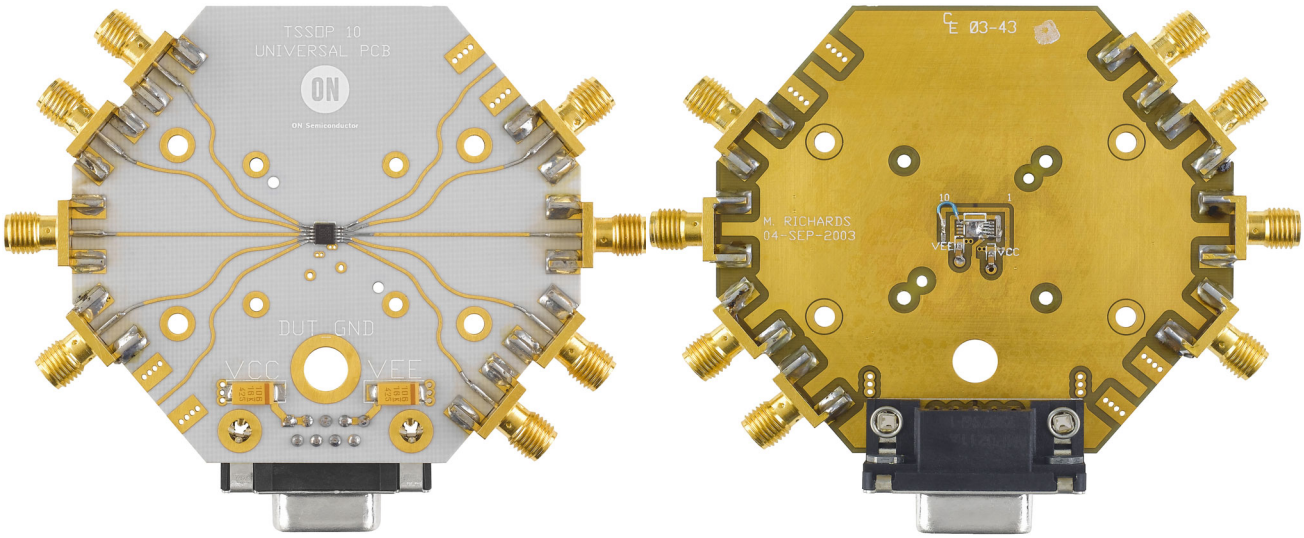
This NB4N855S evaluation board manual contains:

- Appropriate Lab Setup
- Assembly Instructions
- Bill of Materials

This manual should be used in conjunction with the NB4N855S device data sheet, which contains full technical details on the device specifications and operation.

Board Lay−Up

The NB4N855S evaluation board is implemented in four layers with split (dual) power supplies (Figure 6, Evaluation Board Lay−up). For standard lab setup, a split (dual) power supply is essential to enable the 50 Ω internal impedance in the oscilloscope as a devices termination. The first layer or primary trace layer is 0.005″ thick Rogers RO4003 material, which is designed to have equal electrical length on all signal traces from the device under the test (DUT) to the sense output. The second layer is the 1.0 oz copper ground plane. The FR4 dielectric material is placed between second and third layer and between third and fourth layer. The third layer is also 1.0 oz copper ground plane. The fourth layer is the secondary trace layer.



Top View

Bottom View

Figure 1. Top and Bottom View of the NB4N855S Evaluation Board

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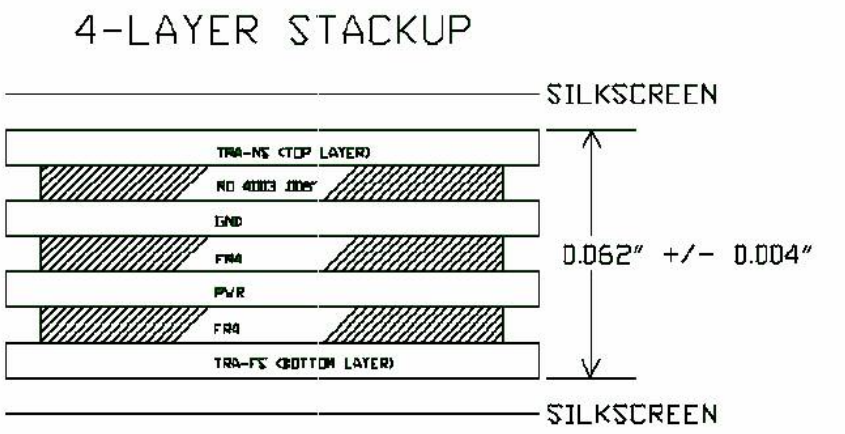


Figure 2. Evaluation Board Lay−up

Connecting Power and Ground Planes

The side launch 9 pin power supply connector is wired as shown in Figure 3. Test points can be soldered on the top of the PCB to accommodated easier connections. Exact values that need to be applied can be found in Table 1.

Table 1. Power Supply Levels

Power Supply Span	V_{CC} (Pin 10)	V_{EE} / GND (Pin 5)	DUT_GND (PCB SMA Ground))
3.0 V	1.75 V	−1.25 V	0 V
3.3 V	2.05 V	−1.25 V	0 V
3.6 V	2.35 V	−1.25 V	0 V

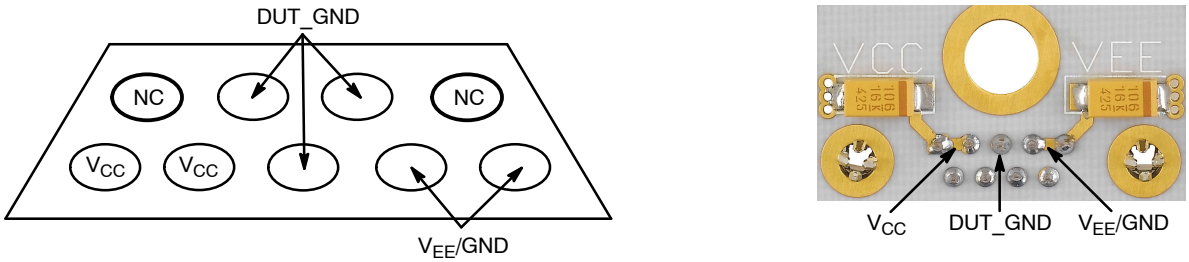


Figure 3. Power Supply Connector − 9 Pin Side View (Left) and PCB Top View (Right)

Stimulus (Generator) Termination

All ECL outputs need to be terminated to V_{TT} ($V_{TT} = V_{CC}$ –2.0 V = GND) via a 50 Ω resistor. The current board design utilizes the space for placement of the external termination resistors. (More information on termination is provided in AN8020). The 0402 chip resistor pads are provided on the bottom side of the evaluation board. Solder the chip resistors to the bottom side of the board between the appropriate input of the device pin pads and the ground pads as shown in Figure 4 (for split power supply setup, PCB is assembled in this configuration).

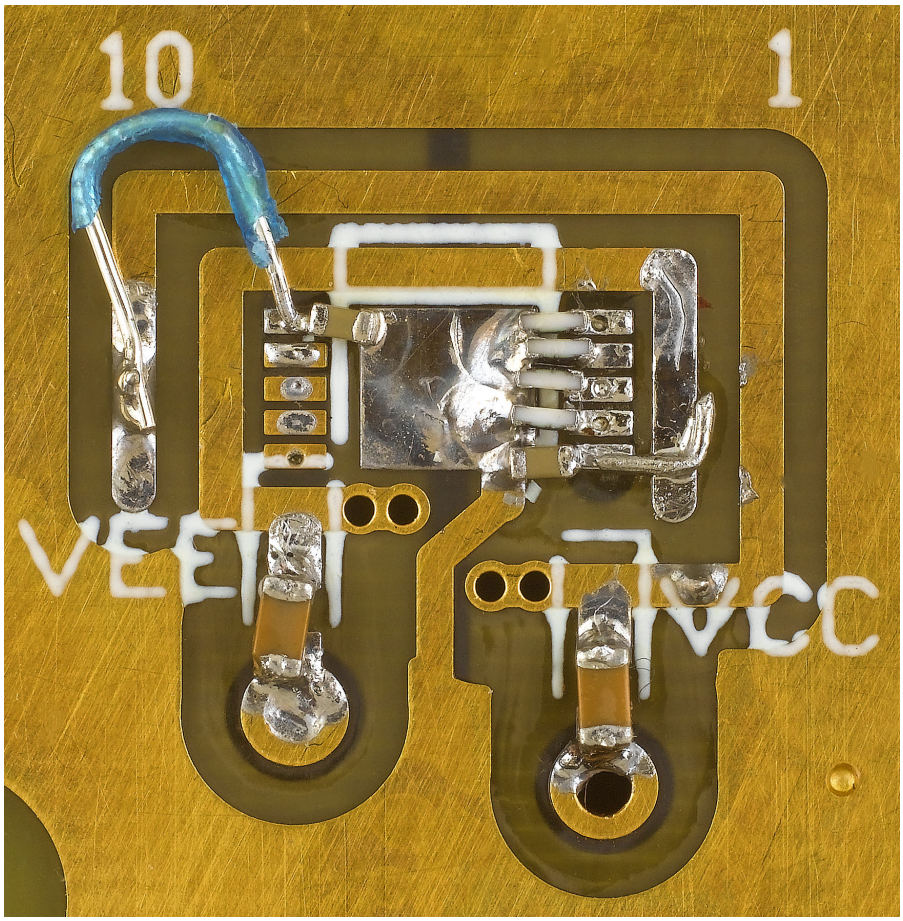


Figure 4. Expanded Bottom View

Likewise for CML outputs, CML stimulus signal need to be terminated to V_{CC} via a 50 Ω resistor. To accomplish this configuration the external termination resistor has to be moved from DUT_GND ring to V_{CC} ring on the bottom of the board.

For the LVDS configuration Input pin pads of the D0 or D1 input has to be shorted using 100 Ω resistor across differential lines.

DUT Termination

For standard lab setup and test, a split (dual) power supply is required enabling the 50 Ω internal impedance in the oscilloscope to be used as a termination of the signals (in split power supply setup DUT_GND is the system ground, V_{CC} is varied, and V_{EE} is –1.25 V; see Table 1, Power Supply Levels).

Board Components Configuration

The NB4N855SMEVB evaluation board requires eight side SMA connectors. Placement locations are described in the Table 2 below.

Table 2. SMA Connectors and Jumpers Placement

Device	J1/D0	J2/D0b	J3/D1	J4/D1b	J5	J6/Q1b	J7/Q1	J8/Q0	J9/Q0b	J10
Pin #	1	2	3	4	5	6	7	8	9	10
Connector	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	No
Resistor (bottom)	0402 50 Ω	0402 50 Ω	0402 50 Ω	0402 50 Ω	0402 0.01 μF	No	No	No	No	0402 0.01 μF
Wire	No	No	No	No	to V_{EE}/GND	No	No	No	No	to V_{CC}

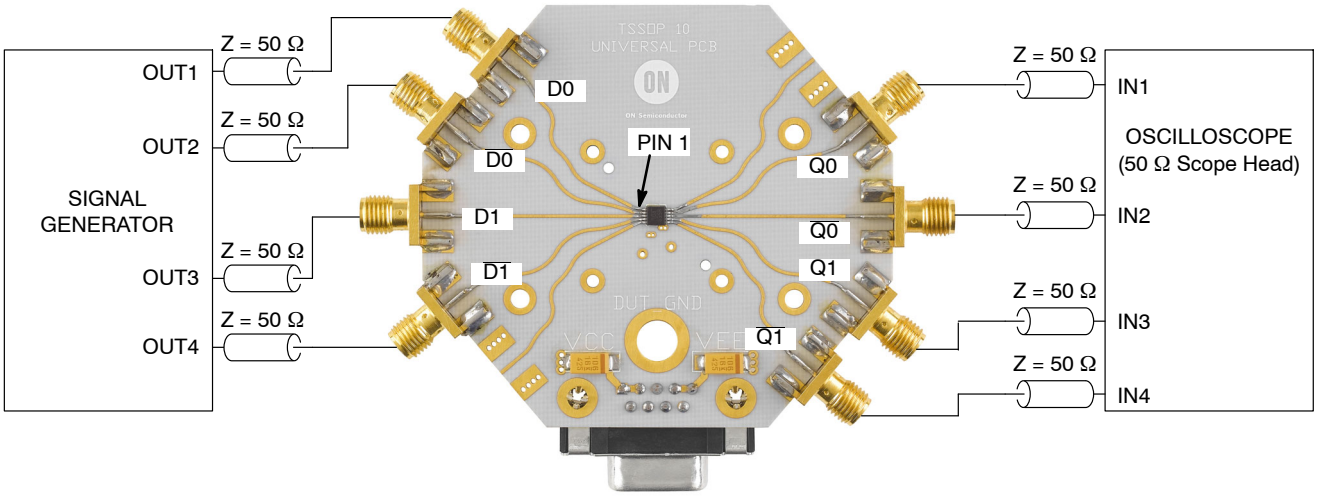


Figure 5. Lab Setup

1. Connect appropriate power supplies to V_{CC}, V_{EE}/GND and DUT_GND (See Table 1)
2. Connect a signal generator to the input SMA connectors via matched cables. Setup input signal according to the device data sheet.
3. Connect a test measurement device on the device output SMA connectors via matched cables.

NOTE: The test measurement device must contain 50 Ω termination.

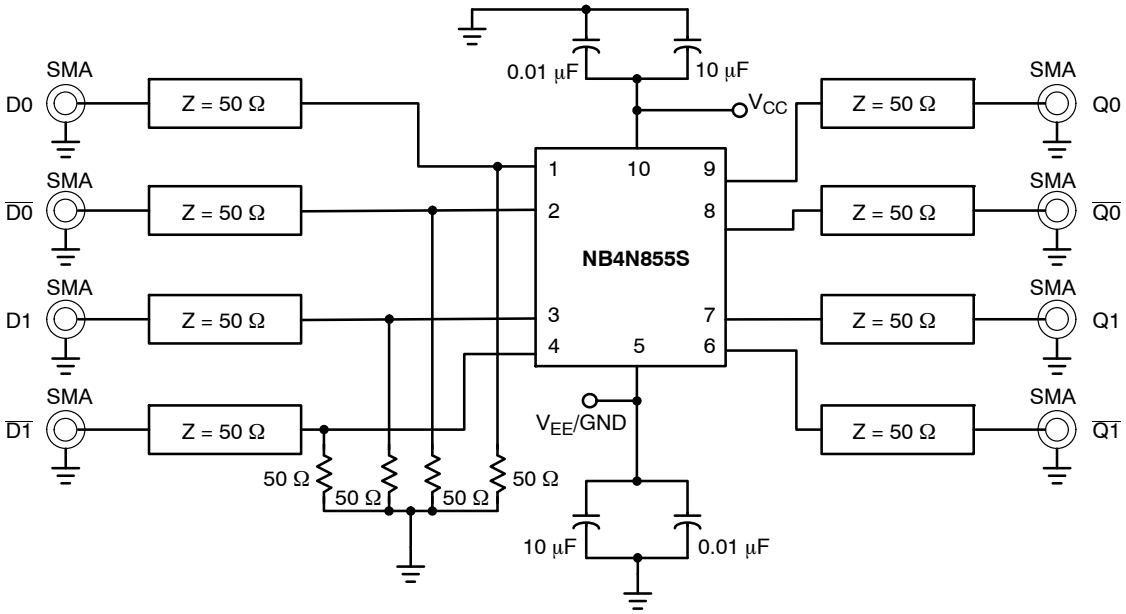


Figure 6. Evaluation Board Schematic

Table 3. Bill of Materials

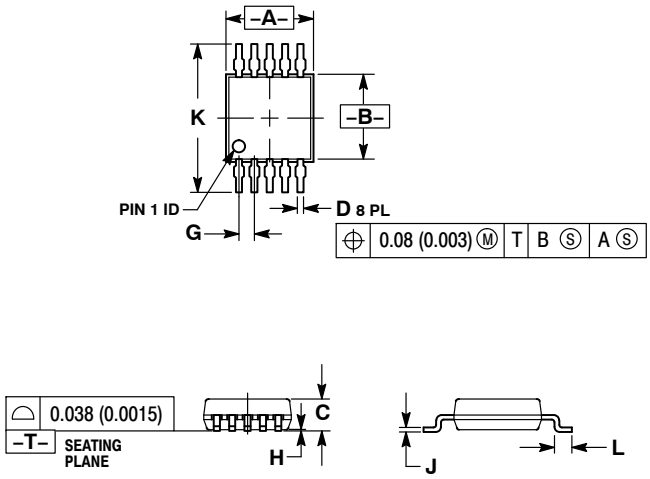
Components	Manufacturer	Description	Part Number	Qty.	Web Site
SMA Connector	Johnson*	SMA Connector − Side Launch	142−0701−851	8	http://www.johnsoncomponents.com
9 Pin D−Sub Receptacle	Amphenol	Connector, Female, 9−Pin, Right Angle	788796−1	1	http://www.amphenol.com
Surface Mount Test Points†	Keystone*	SMT Miniature Test Point	5015	3	http://www.keyelco.com
		SMT Compact Test Point	5016		
Chip Capacitor	AVC Corporation*	0402 0.01 μF ± 10%	04025C103KAT2A	4	http://www.avxcorp.com
		10 μF ± 10%	T491C106K016AS	2	
Chip Resistor	Panasonic*	0402 50 Ω ± 1% Precision Thick Film Chip Resistor	ERJ−2RKF49R9X	4	http://www.panasonic.com
Evaluation Board	ON Semiconductor	Micro−10 Evaluation Board	N/A	1	http://www.onsemi.com
Device Samples	ON Semiconductor	Micro−10 Package Device	NB4N855SM	1	http://www.onsemi.com

*Components are available through most distributors, i.e. www.newark.com, www.Digikey.com

†Surface Mount Test Points can be used for power supply connection in place of power supply cable connector. See Figure 3 for test point placement.

PACKAGE DIMENSIONS

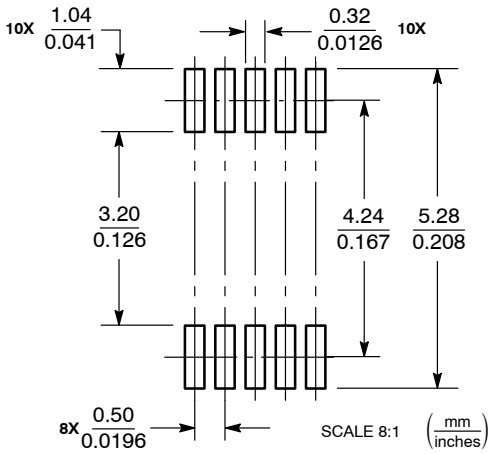
Micro−10
CASE 846B−03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION “A” DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION “B” DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846B−01 OBSOLETE. NEW STANDARD 846B−02

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.95	1.10	0.037	0.043
D	0.20	0.30	0.008	0.012
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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