NB4N527SMNEVB

Evaluation Board User's Manual for NB4N527S

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EVAL BOARD USER'S MANUAL

INTRODUCTION

ON Semiconductor has developed an evaluation board for the NB4N527S device as a convenience for the customers interested in performing their own device engineering assessment. This board provides a high bandwidth 50 Ω controlled impedance environment. The pictures in Figure 1 show the top and bottom view of the evaluation board, which can be configured in several different ways.

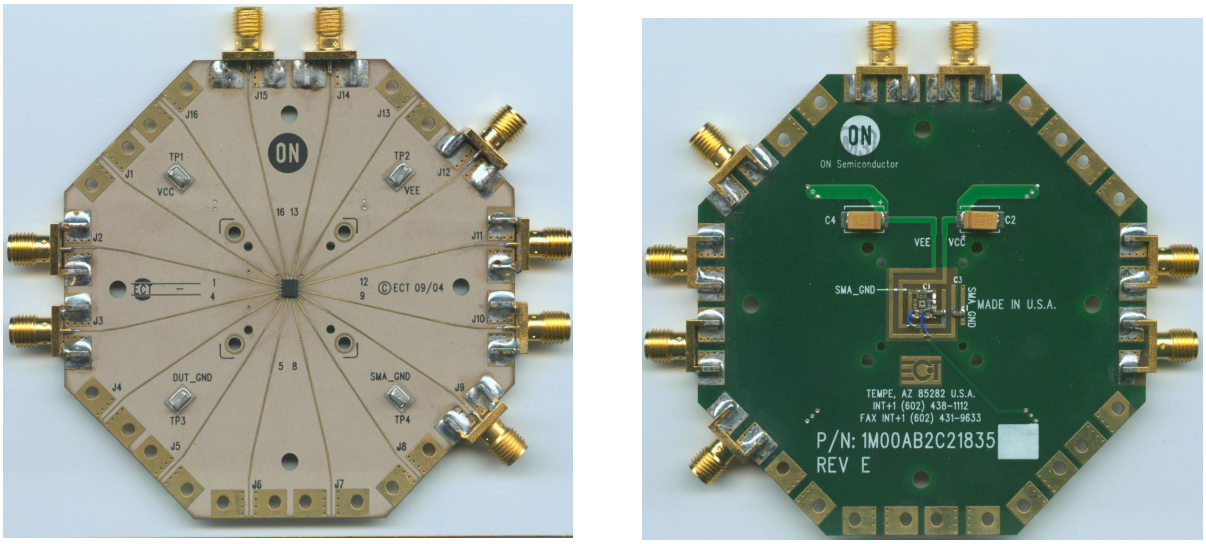
This evaluation board manual contains:

- Information on 16−lead QFN Evaluation Board
- Assembly Instructions
- Appropriate Lab Setup
- Bill of Materials

This manual should be used in conjunction with the NB4N527S device data sheet, which contains full technical details on the device specifications and operation.

Board Lay−Up

The 16−lead QFN evaluation board is implemented in four layers with split (dual) power supplies (Figure 2, Evaluation Board Lay−up). For standard lab setup, a split (dual) power supply is essential to enable the 50 Ω internal impedance in the oscilloscope as a device termination. The first layer or primary trace layer is 0.005, thick Rogers RO6002 material, which is designed to have equal electrical length on all signal traces from the device under the test (DUT) to the sense output. The second layer is the 1.0 oz. copper ground plane. The FR4 dielectric material is placed between the second and third layer, and between the third and fourth layer. The third layer is also a 1.0 oz copper ground plane. The fourth layer is the secondary trace layer.



Top View

Bottom View

Figure 1. Top and Bottom View of the 16 QFN Evaluation Board

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Top / DUT Side	**Rogers 6002 1/2 OZ Copper**	T_W= 0.022
	Dielectric= 0.010	
GND	**Rogers 6002 1 OZ Copper**	
	Min. Adjust 0.025	
SIGNAL DUT GND	**FR4 1 OZ Copper**	
	Dielectric= 0.010	
Bottom / Tester Side	**FR4 1/2 OZ Copper**	

Figure 2. Evaluation Board Lay−up

Connecting Power and Ground Planes

Top side of the evaluation board has the four surfaces mount test point clips labeled V_{CC}, V_{EE}, SMA_GND, and DUT_GND. DUT_GND is connected to the exposed flag of the QFN package. For proper operation, the exposed flag is recommended to be **ELECTRICALLY** left floating or tied to V_{EE}, but must be **THERMALLY** connected to a sufficient heat conduit such as a thermal plane Exact supply voltage values that need to be applied can be found in Table 1 and Figures 4 and 5.

Table 1. Power Supply Levels

Power Supply Span	V_{CC}	V_{EE}	SMA_GND	DUT_GND
3.0 V	1.75 V	−1.25 V	0 V	Float or V_{EE}
3.3 V	2.05 V	−1.25 V	0 V	Float or V_{EE}
3.6 V	2.35 V	−1.25 V	0 V	Float or V_{EE}

Stimulus (Generator) Termination

All ECL outputs need to be terminated to V_{TT} ($V_{TT} = V_{CC}$ –2.0 V = GND) via a 50 Ω resistor. The current board design utilizes the internal resistors and the V_{TDx} pins are wired to ground. (More information on termination is provided in AN8020). If evaluation does not require use of internal termination resistors, 0402 chip resistor pads are provided on the bottom side of the evaluation board. The jumper wires of the V_{TDx} pin pads should be removed (J1, J4, J13 and J15 to SMA_GND jumper). Solder the chip resistors to the bottom side of the board between the appropriate input of the device pin pads and the ground pads (for split power supply setup).

Likewise for CML outputs, CML stimulus signal need to be terminated to V_{CC} via a 50 Ω resistor. If internal resistors are used, the V_{TDx} pin pads should be wired to V_{CC}. To accomplish this configuration, the jumper wire has to be moved from SMA_GND ring to V_{CC} ring on the bottom of the board.

For the LVDS configuration, V_{TDx} pin pads of the D0 or D1 input has to be shorted to form 100 Ω across differential lines. This configuration is accomplished by moving the jumper wire from SMA_GND ring to complementary V_{TDx} pin pad (example: VTD0 and VTD0b for D0 input and VTD1 and VTD1b for D1 input).

DUT Termination

For standard lab setup and test, a split (dual) power supply is required enabling the 50 Ω internal impedance in the oscilloscope to be used as a termination of the signals (in split power supply setup SMA_GND is the system ground, V_{CC} is varied, and V_{EE} is –1.25 V; see Table 1, Power Supply Levels).

Board Components Configuration

The NB4N527SMNEVB evaluation board requires eight side SMA connectors. Placement locations are described in Table 2 and Figure 3.

Table 2. SMA Connectors and Jumpers Placement

Device	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
Pin #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Connector	No	Yes	Yes	No	No	No	No	No	Yes	Yes	Yes	No	No	Yes	Yes	No
Wire	SMA_GND	No	No	SMA_GND	V_{EE}	No	No	V_{CC}	No	No	No	No	SMA_GND	No	No	SMA_GND

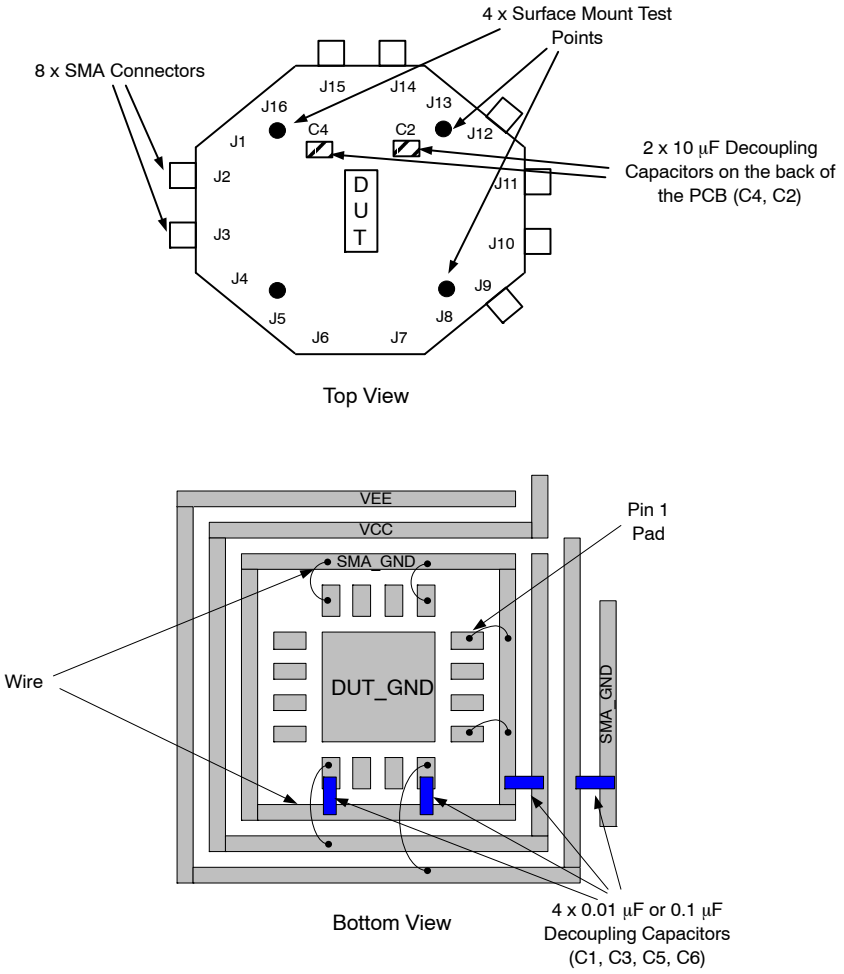


Figure 3. Components Placement

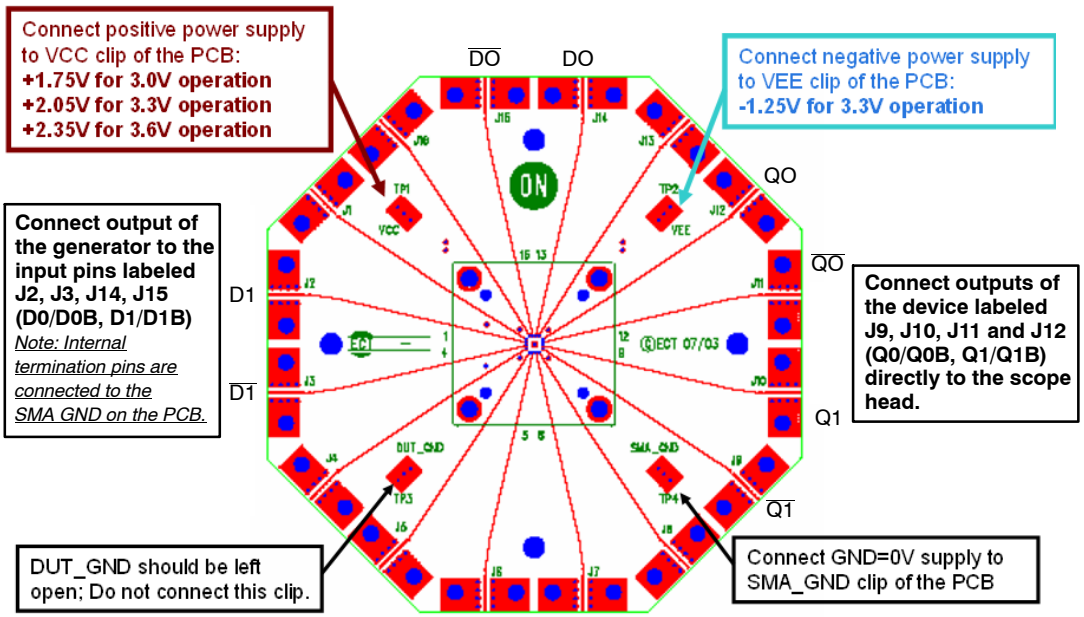


Figure 4. Lab Setup for NB4N527S

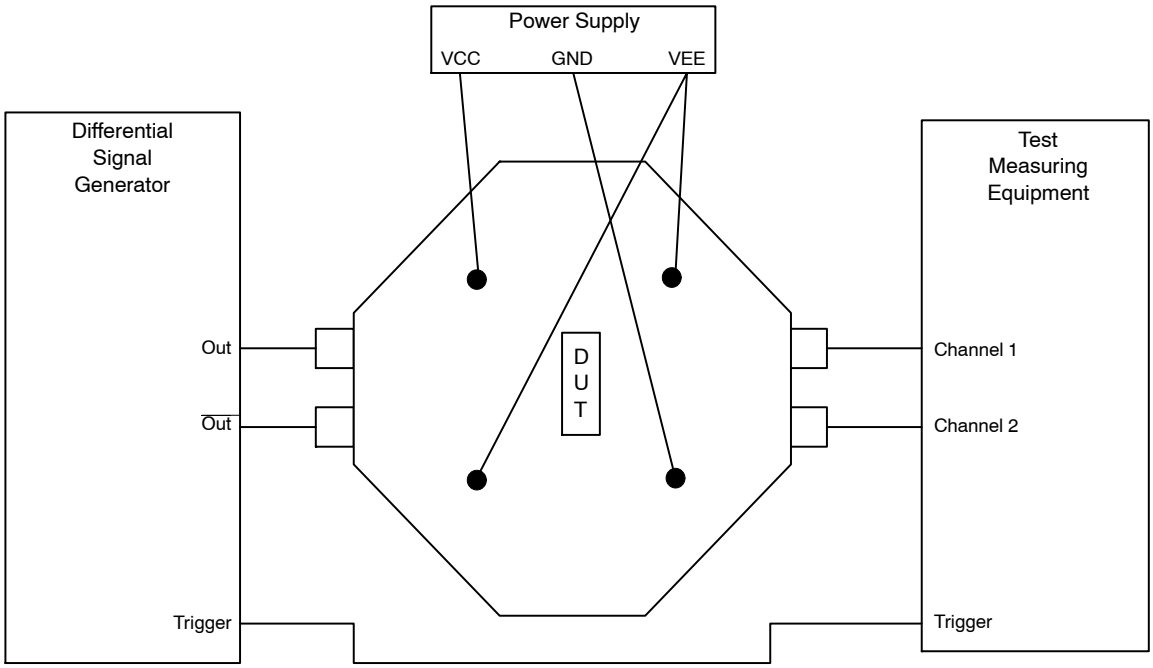


Figure 5. Simplified Equipment Lab Setup Block Diagram

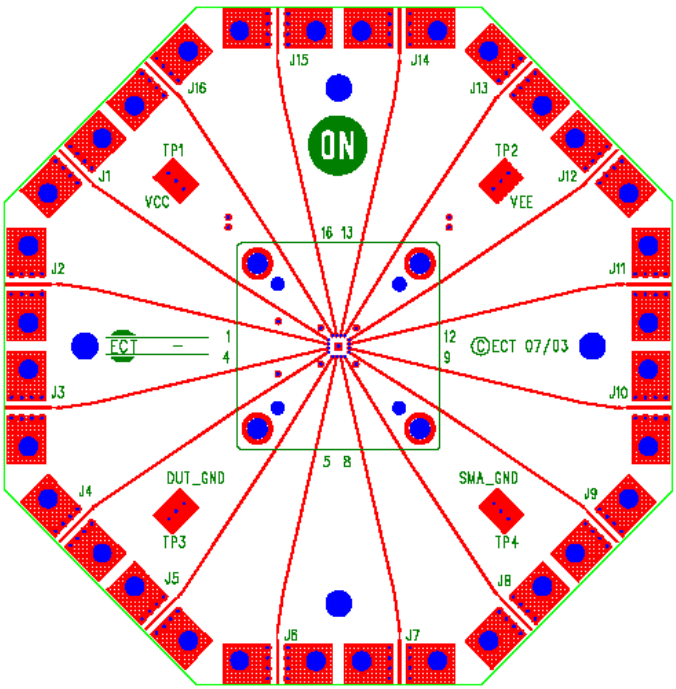
1. Connect appropriate power supplies to V_{CC}, V_{EE}, SMA_GND, and SMA_DUT.
2. Connect a signal generator to the input SMA connectors. Setup input signal according to the device data sheet.
3. Connect a test measurement device on the device output SMA connectors.

NOTE: The test measurement device must contain 50 Ω termination.

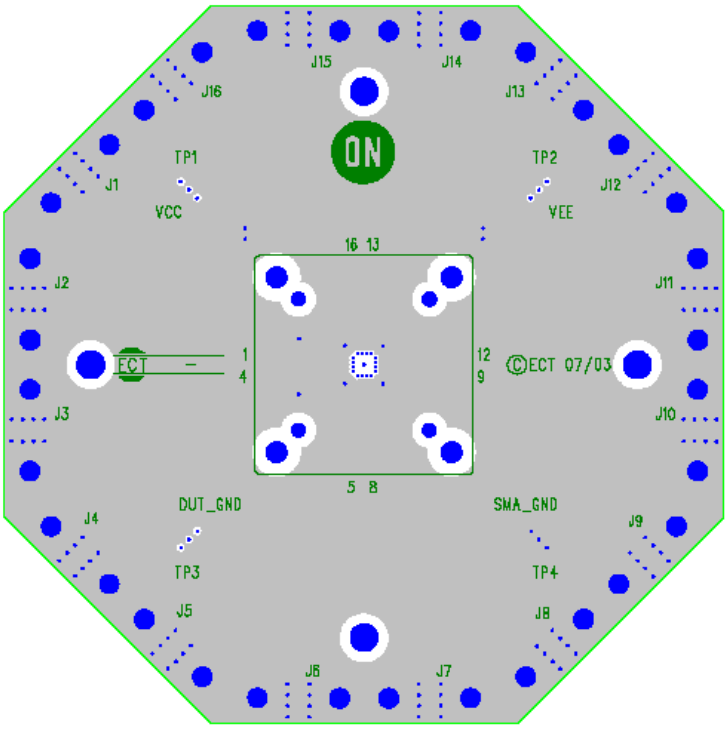
Table 3. Bill of Materials

Components	Manufacturer	Description	Part Number	Qty.	Web Site
SMA Connector	Johnson* Rosenberger	SMA Connector, Side Launch, Gold Plated	142−0701−851 32K243−40ME3	8	http://www.johnsoncomponents.com http://www.rosenbergerna.com
Surface Mount Test Points	Keystone*	SMT Miniature Test Point	5015	4	http://www.keyelco.com
Chip Capacitor	AVC Corporation*	0603 0.01 μF ± 10% 10 μF ± 10%	06035C103KAT2A T491C106K016AS	4 2	http://www.avxcorp.com
Chip Resistor	Panasonic*	0402 50 Ω ± 1% Presicion Thick Film Chip Resistor	ERJ−2RKF49R9X	Optional**	http://www.panasonic.com
Evaluation Board	ON Semiconductor	QFN 16 Evaluation Board	ECLQFN16EVB	1	http://www.onsemi.com
Device Samples	ON Semiconductor	QFN 16 Package Device	NB4N527SMN	1	http://www.onsemi.com

*Components are available through most distributors, i.e. www.newark.com, www.Digikey.com

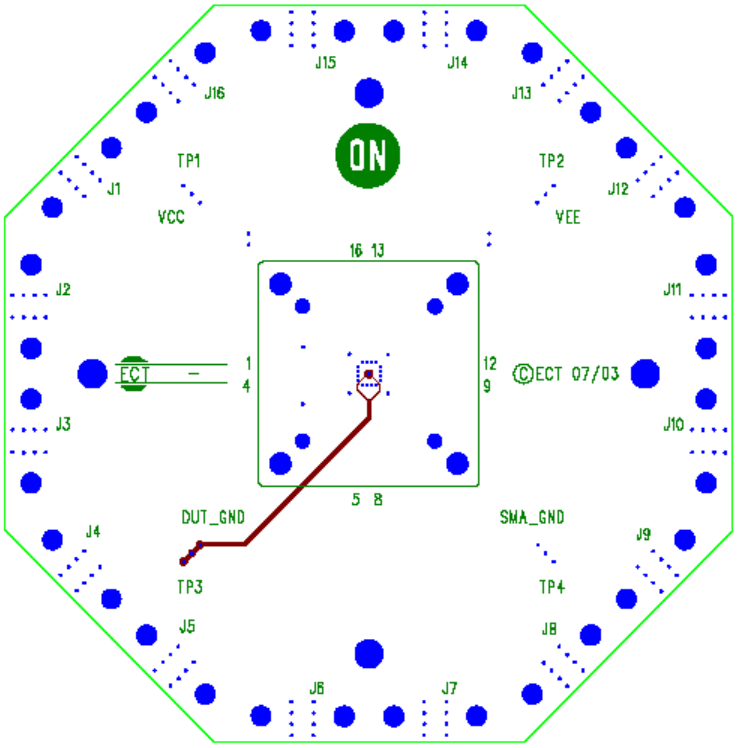


Top Layer

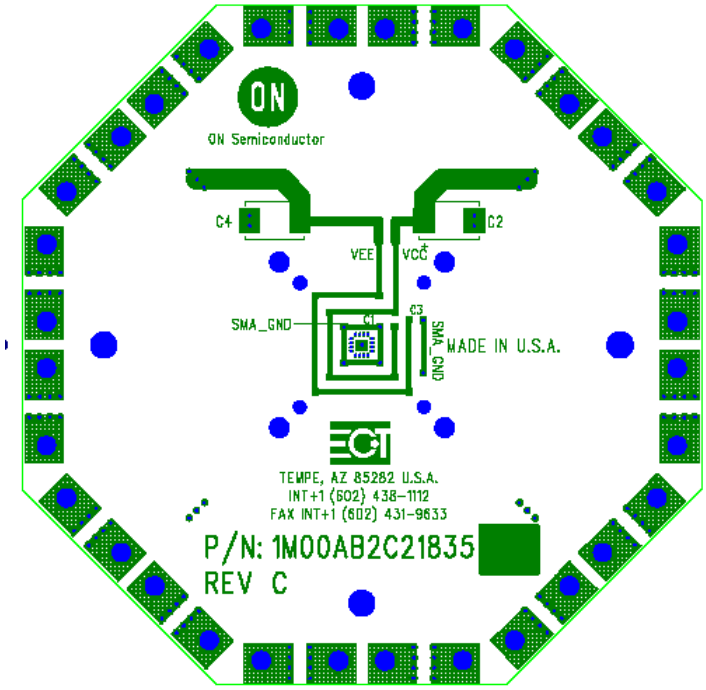


Second Layer (SMA_GND Plane)

Figure 6. Gerber Files



Third Layer (DUT_GND Trace)



Bottom Layer

Figure 7. Gerber Files

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