

- 1 Material: Isola IS400 or similar recommended
  - 2 Finish: ENIG (Electroless Nickel Immersion Gold), nickel layer  $1 \div 4 \mu\text{m}$ , gold layer  $0.076 \div 0.2 \mu\text{m}$
  - 3 All gerber files generated as a top view
  - 4 Gerber files for internal power planes have to be inverted for manufacturing !
5. Fabricate according IPC-A-600
  6. Non-conductive epoxy ink recommended for silkscreen
  7. Silkscreen should not cover any exposed copper, silkscreen gerber data have to be trimmed eventually
  8. All holes diameter refer to final diameter after eventual plating

#### Gerber and drill file extensions table

Gerber files	Description
.GTO	Top side silkscreen
.GTP	Top side solder paste mask
.GTS	Top side solder mask
.GTL	L1_TOP - Top Layer
.GBL	L2_BOTTOM - Bottom Layer
.GBS	Bottom side solder mask
.GBP	Bottom side solder paste mask
.GBO	Bottom side silkscreen
.GM1	Board outline
<b>Drill files</b>	

## SECO-BAT-FUSE-GEVB

**Revision:**  
rev 0.1

**State:**  
in work

*PCB fabrication notes and requirements*

Fabrication  
document

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Engineer: Marek Vajsabel

Date: 26/03/2020

PCB File: PCM\_LC05111CMT.PcbDoc

Repository revision: locally modified 1251

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Layer Stack

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.0102mm(0.400mil)	Solder Resist	Solder Mask	GTS
Copper	Top Layer	0.0356mm(1.400mil)		Signal	GTL
Core		0.7100mm(27.953mil)	FR-4	Dielectric	
Copper	Bottom Layer	0.0356mm(1.400mil)		Signal	GBL
Surface Material	Bottom Solder	0.0102mm(0.400mil)	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
Total thickness: 0.8014mm(31.553mil)					

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in work*Layer stack details*Fabrication  
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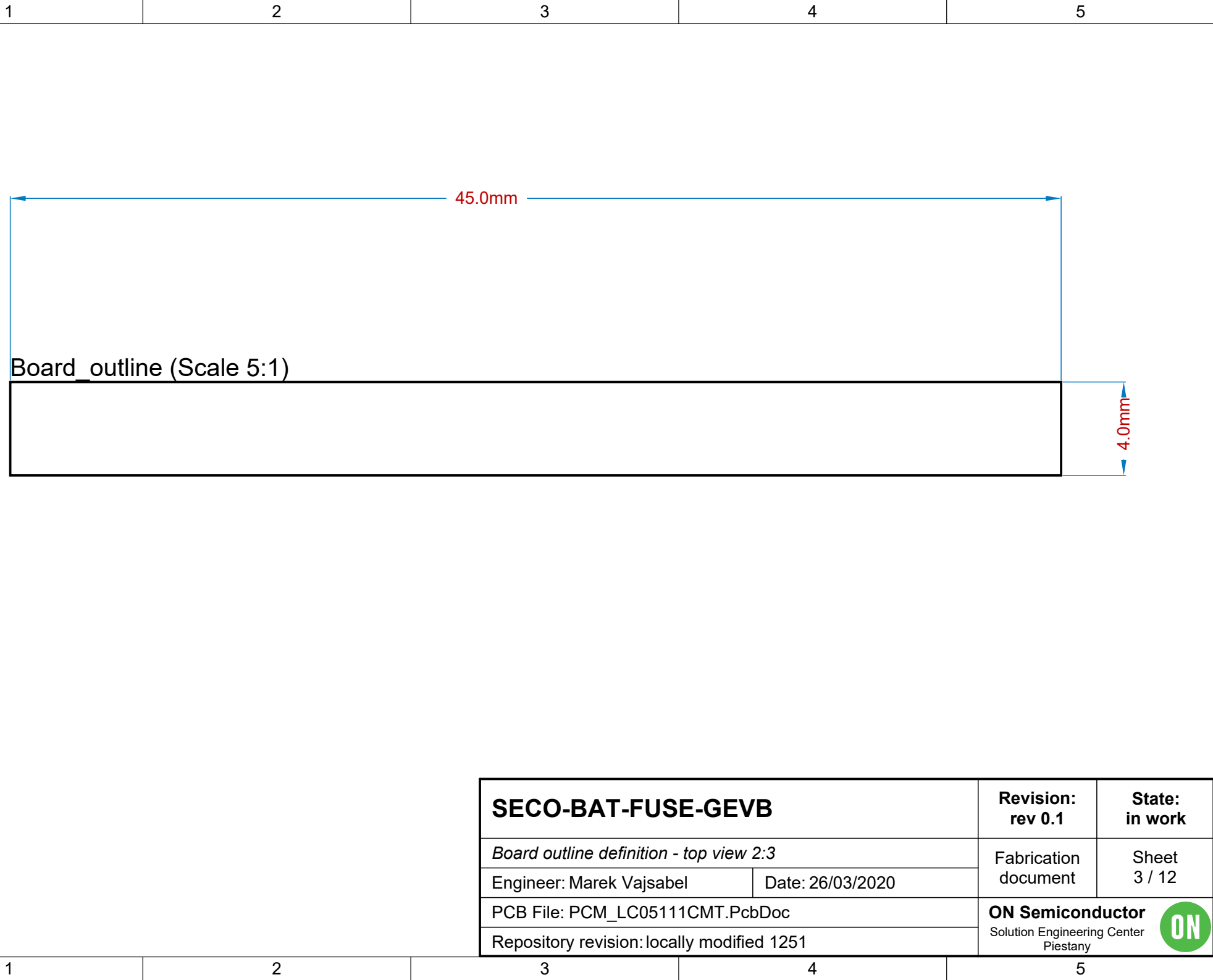
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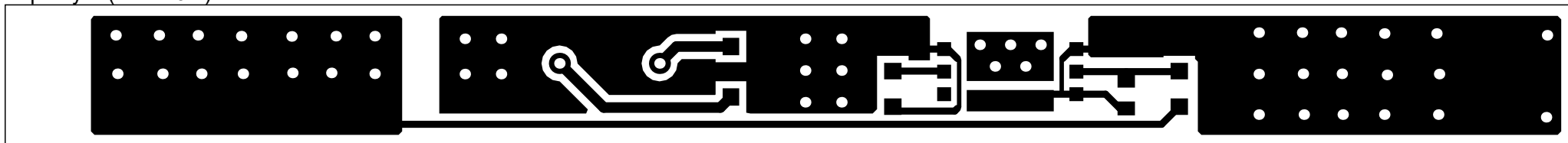
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Top Layer (Scale 6:1)



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<b>SECO-BAT-FUSE-GEVB</b>		<b>Revision:</b> rev 0.1	<b>State:</b> in work
<i>Top side silkscreen - top view</i>		Fabrication document	Sheet 4 / 12
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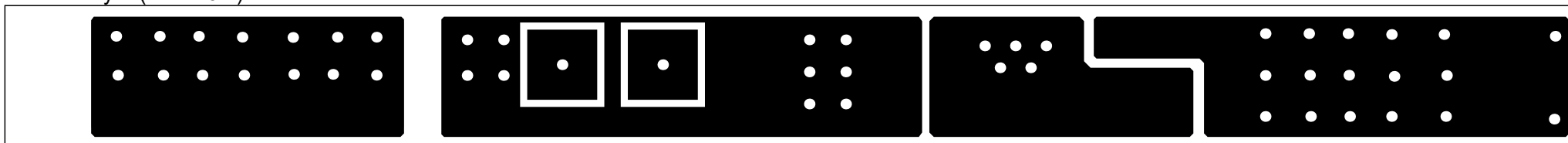
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Bottom Layer (Scale 6:1)



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<b>SECO-BAT-FUSE-GEVB</b>		<b>Revision:</b> rev 0.1	<b>State:</b> in work
<i>Top side solder paste - top view</i>		Fabrication document	Sheet 5 / 12
Engineer: Marek Vajsabel	Date: 26/03/2020		
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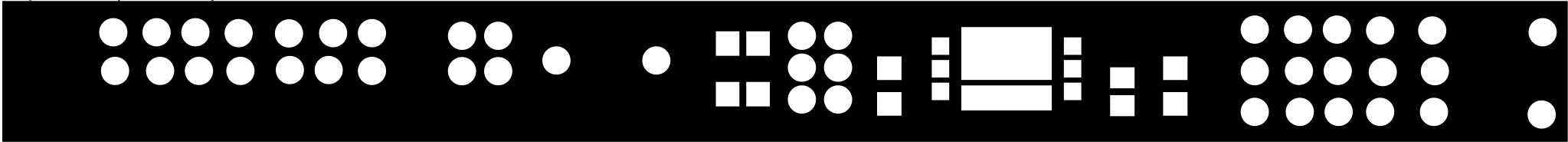
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Top Solder (Scale 6:1)



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Top side solder mask - top view		Fabrication document	Sheet 6 / 12
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Bottom Solder (Scale 6:1)



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Top Layer - top view		Fabrication document	Sheet 7 / 12
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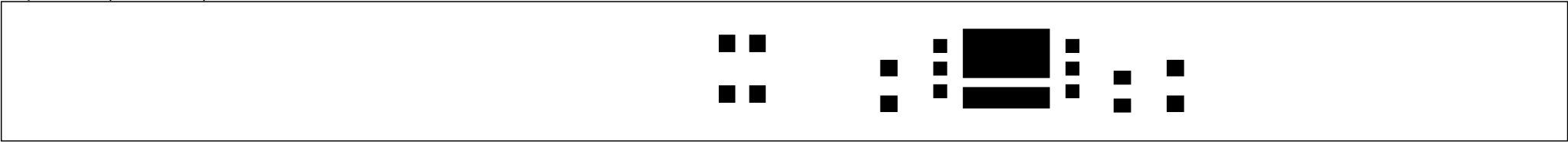
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Top Paste (Scale 6:1)



<b>SECO-BAT-FUSE-GEVB</b>		<b>Revision:</b> rev 0.1	<b>State:</b> in work
<i>L2_GND - internal power plane - top view</i>		Fabrication document	Sheet 8 / 12
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Bottom Paste (Scale 6:1)



<b>SECO-BAT-FUSE-GEVB</b>		<b>Revision:</b> rev 0.1	<b>State:</b> in work
<i>L3_PWR - internal power plane - top view</i>		Fabrication document	Sheet 9 / 12
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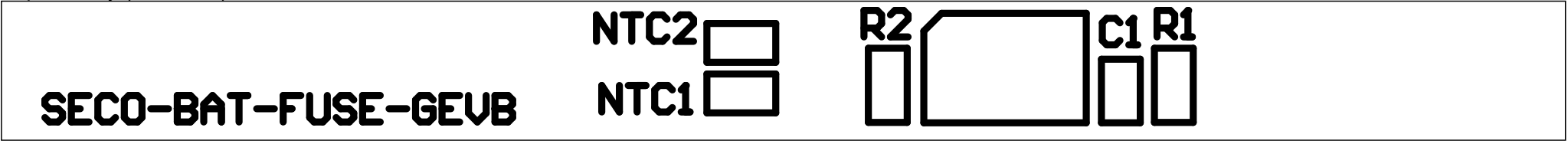
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Top Overlay (Scale 6:1)




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SECO-BAT-FUSE-GEVB		Revision: rev 0.1	State: in work
Bottom Layer - top view		Fabrication document	Sheet 10 / 12
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Bottom Overlay (Scale 6:1)

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-3A9

-TAB

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**SECO-BAT-FUSE-GEVB**

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in work

*Bottom side solder mask - top view*

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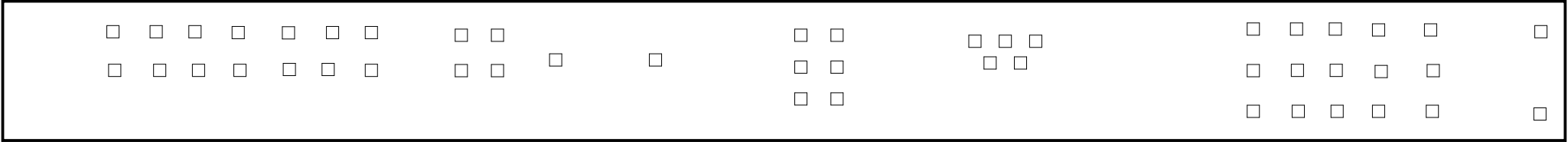
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Drill Drawing View (Scale 6:1)



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad	Template
□	48	0.305mm(12.0mil)	Plated	Top Layer - Bottom Layer	Via	(Mixed)
	48 Total					

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<i>Drill drawing</i>		Fabrication document	Sheet 12 / 12
Engineer: Marek Vajsabel	Date: 26/03/2020		
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