High Voltage Drivers Technical & Design Overview

ASG/MCC/PCS – Sept, 2022
Introduction

• This presentation covers several technical aspects of High Voltage Gate Drivers to provide explanations and guidance’s to engineers designing with onsemi devices.

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Agenda

- What is a HVIC driver
- Key Parameters of HVIC drivers
- Design & Components Selection
- Common issues when using HVIC drivers
- PCB Layout Considerations
- Noise Immunity Performance
- Power Losses & Thermal considerations
- Tools and Generic Help
What is a HVIC driver
Why using High voltage Gate drivers

- Can be directly connected to a microcontroller
- High current output drive
  - Enable high current driving w/o external current buffer in IGBT & MOSFET application
    (If driving switches in parallel external buffer would be recommended)
- Does not require secondary power supply as power supply is created by bootstrap method
- High dV/dt immunity up to 50V/ns
- Embedded Functions & Protections
  - Under Voltage Lockout (UVLO)
  - Dead-time Control
  - Shut-down Function
  - Current Sensing
  - Thermal Shut-down
  - Fault Output
Key Specification of High Voltage Gate Drivers

- 3.3 V and 5 V Input Logic Compatible
- Offset Supply Voltage Level (80 V, 200 V, 600 V and 1200 V)
- Driving Current Capability (From 90 mA up to 4.5 A)

Dynamic Characteristics
- Turn-On/Off propagation Delay Time
- Delay matching between Turn-on and off propagation
- Delay matching between high side and low side (As low as 10ns, 50ns Typ)
- Turn-on rise time and Turn-off fall time

Ruggedness
- CMOS Schmitt-triggered inputs with pull-down for noise immunity
- $dV/dt$ transient immunity voltage level (50 V/ns)
- Allowable negative Vs for high side signal propagation
- Noise immunity on the supply (Positive and negative)

Functions
- Over current protection, Fault reporting, Soft off, built in Bootstrap diode, internal oscillator
- Under Voltage Lockout (UVLO)
- Dead-time control
- Shut-down function
Functional Block Diagram of HV Gate Drive IC

- Pulse generator for edge triggered output
- High voltage level shifter
- dVs/dt noise cancellation circuit
- Input Circuit
- Delay matching

- High Side Gate Driver
- Low Side Gate Driver
- Others Functional Block

- SCHMITT TRIGGER INPUT
- SHAFT THROUGH PREVENTION
- CONTROL LOGIC

- UVLO
- DELAY
- DRIVER

- LIN
- HIN
- SD
- CSC
- GND

- VDD
- LO
- VSL

- VB
- HO
- VS
- VDD
- FO

- 0.5V
- 1.5V

- 20mA

- 20mA
HV Gate Drive IC (HVIC)

**Functional Block Diagram**

**Timing Chart**
**HVIC Main Features**

**Typical Application Circuit**

**Benefits**

- Better noise immunity (due to noise canceling circuit over high dv/dt common-mode noise)
- Low power consumption (IQBS / IQCC are lower than competitor's device)
- \( \frac{dV}{dt} \) transient immunity voltage level (50V/ns)
- Extended allowable negative \( V_s \) swing to -9.8V for signal propagation @ \( V_{CC}=V_{BS}=15V \)
- Matched propagation delay below 50nS
- UVLO functions
- TTL compatible input threshold levels
Key Parameters of HVIC drivers
# Gate Driver: Key attributes & Requirements

| Turn ON/OFF power switch | • Source/Sink Drive strength  
|                          | • Miller Clamp  
|                          | • External VEE input  
|                          | • Split output pins for source / sink  
| Level shifting | • Noise Immunity  
|                | • Separate power and signal ground  
|                | • Galvanic Isolation  
| Timing | • Propagation Delay  
|        | • Delay Matching  
|        | • Blanking, filters and time to protect  
| Protection Functions | • Under/Over Voltage Lockout  
|                      | • Shoot Through Prevention  
|                      | • Desat Protection  
|                      | • Overcurrent Protection  

- Choosing drive strength is often a balance between reducing power losses and minimizing EMI
- Negative voltage spikes result from parasitic inductances
- MOSFETs, used for higher switching frequencies, need shorter propagation delay
- Robust gate drive protection features, make the drivers well-suited for all power devices
Key parameters of the drivers – Drive peak current

This is very simplified schematic of the output of the driver. The Q3 and Q4 are the switchers which provides sink and source current described by DS. The Q1 and Q2 has to charge the gate capacitances of Q3 and Q4, this capacitance is higher with larger transistors. The result is, even for zero load capacitance on DRVx pin the rise and fall time will not be zero.

- Do not just compare the current capability, compare also the rise and fall time for given capacitance.
Key parameters of the drivers – Drive peak current

- $I_{\text{DRVx\_source}}, I_{\text{DRVx\_sink}}$ – the current value is measured by shorting the DRVx pin to GND or VDD. The value is not stable (here NCP5183). The rise and fall time for given load (capacitor) can be calculated only in case, the current is constant and the current is provided in zero time after turn on/off.

- This is not true, so the stronger driver does not always mean faster turn on/off of the switch !!!

- Real performance comes from the technology and circuit design.
Key parameters of the drivers – Rise/fall time vs. drive current

- ON is spec’d as 3.5/3.0 A
- Compet is spec’d as 4.0/4.0 A

Load – 1nF @ Vcc – 12 V

Peak current capabilities relates to shorter R/F times only at high Cload (>= 10 nF)
Key parameters of the drivers – Output resistance

- $R_{OH}$, $R_{OL}$ – the internal resistance of the driver. The parameter is important in case, you want to split power loss between a driver and external gate resistance.

- This $R_{dson}$ varies with $V_{DS}$. 
**Definition for Dynamic Characteristics**

Dynamic Electrical Characteristics

\[ T_A = 25°C, \ V_{IH\text{D}}, \ V_{BS1,2,3} = 15.0 \text{ V}, \ V_{S1,2,3} = \text{COM}, \ C_{\text{RCIN}} = 2 \text{ nF}, \text{ and } C_{\text{LOUT}} = 1000 \text{ pF} \] unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{on} )</td>
<td>Turn-On Propagation Delay</td>
<td>( V_{L H1,2,3} = V_{H H1,2,3} = 5 \text{ V}, V_{S1,2,3} = 0 \text{ V} )</td>
<td>350</td>
<td>500</td>
<td>650</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{off} )</td>
<td>Turn-Off Propagation Delay</td>
<td>( V_{L H1,2,3} = V_{H H1,2,3} = 0 \text{ V}, V_{S1,2,3} = 0 \text{ V} )</td>
<td>350</td>
<td>500</td>
<td>650</td>
<td>ns</td>
</tr>
<tr>
<td>( t_r )</td>
<td>Turn-On Rise Time</td>
<td>( V_{L H1,2,3} = V_{H H1,2,3} = 5 \text{ V} )</td>
<td>20</td>
<td>50</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>( t_f )</td>
<td>Turn-Off Fall Time</td>
<td>( V_{L H1,2,3} = V_{H H1,2,3} = 0 \text{ V} )</td>
<td>10</td>
<td>30</td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{en} )</td>
<td>Enable LOW to Output Shutdown Delay</td>
<td>From ( V_{CBO} = 1 \text{ V} ) to ( \overline{FO} ) Turn-Off</td>
<td>400</td>
<td>500</td>
<td>600</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CELT} )</td>
<td>CS Pin Leading-Edge Blanking Time</td>
<td>From ( V_{CBO} = 1 \text{ V} ) to Starting Gate Turn-Off</td>
<td>400</td>
<td>650</td>
<td>850</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CFO} )</td>
<td>Time from CS Triggering to ( \overline{FO} )</td>
<td>From ( V_{CBO} = 1 \text{ V} ) to ( \overline{FO} ) Turn-Off</td>
<td>850</td>
<td>1300</td>
<td>1300</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CSOFF} )</td>
<td>Time from CS Triggering to Low-Side Gate Outputs Turn-Off</td>
<td>From ( V_{CBO} = 1 \text{ V} ) to Starting Gate Turn-Off</td>
<td>850</td>
<td>1300</td>
<td>1300</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{LTIN} )</td>
<td>Input Filtering Time ( (HI_{N1}, L_{IN1}, EN) )</td>
<td>From ( V_{CBO} = 1 \text{ V} ) to Starting Gate Turn-Off</td>
<td>170</td>
<td>250</td>
<td>330</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{FLTCR} )</td>
<td>Fault-Clear Time</td>
<td>From ( V_{CBO} = 1 \text{ V} ) to Starting Gate Turn-Off</td>
<td>1.30</td>
<td>2.35</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>( * )</td>
<td>Dead Time</td>
<td>Dead-Time Matching (All Six Channels) ( (7) )</td>
<td>230</td>
<td>320</td>
<td>400</td>
<td>ns</td>
</tr>
<tr>
<td>( MDT )</td>
<td>Dead-Time Matching (All Six Channels) ( (7) )</td>
<td>From ( V_{CBO} = 1 \text{ V} ) to Starting Gate Turn-Off</td>
<td>1 ( DT1 )</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( * )</td>
<td>Delay Matching (All Six Channels) ( (7) )</td>
<td>From ( V_{CBO} = 1 \text{ V} ) to Starting Gate Turn-Off</td>
<td>50</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( PM )</td>
<td>Output Pulse-Width Matching ( (6) )</td>
<td>( PW_{IN} &gt; 1 \mu s )</td>
<td>50</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

- \( DT1 \) : Dead Time @ HO Turn-off to HO Turn-on
- \( DT2 \) : Dead Time @ LO Turn-off to LO Turn-on
- \( MTON \) : Delay Matching, HO & LO Turn-on
- \( MTOFF \) : Delay Matching, HO & LO Turn-off
Key parameters of the drivers - Prop delays & Rise/Fall Times

- **t\text{ON}, t\text{OFF}** – is the time needed for pulse to pass through the device. Input signal sharp edge, output one measured at 10%, to measure just propagation delay, not driver capability. When there is an input filter, the filter time is included into the propagation delay.

- **t_r, t_f** – is the time needed to charge and discharge a capacitor of specific value (usually 1 nF). The rise and fall time are somehow linked with driver current capability but not directly.

Higher driver current does not directly translate into shorter Turn-On/Turn-Off times.
Key parameters of the drivers - Input Filters & Impact on Prop. delay

Input filter function is demonstrated on NCP51530 device. Versions A and B are available:
The A version, features a noise rejection function to ensure that any pulse glitch shorter than 30 ns will not produce any output change.
The B version, has no such filters in the input stages, the output signal is just delayed.
Key parameters of the drivers – Delay Matching

- $t_{MT}$ – delay matching time. During testing four values are measured. The propagation delay for low side and high side driver, for positive and negative pulses.
- It is the time difference between the output of both channels

When paralleling MOS they’re driven simultaneously
- Gate drivers outputs to increase driving capabilities
# Conditions for Safe Operation

## Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristics</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_S$</td>
<td>High-side offset voltage</td>
<td>$V_B$-25</td>
<td>$V_B$+0.3</td>
<td>V</td>
</tr>
<tr>
<td>$V_B$</td>
<td>High-side floating supply voltage</td>
<td>-0.3</td>
<td>625</td>
<td>V</td>
</tr>
<tr>
<td>$V_{HO}$</td>
<td>High-side floating output voltage HO</td>
<td>$V_S$-0.3</td>
<td>$V_B$+0.3</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Low-side and logic fixed supply voltage</td>
<td>-0.3</td>
<td>25</td>
<td>V</td>
</tr>
<tr>
<td>$V_{LO}$</td>
<td>Low-side output voltage LO</td>
<td>-0.3</td>
<td>$V_{CC}$+0.3</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Logic input voltage (HI, LIN)</td>
<td>-0.3</td>
<td>$V_{CC}$+0.3</td>
<td>V</td>
</tr>
<tr>
<td>COM</td>
<td>Logic ground</td>
<td>$V_{CC}$-25</td>
<td>$V_{CC}$+0.3</td>
<td>V</td>
</tr>
<tr>
<td>$dV_S/dt$</td>
<td>Allowable offset voltage slew rate</td>
<td>50</td>
<td></td>
<td>V/μs</td>
</tr>
<tr>
<td>$P_D^{(2)(3)(4)}$</td>
<td>Power dissipation</td>
<td>8-SOP 0.625</td>
<td>14-SOP 1.0</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8-DIP 1.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\theta_{JA}$</td>
<td>Thermal resistance, junction-to-ambient</td>
<td>8-SOP 200</td>
<td>14-SOP 110</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8-DIP 100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_J$</td>
<td>Junction temperature</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage temperature</td>
<td>150</td>
<td></td>
<td>°C</td>
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</tbody>
</table>

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### Risk Factors of Malfunction

#### Factors related to Process

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristics</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_s$</td>
<td>High-side offset voltage</td>
<td>$V_B - 0.3$</td>
<td>$V_B + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_b$</td>
<td>High-side floating supply voltage</td>
<td>-0.3</td>
<td>625</td>
<td>V</td>
</tr>
<tr>
<td>$V_{HO}$</td>
<td>High-side floating output voltage HO</td>
<td>$V_s - 0.3$</td>
<td>$V_B + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Low-side and logic fixed supply voltage</td>
<td>-0.3</td>
<td>25</td>
<td>V</td>
</tr>
<tr>
<td>$V_{LO}$</td>
<td>Low-side output voltage LO</td>
<td>-0.3</td>
<td>$V_{CC} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Logic input voltage (HIN, LIN)</td>
<td>-0.3</td>
<td>$V_{CC} + 0.3$</td>
<td>V</td>
</tr>
</tbody>
</table>

#### Basic Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristics</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CCUV+}$, $V_{BSUV+}$</td>
<td>$V_{CC}$ and $V_B$ supply under-voltage positive going threshold</td>
<td>8.2</td>
<td>9.2</td>
<td>10.0</td>
</tr>
<tr>
<td>$V_{CCUV-}$, $V_{BSUV-}$</td>
<td>$V_{CC}$ and $V_B$ supply under-voltage negative going threshold</td>
<td>7.6</td>
<td>8.7</td>
<td>9.6</td>
</tr>
<tr>
<td>$V_{CCUVH}$, $V_{BSUVH}$</td>
<td>$V_{CC}$ supply under-voltage lockout hysteresis</td>
<td>0.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Logic &quot;1&quot; input voltage</td>
<td>2.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Logic &quot;0&quot; input voltage</td>
<td>0.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_S$</td>
<td>Allowable negative $V_S$ pin voltage for HIN signal propagation to HO</td>
<td>-9.8</td>
<td>-7.0</td>
<td>V</td>
</tr>
</tbody>
</table>
Design & Components Selection
How to select the Bootstrap Capacitor (1/2)

A resistor ($R_{BOOT}$) is placed in series with bootstrap diode so to limit the current when the bootstrap capacitor is initially charged. The value should not exceed the ohms (typically 5~10 Ω), which would increase the VBS time constant.

\[
\tau = \frac{R_{BOOT} \cdot C_{BOOT}}{D} \text{[s]} \quad (\approx 3 \text{nC})
\]

### Minimum Value of $C_{BOOT}$

\[
C_{BOOT\ min} = \frac{Q_{TOTAL}}{\Delta V_{BOOT}}
\]

### Total charge of the bootstrap capacitor

\[
Q_{TOTAL} = Q_{GATE} + (I_{LKCAP} + I_{LKG} + I_{QBS} + I_{LK}) \times t_{ON} + Q_{LS}
\]

### Maximum allowable voltage drop on $C_{BOOT}$

\[
\Delta V_{BOOT} = V_{DD} - V_F - V_{GAIN}
\]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_{GATE}$</td>
<td>Total Gate charge</td>
</tr>
<tr>
<td>$I_{LKCAP}$</td>
<td>Bootstrap capacitor leakage current</td>
</tr>
<tr>
<td>$I_{LKG}$</td>
<td>Switch gate-source leakage current</td>
</tr>
<tr>
<td>$I_{QBS}$</td>
<td>Bootstrap circuit quiescent current</td>
</tr>
<tr>
<td>$I_{LK}$</td>
<td>Bootstrap circuit leakage current</td>
</tr>
<tr>
<td>$I_{LK,DIODE}$</td>
<td>Bootstrap diode leakage current</td>
</tr>
<tr>
<td>$T_{ON}$</td>
<td>High side on time</td>
</tr>
<tr>
<td>$Q_{LS}$</td>
<td>Charge required by the internal level shifters</td>
</tr>
</tbody>
</table>
How to select the Bootstrap Capacitor (2/2)

◆ Design Example (HVIC : FAN7382, Switching Device : FCP20N60, Bootstrap Diode : UF4007)

If the maximum allowable voltage drop on the bootstrap capacitor is 1.0V during the high side switch on state, the minimum capacitor value is calculated by the following equation

\[
Q_{TOTAL} = Q_{GATE} + (I_{LKCAP} + I_{LKGS} + I_{QBS} + I_LK + I_{LKDIODE}) \cdot T_{ON} + Q_{LS}
\]

\[
Q_{TOTAL} = (98 \times 10^{-9}) + [(100 \times 10^{-9} + 120 \times 10^{-6} + 50 \times 10^{-6} + 10 \times 10^{-9}) \times (25 \times 10^{-6}) + (3 \times 10^{-9})] = 105.2 \times 10^{-9}[C]
\]

\[
C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{BOOT}} = \frac{105.2 \times 10^{-9}}{1} \approx 105[nF]
\]

The voltage drop due to the external diode is nearly 0.7V. We have assumed the capacitor charging time equal to the high side on time (duty cycle 50%)

Where as different bootstrap capacitor, The Voltage drop is

- 100 nF \to \quad \Delta V_{BOOT} = \frac{Q_{TOTAL}}{C_{BOOT}} = \frac{105nC}{100nF} = 1.05[V]
- 150 nF \to \quad \Delta V_{BOOT} = \frac{Q_{TOTAL}}{C_{BOOT}} = \frac{105nC}{150nF} = 0.7[V]
- 220 nF \to \quad \Delta V_{BOOT} = \frac{Q_{TOTAL}}{C_{BOOT}} = \frac{105nC}{220nF} = 0.48[V]
- 570 nF \to \quad \Delta V_{BOOT} = \frac{Q_{TOTAL}}{C_{BOOT}} = \frac{105nC}{570nF} = 0.18[V]

Suggested values are within the range of 100nF ~ 570nF, but the right value must be selected according to the application in which the device is used, when the capacitor value is too big, the bootstrap charging time is slowed and the low side on time might be not long enough to reach the right bootstrap voltage.
Possible Remedies against Bootstrap Circuit Problem

Adding a small resistor ($R_{\text{BOOT}}$) in series with bootstrap diode

The gate resistor was split into two resistors ($R_{\text{GATE}}$ and $R_{\text{VS}}$) and adding a low forward voltage drop schottky diode from ground to $V_S$.

This method can mitigate the problem. Unfortunately, the series resistor ($R_{\text{BOOT}}$) does not provide a foolproof solution against an over voltage and it also slows down the recharge process of the bootstrap capacitor. we suggest the bootstrap resistor, $R_{\text{BOOT}}$, not exceeding some Ohms (Typically 5~10Ohms) to avoid increasing the $V_{\text{BS}}$ time constant.

The only potential hazard by this circuit is that the charging current of the bootstrap capacitor must go through two resistors, $R_{\text{BOOT}}$ and $R_{\text{VS}}$. The time constant of $C_{\text{BOOT}} \cdot R_{\text{BOOT}}$ and $R_{\text{VS}}$ slows the recharge process which might be a limiting factor as the PWM duty ratio.

The gate resistor split into $R_{\text{GATE}}$ and $R_{\text{VS}}$ has a double purpose: It sets the turn-on and turn-off speed in the MOSFET and also provide current limiting for the schottky diode during the negative voltage transient of the source terminal of the main switch. In additional, the bootstrap capacitor is protected against over voltage by the two diodes connected to the ends of $C_{\text{BOOT}}$. 
Summary of Bootstrap Components Selection

✓ The bootstrap resistor must be considered in sizing the bootstrap resistance that the current developed during initial bootstrap charge. If a resistor is needed in series with the bootstrap diode.

✓ The bootstrap capacitor using low-ESR capacitor such as ceramic capacitor.

✓ And the capacitor from $V_{CC}$ to COM supports both the low-side driver and bootstrap recharge. We recommended a value at least 10 times higher than bootstrap capacitor.

✓ The bootstrap diode must be used a lower forward voltage drop and switching time as soon as possible fast recovery such as ultra-fast.

You can see more detailed information. Please refer to application note, AND-9674: Design and Application Guide of Bootstrap Circuit for HV Gate Driver IC.
How to dimension the gate resistance (1/2)

◆ Gate Resistances

The switching speed of the output transistor (MOSFET or IGBT) can be adjusted sizing the turn-on/off resistors controlling the turn-on and turn-off gate current.

✓ Sizing the turn-on gate resistor
Gate resistance may be chosen in order to fix either the switching-time or the output voltage slope. To obtain the desired switching time the gate resistance can be sized starting from Qgs, Qgd, VDD (or VBS), and Vgs.

\[
I_{g\ (avr)} = \frac{Q_{gs} + Q_{gd}}{t_{SW}} \quad R_{g\ (ON)} = R_{Total} - R_{DRV\ (ON)} = \frac{V_{DD} - V_{gs(\ th)}}{I_{g\ (avr)}} - \frac{V_{DD}}{I_{Source}}
\]

Where, \( R_{g\ (ON)} \) is the gate on resistance and \( R_{DRV\ (ON)} \) is the driver equivalent on resistance.

✓ Output voltage slope and relation with turn-on resistor
Turn-on resistor can be sized to control output voltage slope. (dVout/dt)

\[
\frac{dV_{out}}{dt} = \frac{I_{g\ (avr)}}{C_{gd\ (off)}} \quad \text{Therefore,} \quad R_{Total} = \frac{V_{DD} - V_{gs(\ th)}}{I_{g\ (avr)}} = \frac{V_{DD} - V_{gs(\ th)}}{C_{gd\ (off)} \frac{dV_{out}}{dt}}
\]

Where, \( C_{gd\ (off)} \) is the Miller effect capacitor, specified as \( C_{rss} \) in the datasheet.
How to dimension the gate resistance (2/2)

✓ Sizing the turn-off gate resistor

Turn-off gate resistor must be sized with applying worse case that the drain of the MOSFET in turn-off state is forced to commutate by external events.

The following equation relates the MOSFET gate threshold voltage to the drain dv/dt:

\[ V_{gs(th)} \geq (R_{g(off)} + R_{DRV(off)}) \cdot I_g = (R_{g(off)} + R_{DRV(off)}) \cdot C_{gd} \frac{dV_{out}}{dt} \]

\[ R_{g(off)} \leq \frac{V_{gs(th)}}{C_{gd}} \cdot \frac{dV_{out}}{dt} - \frac{V_{DD}}{I_{Sink}} \]

Where, \( R_{g(off)} \) is the gate on resistance, and \( R_{DRV(off)} \) is the driver equivalent resistance.
Common issues when using HVIC drivers
Latch-up Problem for Short Pulse input

Basically HVIC can transfer about 70 ns pulse, even though input Pulse Width is shorter than internal Pulse Width (typ. 150 ns) of short pulse generator.
But, It is necessary to protect against narrow PWM pulses lower than 100 ns. Generally, recommended min input pulse is 100 ns to avoid response or any malfunction of HVIC.
Please refer to AN-8102: Recommendations to Avoid Short Pulse Width Issues in HVIC Gate Driver Applications

Latest generations of HV drivers can work with shorter Input signals

<Root-cause of Short pulse latch-up>

<Test Result; Pulse width of Latch-up>
PCB Layout Considerations
Layout General Guidelines

- **Printed Circuit Board Layout : Gate Driver**
  - The “Layout” for minimized stray inductances as follows:
    - ✔ Direct tracks between switches with no loops or deviation.
    - ✔ Avoid interconnect links. These can add significant inductance.
    - ✔ Reduced the effect of lead-inductance by lowering package height above the PCB.
    - ✔ Consider co-locating both power switches to reduce track length.
    - ✔ Placement and routing for supply capacitor and gate resistors as close as possible to HVIC.
    - ✔ The bootstrap diode as close as possible to bootstrap capacitor.

- **Printed Circuit Board Layout : Super Junction MOSFET**
  - ✔ To achieve the best performance of Super-Junction MOSFETs, optimized layout is required.
  - ✔ Gate driver and Rg must be placed as close as possible to the MOSFET gate pin.
  - ✔ Separate POWER GND and GATE Driver GND.
  - ✔ Minimize parasitic C_{gd} capacitance and source inductance on PCB.
  - ✔ For paralleling Super-Junction MOSFETs, symmetrical layout is mandatory.
  - ✔ To reduce oscillation, slow down dv/dt and di/dt by increasing Rg or using ferrite bead.
Examples with High External $C_{GD}$ & Reduced $C_{GD}$

High External $C_{GD}$

- $A = x \cdot y$
- $C = \frac{\varepsilon_r \cdot \varepsilon_f \cdot A}{d}$
- External $C_{GD}$ too high!
- Capacity between trace pitches

Minimized External $C_{GD}$

- (a) double layer PCB
- (b) multi layer PCB
- Gnd-plane or shield-plane reduces $C_{GD}$
- Minimized external $C_{GD}$
Examples with High External $C_{GD}$ & Reduced $C_{GD}$ – Spikes During Turn off

**High External $C_{GD}$ – Higher Spikes**

**Minimized External $C_{GD}$ – Lower Spikes**
Paralleling MOSFETs

- Two independent totem pole drivers very close to MOSFET gate
- Minimized source inductance to reference point for gate drive minimized
- Minimized Cgd: Gate and Drain trace at 90° angle
Noise Immunity Performance
Why undershoot spike can be present on Vs?

- When there is negative voltage at the source of the switching device during turn-off it causes load current to flow in the low-side freewheeling diode as shown in below Figure. In this case, the inductive stray elements, \( L_S \), may push \( V_s \) below COM. The amplitude of negative voltage is proportional to the stray inductances and the turn-off speed, \( \frac{di}{dt} \), of the switching device.

- The amplitude of negative voltage given by as below equation,

\[
V_s - COM = -(L_S) \frac{di}{dt}
\]

- For example, in a 10 A gate driver with 100 nH stray inductance has a 50 ns switching time, the amplitude of negative voltage spike between \( V_s \) and ground is -20 V.

\[
V_s - COM = -(100 \times 10^{-9}) \frac{10}{50 \times 10^{-9}} = -20[V]
\]
Why is undershoot spike on Vs pin important?

✓ Effects of the undershoot spike on the output pin (Vs)

Case 1. If undershoot voltage is present on Vs pin, the high side output will temporarily latch in its current state. → Happen when upper and lower switches are short-circuit condition in Half-Bridge topology.

Case 2. If the output pin undershoot spike has a duration in the order to of tenths of nanoseconds the bootstrap capacitor can become overcharged. → Exceed the absolute maximum voltage (V_{BS}) limits in the high side gate driver

Case 3. Provided Vs remains within absolute maximum limits the IC will not suffer damages, however if Vs is lower than “Allowable negative Vs voltage” which was specified in the data sheet, input signal for high-side cannot be delivered to the high-side gate driver while undershoot → At this situation, the level shifter of the HVIC suffers from a lack of the operating voltage headroom.
The Definition of NPSOA (Neg. Pulse Safety of Area)

- When high side MOSFET is turned off, negative VS undershoot occurs by low side freewheeling current. Excessive negative VS undershoot can result in malfunction or destruction of HVIC.

- VS-NPSOA describe allowable negative VS in terms of negative pulse width and voltage level.

※ Note: We do not guarantee Recommended SOA regarding MP condition, but just provide reference data according to test results.
Typical VS immunity curve - NPSOA

- Typical VS-NPSOA curves were made based on real test measurement value.
- Curve means malfunction or damage point of HVIC.
- Onsemi HVIC shows better ruggedness of negative pulse VS than competitors.
Results of Negative Vs Pulse & DC Level Test

◆ Add Positive/Negative Noise on \( V_s \)
- Negative: \( V_{DD}=15 \text{ V}, V_{CC}=V_B=15 \text{ V}, \) VS= 50ns, Positive/Negative Pulse Noise on \( V_s \)

◆ Test Result

<table>
<thead>
<tr>
<th>Negative Noise Peak</th>
<th>FAN7392</th>
<th>Competitor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NORMAL</td>
<td>ABNORMAL OPERATION</td>
</tr>
<tr>
<td>VS Noise</td>
<td>-10 -20 -30 -40 -50 -60 -70 -80 -90 -100</td>
<td></td>
</tr>
<tr>
<td>FAN7392</td>
<td>-27.8 V</td>
<td></td>
</tr>
<tr>
<td>Competitor</td>
<td>-6.4 V</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Negative DC Voltage</th>
<th>FAN7392</th>
<th>Competitor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NORMAL OPERATION</td>
<td>ABNORMAL</td>
</tr>
<tr>
<td></td>
<td>-1 -2 -3 -4 -5 -6 -7 -8 -9 -10</td>
<td></td>
</tr>
<tr>
<td>FAN7392</td>
<td>-10.19 V</td>
<td></td>
</tr>
<tr>
<td>Competitor</td>
<td>-6.38 V</td>
<td></td>
</tr>
</tbody>
</table>
# Waveforms of Negative Vs Pulse & DC Level Test

<table>
<thead>
<tr>
<th>Pulse</th>
<th>FAN7392</th>
<th>-27.8 V</th>
<th>I-Company’s A</th>
<th>-6.4V</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>[10V/div]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_s$</td>
<td>[10V/div]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{HO}$</td>
<td>[10V/div]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{LO}$</td>
<td>[10V/div]</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Latch off

<table>
<thead>
<tr>
<th>DC</th>
<th>FAN7392</th>
<th>-10.19/-10.20V</th>
<th>I-Company’s A</th>
<th>-6.38/-6.40V</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_s$</td>
<td>[2V/div]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{HO}$</td>
<td>[10V/div]</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Missing
Waveforms of Negative Vs Pulse & DC Level Test

**Equation**

When Temp = 25°C, $V_{DD} = 15$ V, $V_{DBOOT} = 1$ V, $V_R = 400$ V, Freq = 100 kHz, $T_{ON} = 150$ ns, $I_d = 13$ mA,

Set $Q_P = I_d \times T_{ON} = 5$mA $\times 150$ns = 0.75 nC

Reset $Q_P = I_d \times T_{ON} = 13$mA $\times 150$ns = 1.95 nC

Set $P_D = (V_{DD} - V_{DBOOT}) \times Q_P \times$ Freq = 14V $\times 0.75$nC $\times 100$KHz = 1 mW

Reset $P_D = (V_R + V_{DD} - V_{DBOOT}) \times Q_P \times$ Freq = 414V $\times 1.95$nC $\times 100$KHz = 81 mW
Appendix. HV IC Robustness Test Items

<table>
<thead>
<tr>
<th>Items</th>
<th>Test Objective</th>
<th>Test Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive $V_B$ Pulse</td>
<td>Output status of the high-side driver is memorized by an internal latch circuit. The latch status must be only changed by input signal’s rising and falling edges. However, a noise pulse applied to between $V_B$ and $V_S$ also can change the latch status. Such latch status change driven by the noise cause malfunction of HVIC. In general, it normally causes disastrous failure. Therefore, this test result gives how much the HVIC is robust against $V_{BS}$ pulse noise.</td>
<td><img src="image" alt="Test Circuit" /></td>
</tr>
</tbody>
</table>
Power Losses & Thermal considerations
Brief look on losses

**Half Bridge Driver Losses**

**Static**
- Low side quiescent current
- High side quiescent current
- High side to low side leakage current

**Dynamic**
- High side logic consumption
- Low side logic consumption
- Level shifter loss
- Charge and discharge external MOSFET, IGBT, etc.
Brief look on losses

The Losses on one slide

Static losses: 1. Quiescent current from the positive voltage supply $\rightarrow V_{CC} \cdot I_{QDD}$, $V_{boot} \cdot I_{Qboot}$
   2. Leakage current from the high side to low side $\rightarrow V_{BOOTpin} \cdot I_{HVleak}$

Dynamic losses: 1. Charge and discharge the gate of MOSFET $\rightarrow V_{CC} \cdot Q_{G} \cdot f_{SW}$
   there are two MOSFETS, multiple by 2
   2. Operating for level shifter $\rightarrow (V_{bulk} + V_{CC} - V_{Df_{boot}}) \cdot Q_{set,reset} \cdot f_{sw}$
   3. Internal dynamic loss $\rightarrow V_{CC} \cdot I_{CC}$, $V_{boot} \cdot I_{boot}$ without load condition

Bootstrap circuit loss: power loss on bootstrap diode and resistor during charging bootstrap capacitor and reverse bias power loss due to reverse recovery.
**Brief look on losses – NCV51511**

- **Condition:** Temp = 25°C, $V_{DD} = 12$ V, $V_{DBOOT} = 1$ V, $V_B = 80$ V, Freq = 100 kHz, $R_g = 0$ ohm, $Q_G$ of external MOSFET = 80 nC

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Equation</th>
<th>Calculation</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Loss at high side</td>
<td>$P_{D,q(HS)}$</td>
<td>$= V_{Boot} \times I_{LK}$</td>
<td>$= V_R \times I_{LK} = 80 \text{V} \times 0.3 \mu\text{A} = 2.4 \mu\text{W}$ (negligibility)</td>
<td>Calculated by leakage currents in the level shifting stage</td>
</tr>
<tr>
<td>Dynamic Loss on level shifter</td>
<td>$P_{D,sw(HS)}$</td>
<td>$(V_R + V_{DD} - V_{DBOOT}) \times \text{reset } Q_p \times f + (V_{DD} - V_{DBOOT}) \times \text{set } Q_p \times f$</td>
<td>$(V_R + V_{DD} - V_{DBOOT}) \times \text{reset } Q_p \times f + (V_{DD} - V_{DBOOT}) \times 0.48\text{nC} \times 100 \text{kHz} + (12\text{V} - 1\text{V}) \times 0.48\text{nC} \times 100\text{kHz} = 4.94 \text{mW}$</td>
<td>Calculated by the level shifting circuit. ($Q_p$ : Charge for level shifting circuit) See the appendix for more info.</td>
</tr>
<tr>
<td>Quiescent current power Loss</td>
<td>$P_{D,Q(LS)}$</td>
<td>$= V_{DD} \times (I_{QDD} + I_{QBS})$</td>
<td>$= V_{DD} \times (I_{QDD} + I_{QBS}) = 12 \text{V} \times (0.3 + 0.2) \mu\text{A} = 6 \text{mW}$</td>
<td>Calculated by quiescent currents from the supplies voltage</td>
</tr>
<tr>
<td>Internal Dynamic Loss in</td>
<td>$P_{predriver}$</td>
<td>$= P_{predriver} = V_{DD} \times (I_{PDD} + I_{PBS})$</td>
<td>$= V_{DD} \times (I_{PDD} + I_{PBS}) = 12 \text{V} \times (0.3 + 0.4) \mu\text{A} = 8.4 \mu\text{W}$</td>
<td>Dynamic losses associated internal pre-driver block See the datasheet</td>
</tr>
<tr>
<td>Gate driving Loss</td>
<td>$P_G$</td>
<td>$= 2xV_{DD} \times Q_G \times f$</td>
<td>$= 2xV_{DD} \times Q_G \times f = 2 \times 12 \text{V} \times 80 \text{nC} \times 100 \text{kHz} = 192 \text{mW}$</td>
<td>The losses in the gate drive resistance for charging external MOSFET ($Q_G$ : Total gate Charge of Switching Device)</td>
</tr>
<tr>
<td>Total Power Loss</td>
<td>$P_{Total}$</td>
<td>$= P_{D,q(HS)} + P_{D,q(LS)} + P_{D,sw(HS)} + P_{predriver} + P_G$</td>
<td>$= 4.94+6+8.4+192= 211.34 \text{mW}$</td>
<td></td>
</tr>
</tbody>
</table>

In NCV51511, the main power loss is dynamic losses for charging/discharging FET.
Brief look on losses – NCV51511 Thermal Analysis

◆ Power dissipation = 211.34 mW.

◆ If $\theta_{JA}$ and $T_a$ are given

$T_j = P_d \cdot \theta_{JA} + T_a = 0.21 \cdot 39 + T_a = 8.19 + T_a \ (^\circ C)$

◆ If $\Psi_{JL}$ is known and can measure lead temperature ($T_{Lead}$)

$T_j = P_d \cdot \Psi_{JL} + T_{Lead} = 0.21 \cdot 15 + T_{Lead} \ ^\circ C = 3.15 + T_{Lead} \ (^\circ C)$

◆ If $\Psi_{JT}$ is known and can measure case-top temperature ($T_{Top}$)

$T_j = P_d \cdot \Psi_{JT} + T_{Top} = 0.21 \cdot 6 + T_{Top} \ ^\circ C = 1.26 + T_{Top} \ (^\circ C)$

Junction temperature ($T_j$) should be controlled within the recommended operating temperature range

If $T_j$ is over than recommended operating temperature
1. Add external gate resistors to share the thermal distribution
2. Reduce switching frequency
3. Use heat sink

Table 4. THERMAL INFORMATION (Note 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\theta_{JA}$</td>
<td>Thermal Resistance Junction–Air (Note 4)</td>
<td>39</td>
<td>$^\circ C/W$</td>
</tr>
<tr>
<td>$\Psi_{JL}$</td>
<td>Thermal characterization parameter Junction–Lead</td>
<td>15</td>
<td>$^\circ C/W$</td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>Thermal characterization parameter Junction–Case (TOP)</td>
<td>6</td>
<td>$^\circ C/W$</td>
</tr>
</tbody>
</table>

4. As mounted on a 78.2 x 114.3 x 1.6 mm FR4 substrate with a Multi-layer of 1 oz copper traces and heat spreading area. As specified for a JEDEC 51–7 conductivity test PCB. Test conditions were under natural convection or zero air flow.
Brief look on losses

**NCV51511**
- Package SOIC8 EP
- $R_{tja} = 39 \, \text{K/W}$
- $P_{\text{loss}} = 211 \, \text{mW}$
- $t_j (@ \text{amb} = 60 ^\circ \text{C}) = 68.2 ^\circ \text{C}$

**NCV5183**
- Package SOIC8
- $R_{tja} = 183 \, \text{K/W}$
- $P_{\text{loss}} = 209 \, \text{mW}$
- $t_j (@ \text{amb} = 60 ^\circ \text{C}) = 98 ^\circ \text{C}$

The exposed pad decreases junction temperature by 30 °C
Quick tool for HVIC Drivers Loss & Thermal estimation

AND90004 : Analysis of Power Dissipation and Thermal Considerations for High Voltage Gate Drivers
(and Pβ calculator is linked in each devices’ landing page ‘Design & Development Tools’)

**Analysis of Power Dissipation and Thermal Considerations for High Voltage Gate Drivers**

**AND90004/D**

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amount of power depending on the operating conditions. It is important to determine the driver power dissipation and the resulting junction temperature to ensure the component is not over temperature. Figure 1 shows the typical input block diagram of HVIC. The main function blocks are the input stage, UVL06 protection, level shifter and output driver stages. The gate driver losses include:

- Static losses related with static current at high and low side circuit blocks when driver is biased and not switching.
- Dynamic losses related with dynamic current when the switching signal is applied to the switching device.
- Gate driver losses related with load switch charges and also directly dependent on switching frequency.

**Static Power Loss Analysis**

The Figure 2 shows a simplified schematic of the half bridge switch network associated with high and low side driver to explain the static losses.

**Gate Driving Loss Analysis**

The gate driver loss is the most significant power loss resulting from supplying gate current to switch the load MOSFET on and off at the switching frequency. The gate driving losses are coming from charging and discharging the load capacitor (for MOSFET) the load inductive (for IGBT) and expressed by the following equation:

\[
P_{\text{gate}} = P_{\text{charge}} + P_{\text{discharge}} = V_{\text{g}} I_{\text{g}} + \frac{1}{2} C_{\text{g}} V_{\text{g}}^2(10)
\]

Where, \(Q_g\) is the total gate charge of the external MOSFET and \(C_{\text{g}}\) is the gate charging the frequency. In case of a soft switching topology, \(Q_g\) is equal to gate to source charge \(Q_{gs}\) of the FET or IGBT. The total gate driving losses in high and low side drivers are then 4 times \(P_{\text{gate}}\) as:

\[
P_{\text{total}} = 4 P_{\text{gate}} = 4 \left( V_{\text{g}} I_{\text{g}} + \frac{1}{2} C_{\text{g}} V_{\text{g}}^2 \right)
\]

Since the major power loss is the gate driving losses, the simplest and fastest way to calculate the losses in a driver is to sum the gate driving loss \(P_{\text{gate}}\) and dynamic losses on \(V_{\text{g}}\).

These losses account for more than 90% in recent middle voltage class high and low side driver products.

**Thermal Analysis**

Once the power dissipated inside the driver is calculated, we can estimate the junction temperature of the driver. This can be evaluated assuming thermal resistance or characterization was determined for a similar thermal design (heat sinking and air flow). The thermal equation is:

\[
T_J = T_A + \frac{R_{thJA} P_{\text{diss}}}{\text{Tdp}}
\]

Where:

- \(T_J\) is the junction temperature of the device
- \(T_A\) is the ambient temperature
- \(R_{thJA}\) is the thermal resistance parameter
- \(P_{\text{diss}}\) is the total power dissipation
- \(\text{Tdp}\) is the temperature at point x as defined in the thermal characteristic table from datasheet.

The thermal information is shown in Figure 5 and Table 1.

**Characterization of the package**

The thermal characteristic of the package is a function of several parameters such as geometry, boundary condition, test condition, etc. This requires numerical analysis and/or modeling techniques that are generally cumbersome to manage. It can be tricky to estimate the junction temperature precisely with thermal information coming from data sheets.

So it is helpful to review the definition of thermal information.

1. \(T_J\) is the Junction-to-Air Thermal Resistance. It measures the heat flow between the die junction and the air. It is mainly relevant for packages used without any external heat sink.

2. \(T_J\) is the Junction-to-Case Thermal Resistance and it measures the heat flow between the die junction and the surface of the package. It is mainly relevant for packages using some external heat sinks.

3. \(T_J\) is the Junction-to-PKG Top Thermal Characterization parameter and it provides correlation between die temperature and temperature of package topside. This can be used to estimate die temperature in applications where the package topside is exposed to waste heat.

**Table 1. Definition of Thermal Resistance and Characterization Parameters**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{thJC})</td>
<td>Thermal resistance between (T_J) and (T_C)</td>
</tr>
<tr>
<td>(R_{thJA})</td>
<td>Thermal resistance between (T_J) and (T_A)</td>
</tr>
<tr>
<td>(R_{thCJA})</td>
<td>Thermal resistance between (T_C) and (T_A)</td>
</tr>
<tr>
<td>(T_{min})</td>
<td>Minimum temperature at (T_J)</td>
</tr>
<tr>
<td>(T_{max})</td>
<td>Maximum temperature at (T_J)</td>
</tr>
</tbody>
</table>

Generally, the thermal information provided in semiconductor datasheet can’t cover all applications cases. For the following examples we’ll only use \(R_{thJC}\) for \(T_J\) calculation.


**Recommendations to Reduce \(T_J\)**

In case \(T_J\) is too high, to the recommended operating temperature, there are few things that could be considered:

1. Add external gate resistors so that the power dissipation. When no external gate resistor is inserted between the driver and MOSFET, the power is entirely dissipated inside the driver package. Using external gate resistor allows to share the power.

2. Add heatsink to reduce the temperature. A heatsink is typically a large metal block that conducts heat away from the device to a surface at a lower temperature. Heatsinks are often made of aluminum, which has a high thermal conductivity and a low weight.

3. Add heat sinks to the package to dissipate the heat. Heat sinks are typically made of aluminum, which has a high thermal conductivity and a low weight.

4. Add heat sinks to the package to dissipate the heat. Heat sinks are typically made of aluminum, which has a high thermal conductivity and a low weight.
Tools and Generic Help
New landing page access

Website Link: onsemi Gate Drivers

Product Family

- **IGBT Drivers**: Drivers designed for high efficiency and reliability in high power applications.
- **MOSFET Drivers**: Drivers designed to drive low-side switching applications by providing high peak currents during the short switching interval.
- **Galvanic Isolated Drivers**: High performance drivers for high power automotive applications that include PTC heaters, traction inverters, high voltage DC-DC and other auxiliary subsystems.

Evaluation Boards

- **Gate Drivers Plug-and-Play Ecosystem**
- **NCP51705 Mini SMD Evaluation Board Manual**
- **NCP51530 Half Bridge Evaluation Board Manual**
## Nomenclature

**FAN 73 X XX X X X**

- **HVIC Family**
  - 73: 600–78: 100–200V

- **xFCS Product**

- **ID #**
  - 0~99: Normal
  - 0A~99A: Advanced

- **Sourcing/ Sinking Current Rating**
  - 6: Low current High side driver (H/S)
  - 7: High current High side driver (H/S)
  - 8: Low current Half-Bridge driver (H/S + L/S)
  - 9: High current Half-Bridge driver (H/S + L/S)

- **Package Type**
  - M: SOIC (SOP)
  - N: DIP
  - M1: Optional Package (Not available for new one)

- **Packing Type**
  - No suffix: Tube (Not available)
  - X: Tape & Reel

- **Package Option**
  - No suffix: Normal
  - 1~9: Option

**NCP/V 51 X Y Z**

- **ID in the family**
  - 0~4: Core
  - 5~9: Performance

- **Voltage**
  - 0: Low-side driver
  - 1: 100–200 V driver
  - 2: 600 V driver
  - 3: 700 V driver
  - 4: Above 700 V
  - 5: Isolated Single
  - 6: Isolated Dual

- **Driver Type**
  - 1: Single Low-side
  - 2: Dual Low-side
  - 3: All High-side
  - 4: Not used
  - 5: Single High & Low-side
  - 6: 3-ph High & Low-side
  - 7: SiC driver
  - 8: eGan driver

- **P**: Industrial
- **V**: Automotive
## High Voltage Gate Driver Products

<table>
<thead>
<tr>
<th>Type</th>
<th>Product</th>
<th>In - Out</th>
<th>Offset Voltage (V)</th>
<th>Output Current</th>
<th>Delay Time</th>
<th>Shut Down</th>
<th>OCP</th>
<th>DT/IL (ns)</th>
<th>PKG</th>
</tr>
</thead>
<tbody>
<tr>
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