

# QORVO

## SiC JFET Division

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## Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ( $R_{DS(on)}$ ), output capacitance ( $C_{oss}$ ), gate charge ( $Q_G$ ), and reverse recovery charge ( $Q_{rr}$ ) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

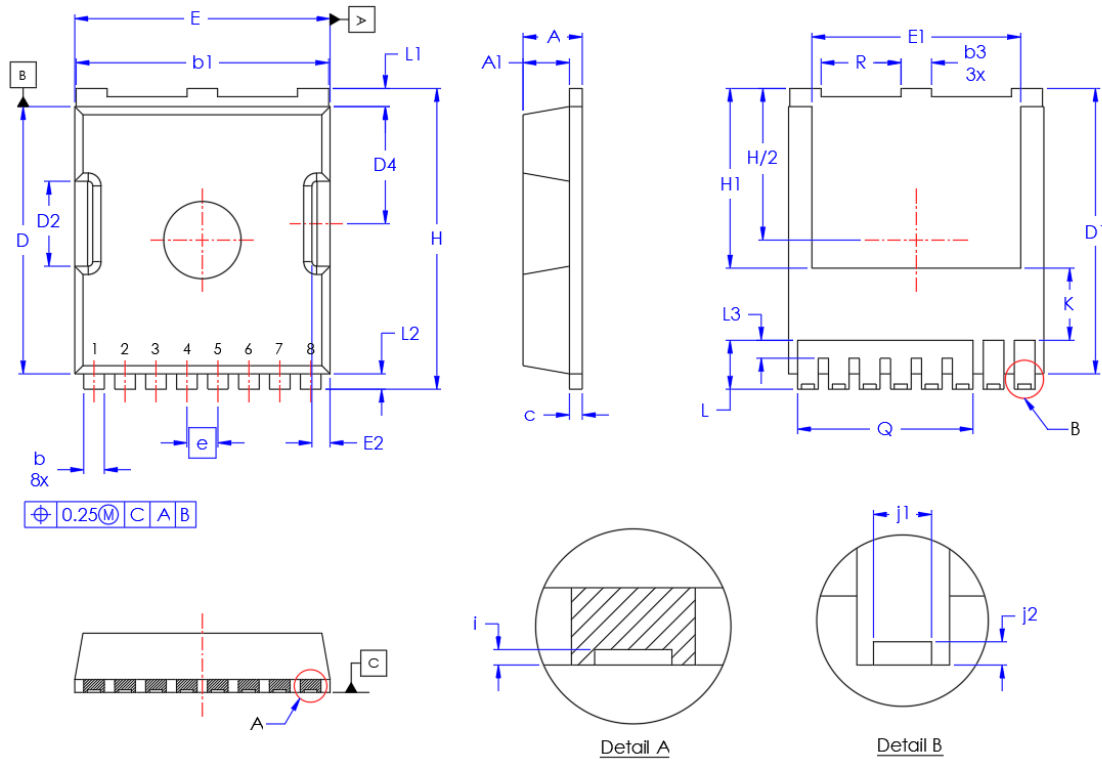
Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high  $dv/dt$  and  $di/dt$  rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see [www.unitedsic.com](http://www.unitedsic.com).

A snubber circuit with a small  $R_{(G)}$ , or gate resistor, provides better EMI suppression with higher efficiency compared to using a high  $R_{(G)}$  value. There is no extra gate delay time when using the snubber circuitry, and a small  $R_{(G)}$  will better control both the turn-off  $V_{(DS)}$  peak spike and ringing duration, while a high  $R_{(G)}$  will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high  $R_{(G)}$ , while greatly reducing  $E_{(OFF)}$  from mid-to-full load range with only a small increase in  $E_{(ON)}$ . Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at [www.unitedsic.com](http://www.unitedsic.com)

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**PACKAGE OUTLINE**



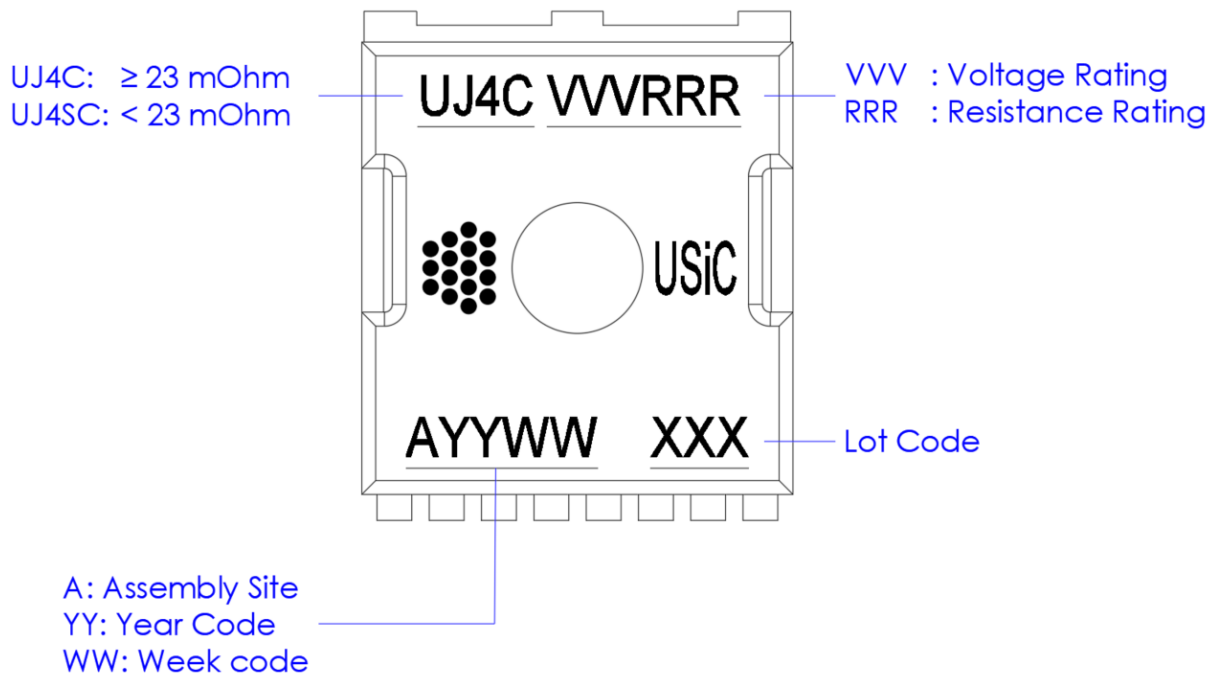
⊕ 0.25(M) C A B

SYMBOL	TO-LL Value	
	Min	Max
A	2.15	2.45
A1	1.80 REF	
b	0.65	0.90
b1	9.65	9.95
b3	1.10	1.30
c	0.40	0.60
D	10.18	10.58
D1	10.88	11.28
D2	3.15	3.45
D4	4.40	4.70
E	9.70	10.10
E1	7.95	8.25
E2	0.60	0.80
e	1.20 BSC	
H	11.48	11.88
H1	6.80	7.10
i	0.10 REF	
j1	0.46 REF	
j2	0.20 REF	
K	2.80 REF	
L	1.40	2.10
L1	0.50	0.90
L2	0.48	0.72
L3	0.30	0.80
Q	6.80 REF	
R	3.00	3.20

**Note:**

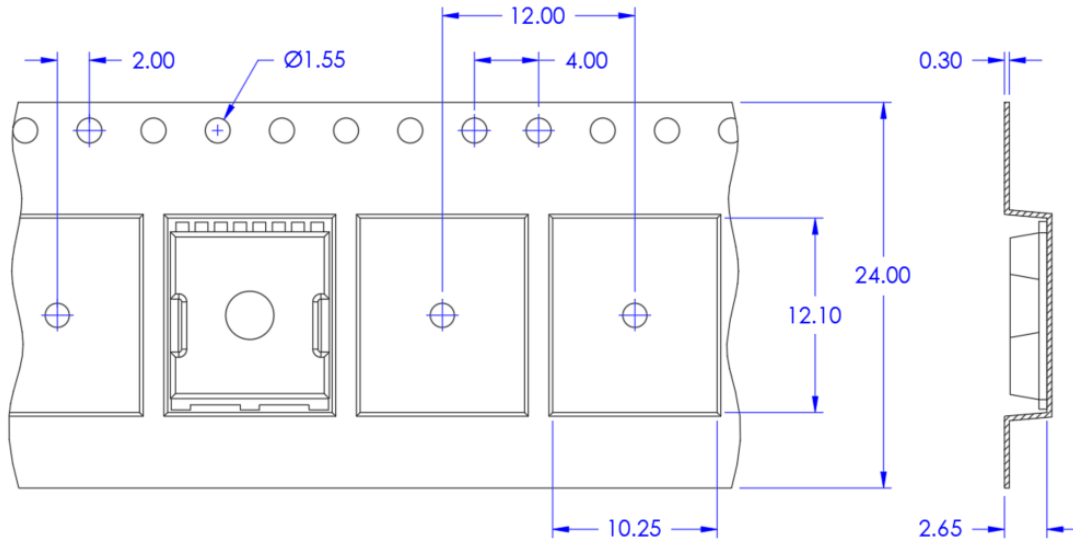
1. All dimensions in millimeters
2. Dimensions does not include Burrs and Mold Flashes

**PART MARKING**

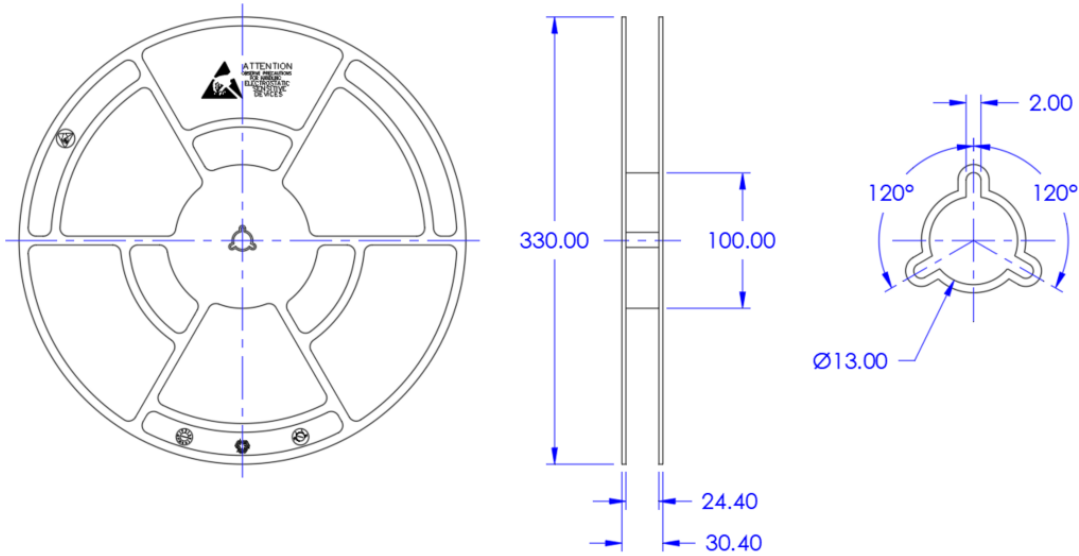


**PACKING TYPE**


*Carrier Tape*



*Reel*



All dimensions in millimeters  
Quantity per Reel: 2000 units

	TOLL PACKAGE OUTLINE, PART MARKING, TAPE AND REEL SPECIFICATION	Page 4 of 4
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**REVISION HISTORY**

Revision	Create Date (mm/dd/yyyy)	Description of Change	Initiator of Change
A	10/13/2023	Initial Production Release	Glenn Galang
B	01/31/2024	Corrected device orientation inside carrier tape pocket (Page 3)	Glenn Galang



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