

Silicon Carbide (SiC) JFET - EliteSiC, Power N-Channel, TOLL, 750V, 4 mohm

DATASHEET

UJ4N075004L8S

Rev. C, January 2025

Description

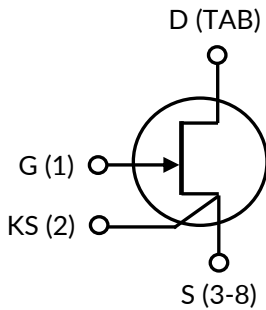
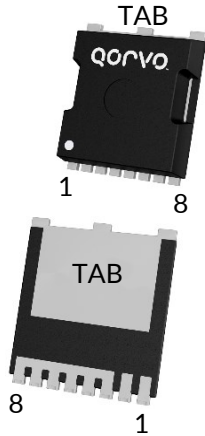
Qorvo's UJ4N075004L8S is a 750 V, 4.3mΩ high-performance Gen 4 normally-on SiC JFET transistor. This device exhibits ultra-low on resistance ($R_{DS(on)}$) in a compact TOLL package, making it an ideal fit to address the challenging thermal and space constraints of solid-state circuit breakers and relay applications. Additionally, the JFET is a robust device technology capable of the high-energy switching required in circuit protection applications.

Features

- ◆ Single digit on-resistance in a TOLL SMD package
- ◆ Operating temperature: 175°C (max)
- ◆ High pulse current capability
- ◆ Excellent device robustness
- ◆ Silver-sintered die attach for excellent thermal resistance
- ◆ Short circuit rated
- ◆ RoHS compliant

Typical applications

- ◆ Solid State / Semiconductor Circuit Breaker
- ◆ Solid State / Semiconductor Relay
- ◆ Battery Disconnects
- ◆ Surge Protection
- ◆ Inrush Current Control



Part Number	Package	Marking
UJ4N075004L8S	MO-229	UJ4N075004



Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
Gate-source voltage	V_{GS}	DC	-30 to +3	V
		AC ¹	-30 to +30	V
Continuous drain current ²	I_D	$T_C < 145^\circ\text{C}$	120	A
Pulsed drain current ³	I_{DM}	$T_C = 25^\circ\text{C}$	588	A
Short circuit withstand time	t_{SC}	$V_{DS} = 400\text{V}, T_{J(\text{START})} = 175^\circ\text{C}$	5	μs
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	1153	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Reflow soldering temperature	T_{solder}	reflow MSL 1	260	$^\circ\text{C}$

- +30V AC rating applies for turn-on pulses <200ns applied with external $R_G > 1\Omega$.
- Limited by bondwires
- Pulse width t_p limited by $T_{J,max}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.10	0.13	$^\circ\text{C}/\text{W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS} = -20\text{V}, I_D = 2\text{mA}$	750			V
Total drain leakage current	I_{DSS}	$V_{DS} = 750\text{V},$ $V_{GS} = -20\text{V}, T_J = 25^\circ\text{C}$		13	120	μA
		$V_{DS} = 750\text{V},$ $V_{GS} = -20\text{V}, T_J = 175^\circ\text{C}$		65		
Total gate leakage current	I_{GSS}	$V_{GS} = -20\text{V}, T_J = 25^\circ\text{C}$		0.1	100	μA
		$V_{GS} = -20\text{V}, T_J = 175^\circ\text{C}$		0.3		μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS} = 2\text{V}, I_D = 80\text{A},$ $T_J = 25^\circ\text{C}$		4.3		$\text{m}\Omega$
		$V_{GS} = 0\text{V}, I_D = 80\text{A},$ $T_J = 25^\circ\text{C}$		4.9	6.6	
		$V_{GS} = 2\text{V}, I_D = 80\text{A},$ $T_J = 175^\circ\text{C}$		9.9		
		$V_{GS} = 0\text{V}, I_D = 80\text{A},$ $T_J = 175^\circ\text{C}$		11.5		
Gate threshold voltage	$V_{G(th)}$	$V_{DS} = 5\text{V}, I_D = 180\text{mA}$	-8.3	-6.0	-3.7	V
Gate resistance	R_G	$f = 1\text{MHz}, \text{open drain}$		0.8		Ω

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	$V_{DS} = 400\text{V}, V_{GS} = -20\text{V}$ $f = 100\text{kHz}$		3028		pF
Output capacitance	C_{oss}			364		
Reverse transfer capacitance	C_{rss}			360		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS} = 0\text{V to } 400\text{V},$ $V_{GS} = -20\text{V}$		448		pF
C_{OSS} stored energy	E_{oss}	$V_{DS} = 400\text{V}, V_{GS} = -20\text{V}$		36		μJ
Total gate charge	Q_G	$V_{DS} = 400\text{V}, I_D = 80\text{A},$ $V_{GS} = -18\text{V to } 0\text{V}$		400		nC
Gate-drain charge	Q_{GD}			270		
Gate-source charge	Q_{GS}			60		

Typical Performance Diagrams

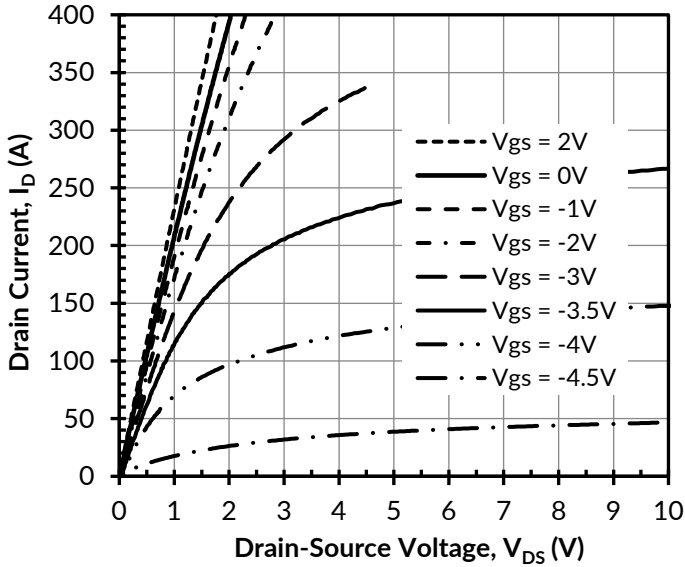


Figure 1. Typical output characteristics at $T_j = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

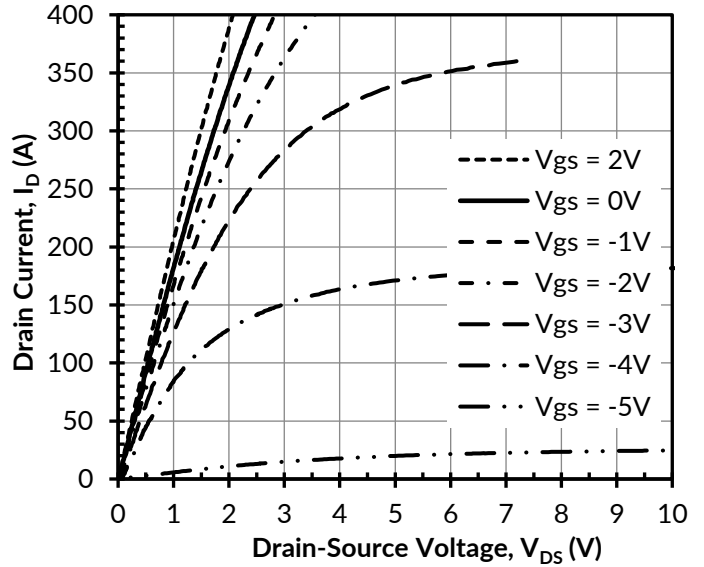


Figure 2. Typical output characteristics at $T_j = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

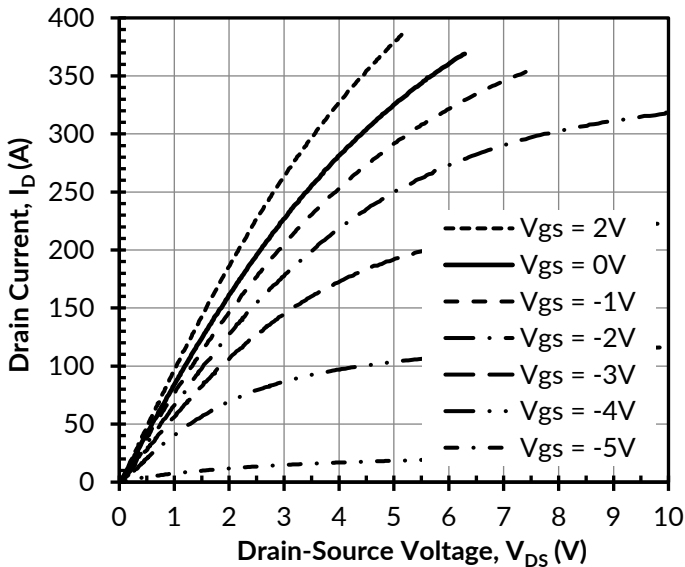


Figure 3. Typical output characteristics at $T_j = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

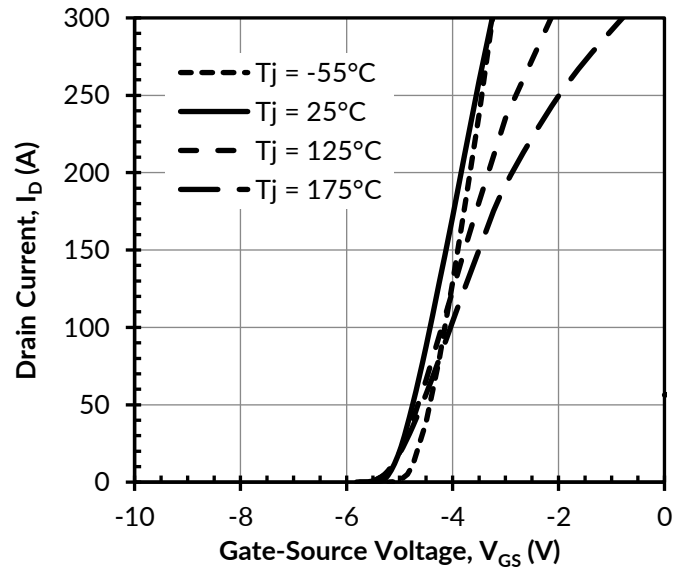


Figure 4. Typical transfer characteristics at $V_{DS} = 5\text{V}$

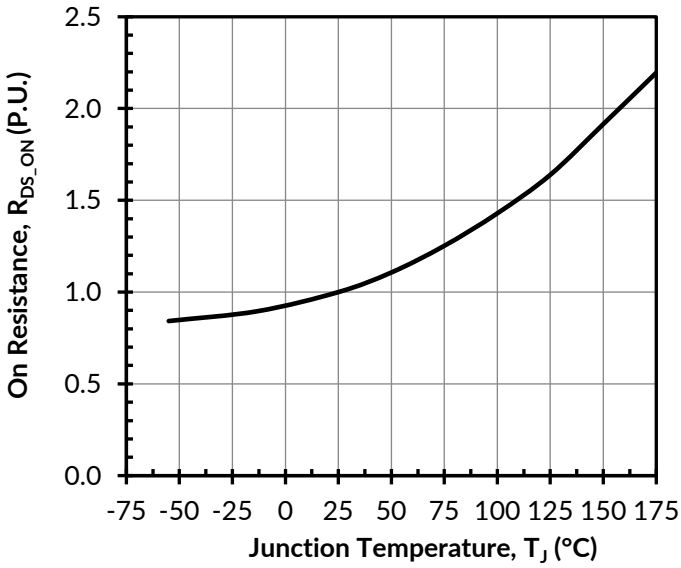


Figure 5. Normalized on-resistance vs. temperature at $V_{GS} = 0V$ and $I_D = 80A$

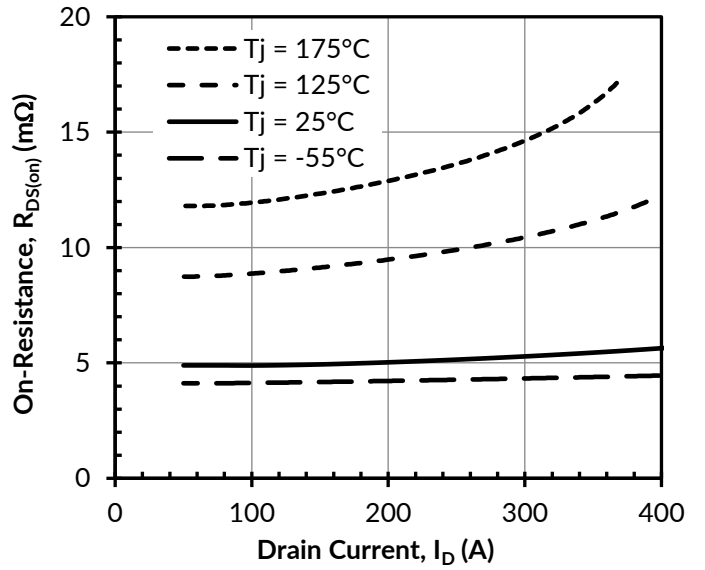


Figure 6. Typical drain-source on-resistances at $V_{GS} = 0V$

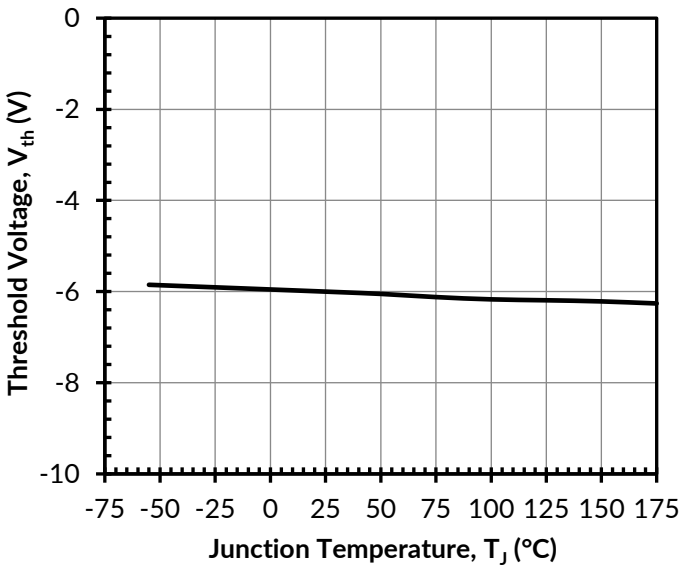


Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5V$ and $I_D = 180mA$

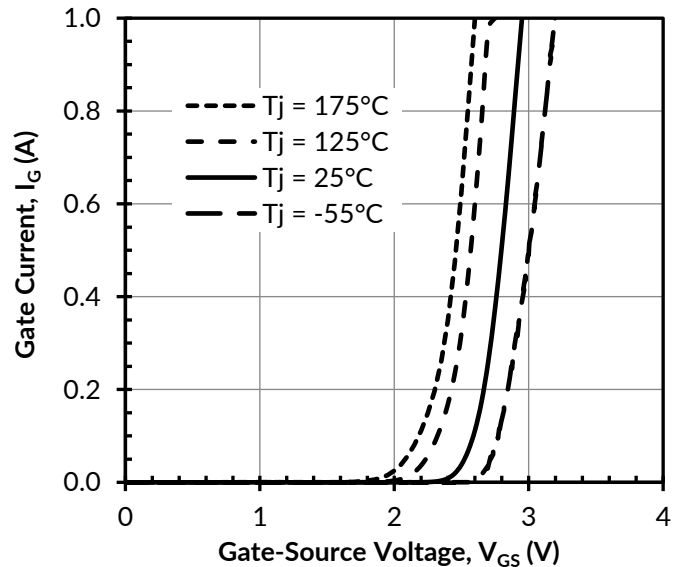


Figure 8. Typical gate forward current at $V_{DS} = 0V$

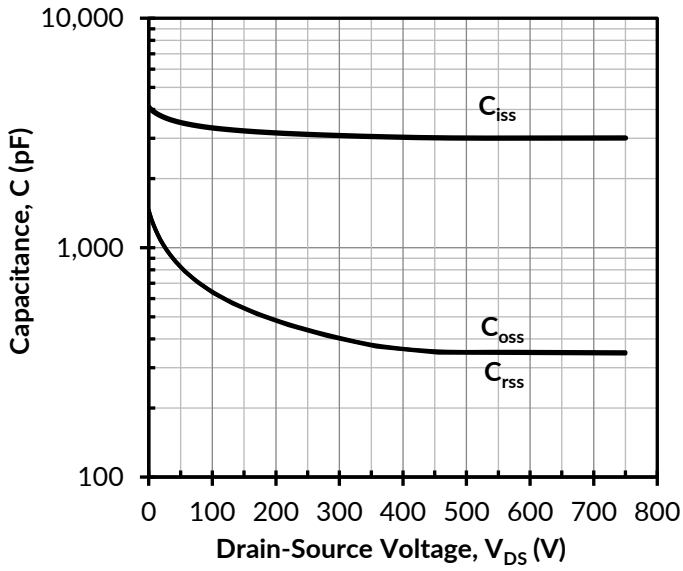


Figure 9. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = -20\text{V}$

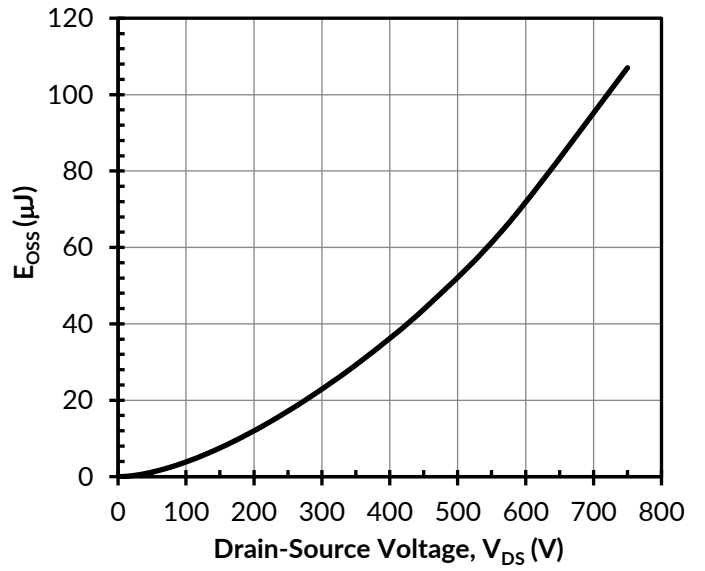


Figure 10. Typical stored energy in C_{OSS} at $V_{GS} = -20\text{V}$

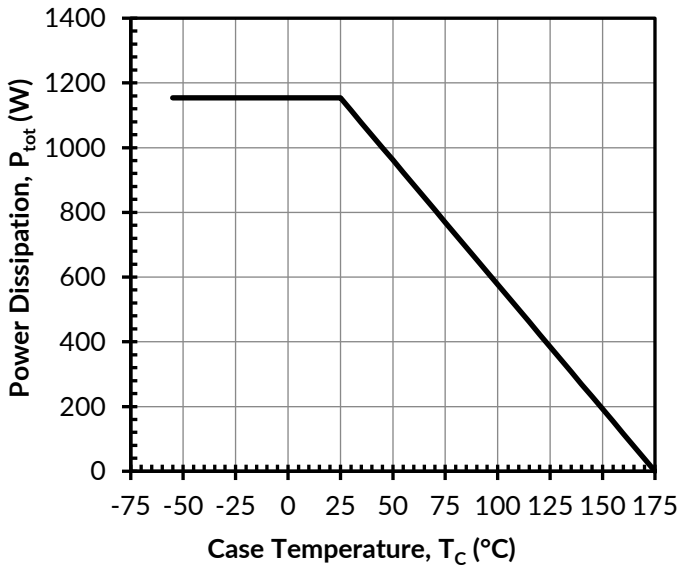


Figure 11. Total power Dissipation

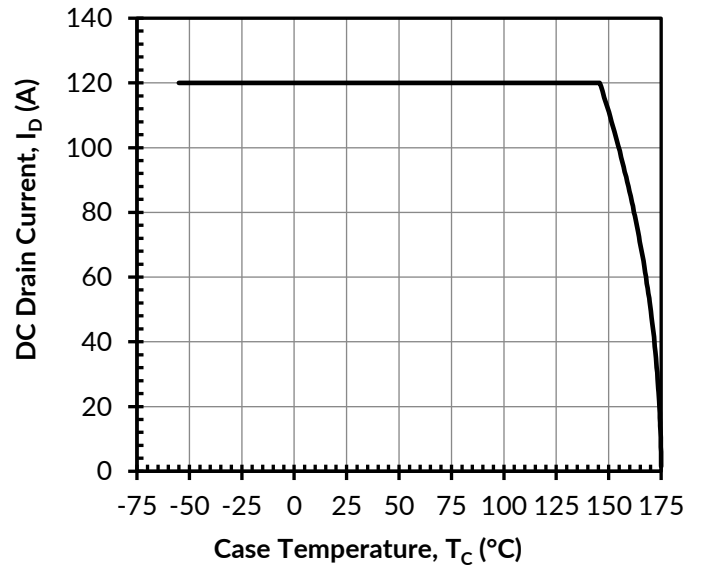


Figure 12. DC drain current derating

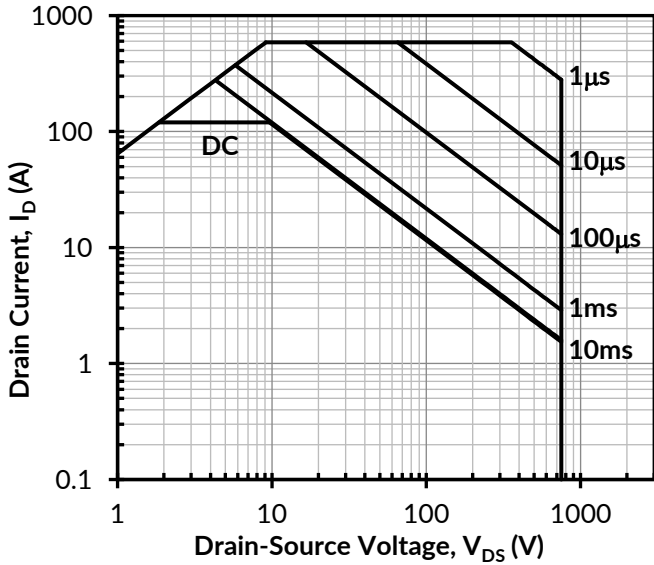


Figure 13. Safe operation area at $T_C = 25^\circ\text{C}$, Parameter t_p

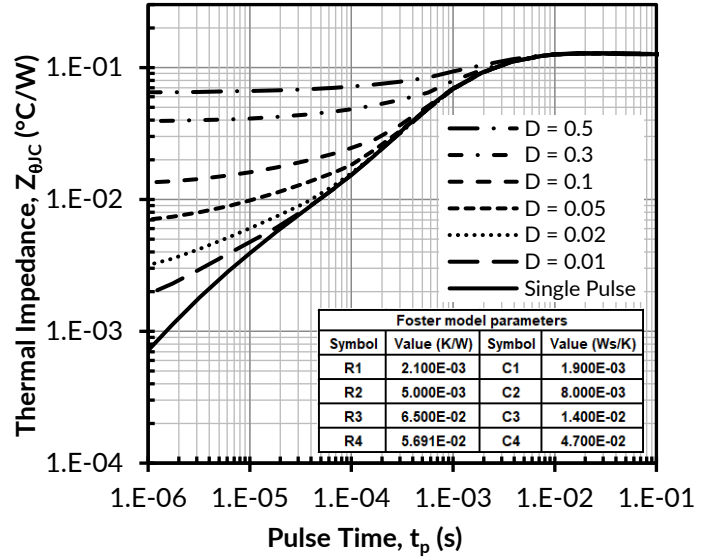


Figure 14. Maximum transient thermal impedance

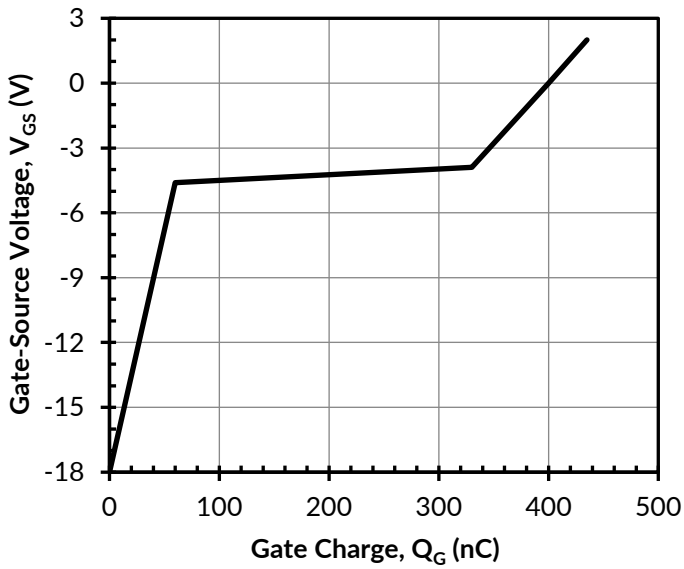
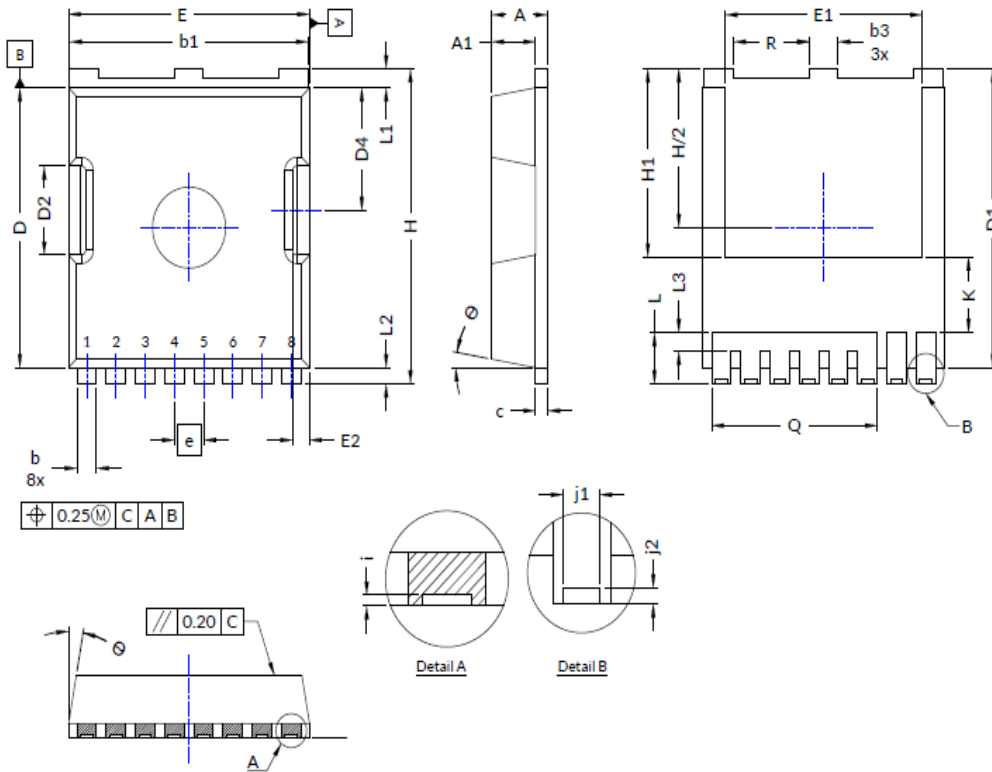


Figure 15. Typical gate charge at $V_{DS} = 400\text{V}$ and $I_D = 80\text{A}$

Package Outlines



SYMBOL	TO-LL		
	Min	Nom	Max
A	2.15	2.30	2.45
A1	1.80 REF		
b	0.70	0.80	0.90
b1	9.65	9.80	9.95
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	10.98	11.08	11.18
D2	3.15	3.30	3.45
D4	4.40	4.55	4.70
E	9.70	9.90	10.10
E1	7.95	8.10	8.25
E2	0.60	0.70	0.80
e	1.20 BSC		
H	11.48	11.68	11.88
H1	6.80	6.95	7.10
i	0.10 REF		
j1	0.46 REF		
j2	0.20 REF		
K	2.80 REF		
L	1.40	1.90	2.10
L1	0.50	0.70	0.90
L2	0.48	0.60	0.72
L3	0.30	0.70	0.80
Q	6.80 REF		
R	3.00	3.10	3.20
θ	10°		

Note:

1. All dimensions in millimeters
2. Dimensions does not include Burrs and Mold Flashes
3. Dimensions in compliance with JEDEC MO-299B except for backside heatsink exposed pad dimension, E1 and H1

Pin Designations:

- 1 : Gate
- 2 : Source Kelvin
- 3-8 : Source

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