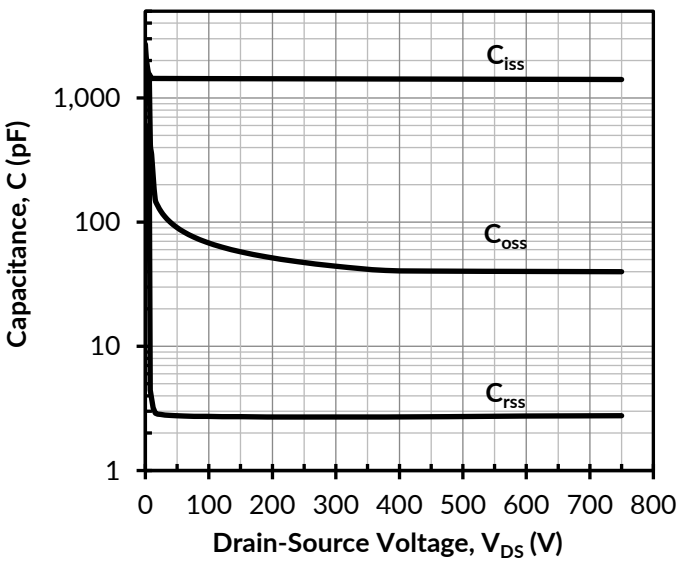


Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

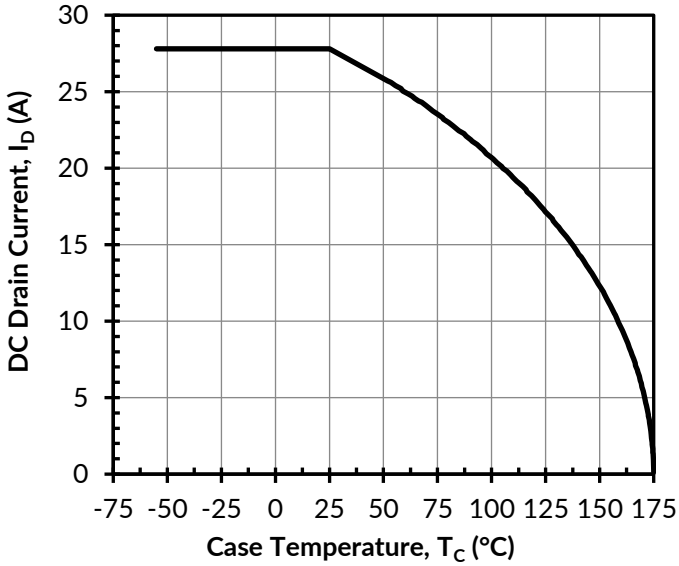


Figure 14. DC drain current derating

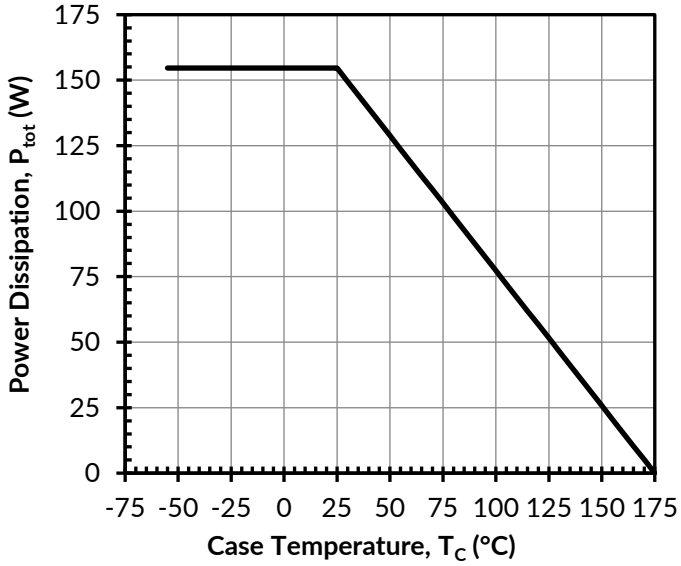


Figure 15. Total power dissipation

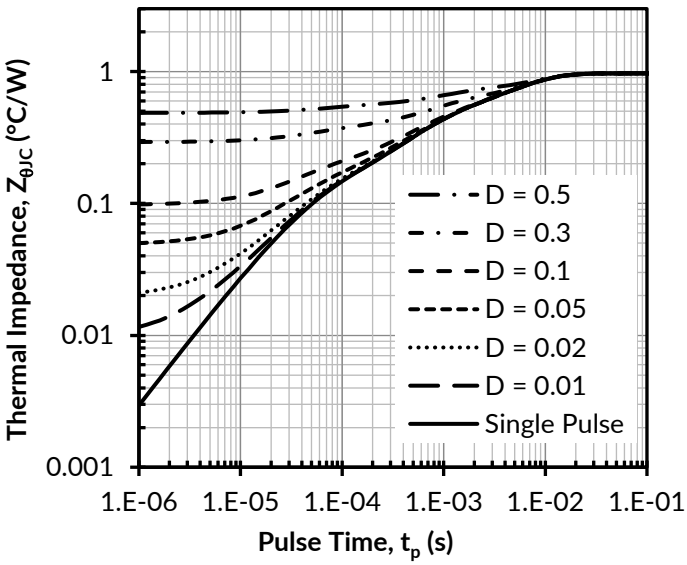


Figure 16. Maximum transient thermal impedance

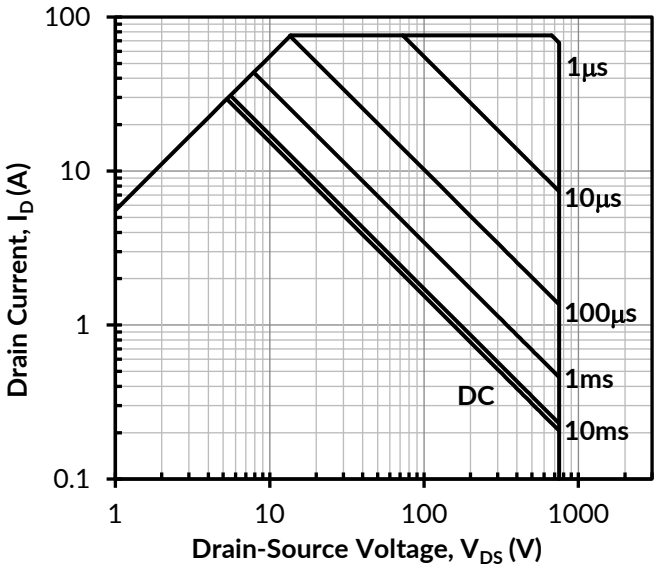


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

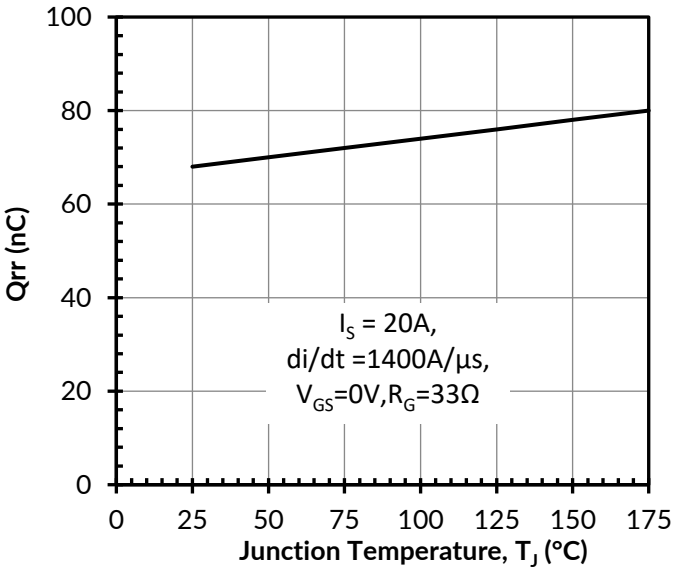


Figure 18. Reverse recovery charge Qrr vs. junction temperature at V_{DS} = 400V

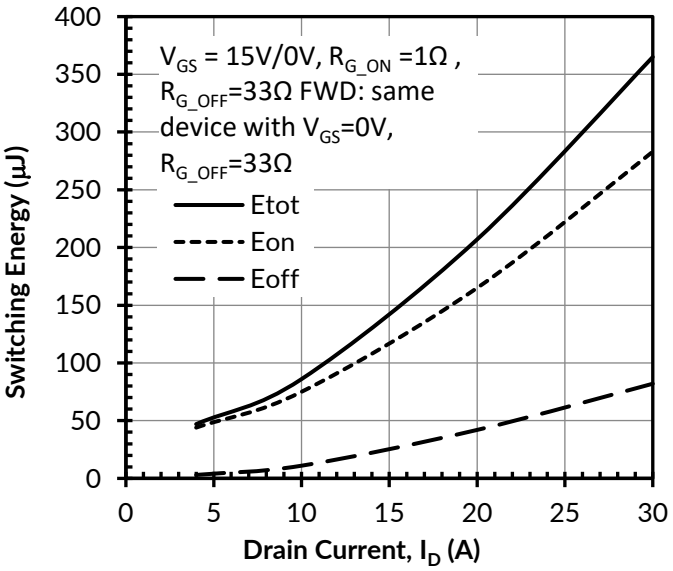


Figure 19. Clamped inductive switching energy vs. drain current at V_{DS} = 400V and T_J = 25°C

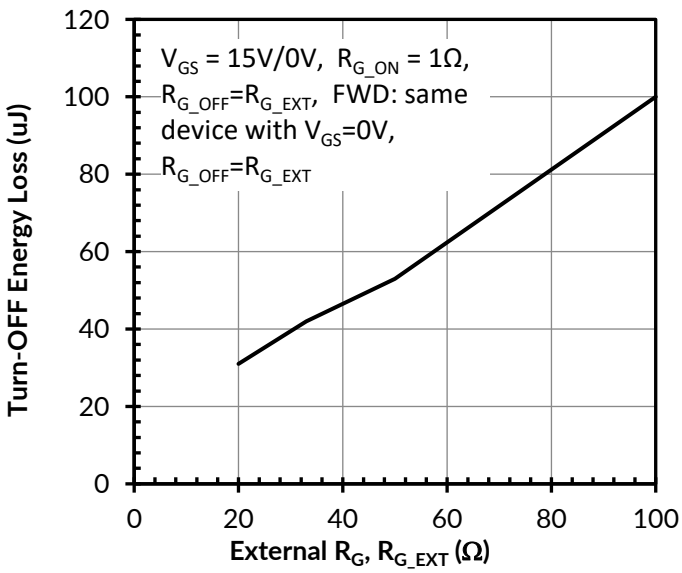


Figure 20. Clamped inductive switching turn-off energy vs. R_{G,EXT_OFF}

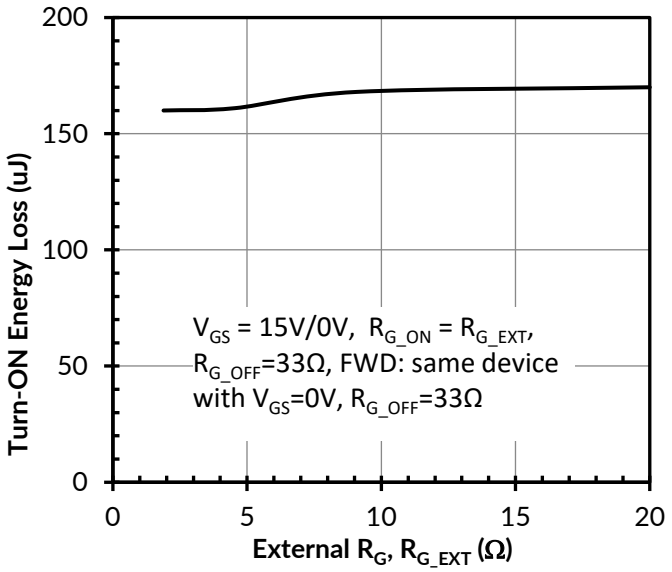


Figure 21. Clamped inductive switching turn-off energy vs. R_{G,EXT_ON}

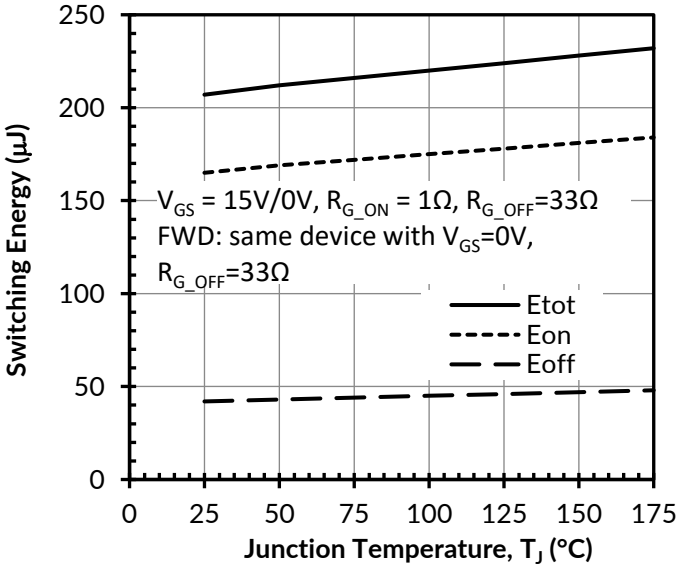


Figure 22. Clamped inductive switching energy vs. junction temperature at V_{DS} = 400V and I_D = 20A

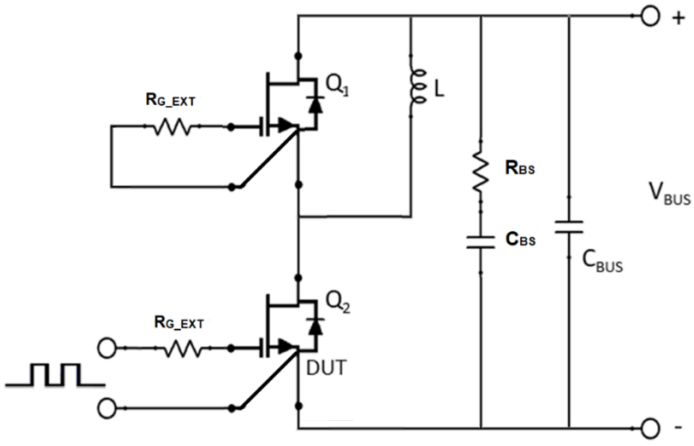


Figure 23. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber (R_{BS} = 2.5Ω, C_{BS}=100nF) is used to reduce the power loop high frequency oscillations.

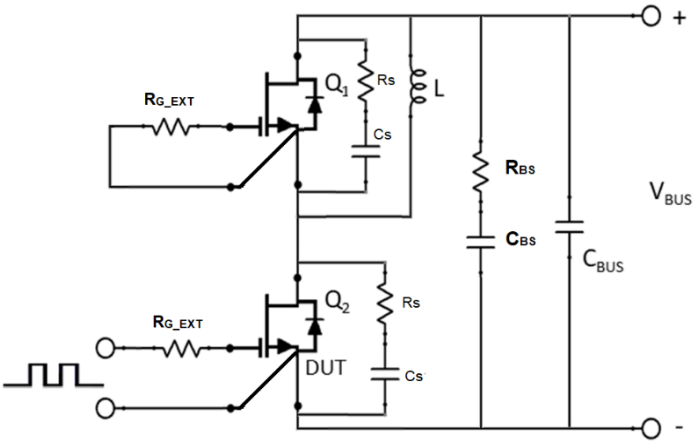
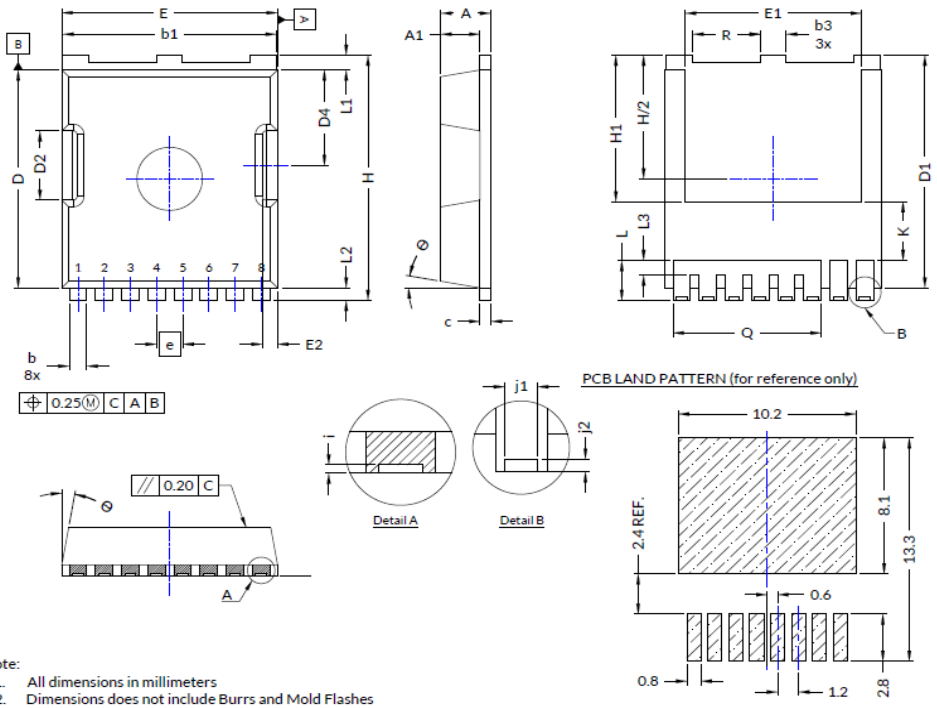


Figure 24. Schematic of the half-bridge mode switching test circuit with device RC snubbers (R_s =10Ω, C_s = 100pF) and a bus RC snubber (R_{BS} = 2.5Ω, C_{BS}=100nF).

Package Outlines



SYMBOL	TO-LL		
	Value		
	Min	Nom	Max
A	2.15	2.30	2.45
A1		1.80 REF	
b	0.70	0.80	0.90
b1	9.65	9.80	9.95
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	10.98	11.08	11.18
D2	3.15	3.30	3.45
D4	4.40	4.55	4.70
E	9.70	9.90	10.10
E1	7.95	8.10	8.25
E2	0.60	0.70	0.80
e		1.20 BSC	
H	11.48	11.68	11.88
H1	6.80	6.95	7.10
i		0.10 REF	
j1		0.46 REF	
j2		0.20 REF	
K		2.80 REF	
L	1.40	1.90	2.10
L1	0.50	0.70	0.90
L2	0.48	0.60	0.72
L3	0.30	0.70	0.80
Q		6.80 REF	
R	3.00	3.10	3.20
θ		10°	

Note:
1. All dimensions in millimeters
2. Dimensions does not include Burrs and Mold Flashes
3. Dimensions in compliance with JEDEC MO-299B except for backside heatsink exposed pad dimension, E1 and H1

Pin Designations:
1 : Gate
2 : Source Kelvin
3-8 : Source

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see https://www.qorvo.com/design-hub.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at https://www.qorvo.com/design-hub.

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