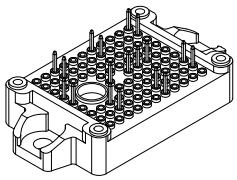
Silicon Carbide (SiC) Cascode JFET Module – EliteSiC, Half-Bridge Module, 1200 V, 19 mohm

UHB50SC12E1BC3N



PIM18 33.80x42.50x12.00 E1B
HALF BRIDGE (SOLDER PIN)
CASE 180DE

Description

This SiC FET device is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's silicon-like gate-drive characteristics allows the use of unipolar gate drives, compatible with Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the E1B module package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive. Advanced Ag sintering die attach technology gives the module superior thermal performance.

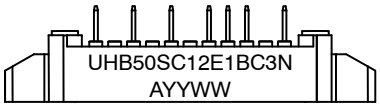
Features

- On-resistance $R_{DS(on)}$: 19 mΩ (Typ)
- Operating Temperature: 150 °C (Max)
- Excellent Reverse Recovery: Q_{rr} = 495 nC
- Low Body Diode Voltage :V_{FSD} = 1.2 V
- Low Gate Charge: Q_G = 85 nC
- Threshold Voltage $V_{G(th)}$: 5 V (Typ) Allowing 0 to 15 V Drive
- Low Intrinsic Capacitance
- ESD Protected: HBM Class 2 and CDM Class C3
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

Typical Applications

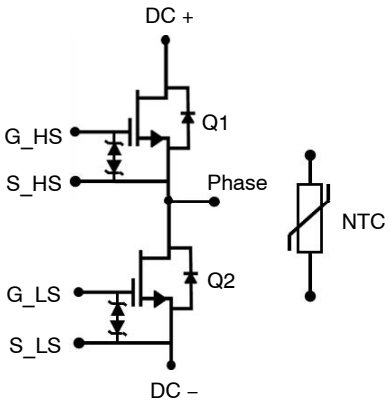
- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating

MARKING DIAGRAM



UHB50SC12E1BC3N	= Specific Device Code
A	= Assembly Location
YY	= Year
WW	= Work Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		1200	V
Gate-source Voltage	V_{GS}	DC	−20 to +20	V
		AC (f > 1 Hz)	−25 to +25	
Continuous Drain Current (Note 1)	I_D	T_C = 25 °C	69	A
		T_C = 85 °C	50	A
Pulsed Drain Current (Note 2)	I_{DM}	T_C = 25 °C	350	A
Power Dissipation per Switch	P_{tot}	T_C = 25 °C	208	W
Maximum Junction Temperature	$T_{J,max}$		150	°C
Operating and Storage Temperature	T_J, T_{STG}		−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by $T_{J, max}$
2. Pulse width t_p limited by $T_{J,max}$

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		–	0.46	0.6	°C/W

NTC THERMISTOR CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Rated Resistance	R_{25}	T_{NTC} = 25 °C	–	5	–	kΩ
Resistance Value Tolerance	ΔR/R	T_{NTC} = 25 °C	−5	–	5	%
Power Dissipation	P_{25}	T_{NTC} = 25 °C	–	–	20	mW
B Constant	$B_{25/50}$	$R_2 = R_{25} \exp [B_{25/50} (1/T_2 - 1/(298.15\ K))]$	–	3375	–	K

MODULE

Parameter	Symbol	Test Conditions	Value	Unit
Isolation Voltage	V_{ISOL}	RMS, f = 50 Hz, t = 1 min	3	kV
Internal Isolation			Al_2O_3	
Creepage Distance		Terminal to heatsink	12.7	mm
		Terminal to terminal	6.3	
Clearance Distance		Terminal to heatsink	10	mm
		Terminal to terminal	5	
Stray Inductance Module	L_{sCE}		11	nH

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC						
Drain-source Breakdown Voltage	BV_{DS}	V_{GS} = 0 V, I_D = 4 mA	1200	–	–	V
Total Drain Leakage Current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V, T_J = 25 °C	–	16	300	μA
		V_{DS} = 1200 V, V_{GS} = 0 V, T_J = 150 °C	–	50	–	
Total Gate Leakage Current	I_{GSS}	V_{DS} = 0 V, T_J = 25 °C, V_{GS} = −20 V / +20 V	–	12	40	μA
Drain-source On-resistance	$R_{DS(on)}$	V_{GS} = 12 V, I_D = 50 A, T_J = 25 °C	–	19	24	mΩ
		V_{GS} = 12 V, I_D = 50 A, T_J = 125 °C	–	30	–	
		V_{GS} = 12 V, I_D = 50 A, T_J = 150 °C	–	35	–	
Gate Threshold Voltage	$V_{G(th)}$	V_{DS} = 5 V, I_D = 20 mA	4	5	6	V
Gate Resistance	R_G	f = 1 MHz, open drain	–	2.2	–	Ω
TYPICAL PERFORMANCE – REVERSE DIODE						
Diode Continuous Forward Current (Note 1)	I_S	T_C = 25 °C	–	–	69	A
Diode Pulse Current (Note 2)	$I_{S,pulse}$	T_C = 25 °C	–	–	350	A
Forward Voltage	V_{FSD}	V_{GS} = 0 V, I_S = 25 A, T_J = 25 °C	–	1.2	1.4	V
		V_{GS} = 0 V, I_S = 25 A, T_J = 150 °C	–	1.4	–	
Reverse Recovery Charge	Q_{rr}	V_{DS} = 800 V, I_S = 50 A, V_{GS} = −5 V, R_{G_EXT} = 20 Ω, di/dt = 4000 A/μs, T_J = 25 °C	–	495	–	nC
Reverse Recovery Time	t_{rr}		–	21	–	ns
Reverse Recovery Charge	Q_{rr}	V_{DS} = 800 V, I_S = 50 A, V_{GS} = −5 V, R_{G_EXT} = 20 Ω, di/dt = 4000 A/μs, T_J = 150 °C	–	465	–	nC
Reverse Recovery Time	t_{rr}		–	22	–	ns
TYPICAL PERFORMANCE – DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz	–	2930	–	pF
Output Capacitance	C_{oss}		–	187	–	
Reverse Transfer Capacitance	C_{rss}		–	3.3	–	
Effective Output Capacitance, Energy Related	$C_{oss(er)}$	V_{DS} = 0 V to 800 V, V_{GS} = 0 V	–	240	–	pF
Effective Output Capacitance, Time Related	$C_{oss(tr)}$		–	533	–	
C_{OSS} Stored Energy	E_{oss}	V_{DS} = 800 V, V_{GS} = 0 V	–	77	–	μJ
Total gate Charge	Q_G	V_{DS} = 800 V, I_D = 50 A, V_{GS} = −5 V to 15 V	–	85	–	nC
Gate-drain Charge	Q_{GD}		–	19	–	
Gate-source Charge	Q_{GS}		–	31	–	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 800 V, I_D = 50 A, Gate Driver = −5 V to +15 V, R_{G_EXT} = 10 Ω, Inductive Load, FWD: same device with V_{GS} = −5 V, and R_{G_EXT} = 10 Ω, T_J = 25 °C (Notes 3, 4)	–	22	–	ns
Rise Time	t_r		–	18	–	
Turn-off Delay Time	$t_{d(off)}$		–	65	–	
Fall Time	t_f		–	10	–	
Turn-on Energy	E_{ON}		–	843	–	μJ
Turn-off Energy	E_{OFF}		–	139	–	
Total Switching Energy	E_{TOTAL}		–	982	–	

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – DYNAMIC						
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 800 V, I_D = 50 A, Gate Driver = −5 V to +15 V, R_{G_EXT} = 10 Ω, Inductive Load, FWD: same device with V_{GS} = −5 V, and R_{G_EXT} = 10 Ω, T_J = 150 °C (Notes 3, 4)	–	22	–	ns
Rise Time	t_r		–	16	–	
Turn-off Delay Time	$t_{d(off)}$		–	67	–	
Fall Time	t_f		–	12	–	
Turn-on Energy	E_{ON}		–	805	–	μJ
Turn-off Energy	E_{OFF}		–	125	–	
Total Switching Energy	E_{TOTAL}		–	930	–	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 800 V, I_D = 50 A, Gate Driver = −5 V to +15 V, Turn-on $R_{G,EXT}$ = 2 Ω, Turn-off $R_{G,EXT}$ = 2 Ω, Inductive Load, FWD: same device with V_{GS} = −5 V and R_G = 2 Ω, RC snubber: R_S = 5 Ω and C_S = 150 pF, T_J = 25 °C (Notes 5, 6)	–	32	–	ns
Rise Time	t_r		–	24	–	
Turn-off Delay Time	$t_{d(off)}$		–	40	–	
Fall Time	t_f		–	20	–	
Turn-on Energy Including R_S Energy	E_{ON}		–	738	–	μJ
Turn-off Energy Including R_S Energy	E_{OFF}		–	260	–	
Total Switching Energy	E_{TOTAL}		–	998	–	
Snubber R_S Energy During Turn-on	E_{RS_ON}		–	10	–	
Snubber R_S Energy During Turn-off	E_{RS_OFF}		–	5	–	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 800 V, I_D = 50 A, Gate Driver = −5 V to +15 V, Turn-on $R_{G,EXT}$ = 2 Ω, Turn-off $R_{G,EXT}$ = 2 Ω, Inductive Load, FWD: same device with V_{GS} = −5 V and R_G = 2 Ω, RC snubber: R_S = 5 Ω and C_S = 150 pF, T_J = 150 °C (Notes 5, 6)	–	30	–	ns
Rise Time	t_r		–	21	–	
Turn-off Delay Time	$t_{d(off)}$		–	41	–	
Fall Time	t_f		–	19	–	
Turn-on Energy Including R_S Energy	E_{ON}		–	655	–	μJ
Turn-off Energy Including R_S Energy	E_{OFF}		–	263	–	
Total Switching Energy	E_{TOTAL}		–	918	–	
Snubber R_S Energy During Turn-on	E_{RS_ON}		–	11	–	
Snubber R_S Energy During Turn-off	E_{RS_OFF}		–	5.5	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Measured with the half-bridge mode switching test circuit in Figure 23.
4. A bus RC snubber (R_{BS} = 2.5 Ω, C_{BS} = 200 nF) must be applied to reduce the power loop high frequency oscillations.
5. Measured with the half−bridge mode switching test circuit in Figure 24.
6. In this table, the switching energies (turn−on energy, turn−off energy and total energy) presented include the device RC snubber energy losses.

SiC FET TYPICAL PERFORMANCE DIAGRAMS

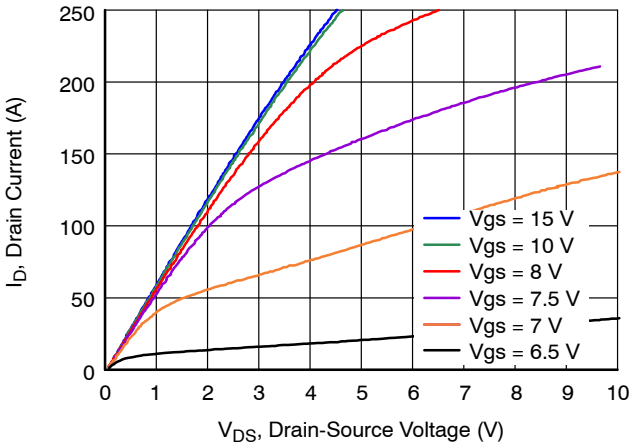


Figure 1. Typical Output Characteristics at T_J = −55 °C, t_p < 250 μs

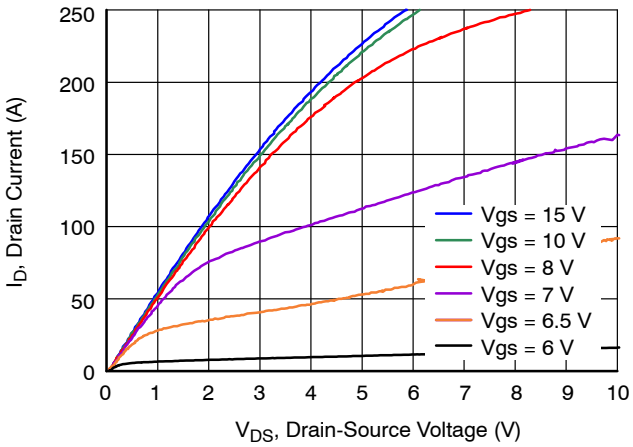


Figure 2. Typical Output Characteristics at T_J = 25 °C, t_p < 250 μs

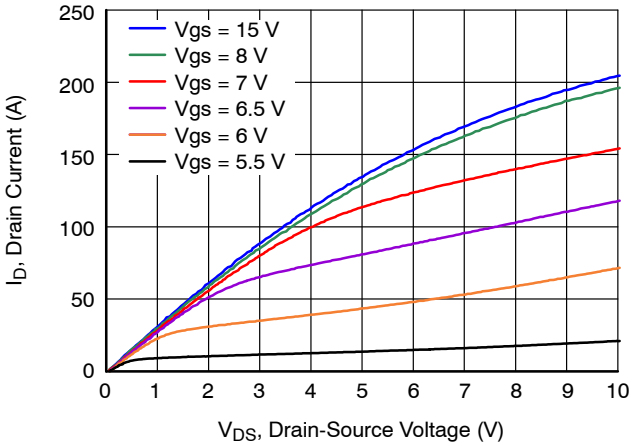


Figure 3. Typical Output Characteristics at T_J = 150 °C, t_p < 250 μs

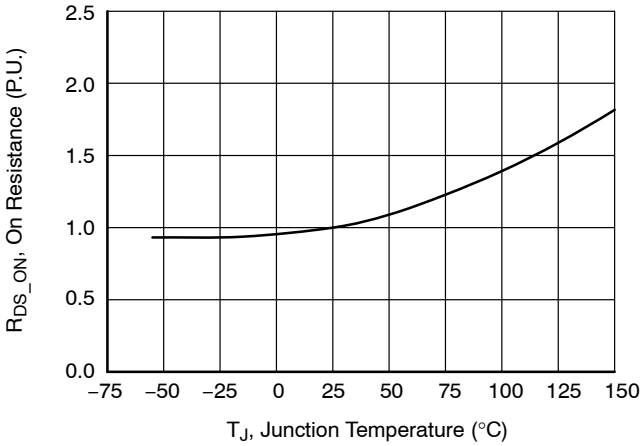


Figure 4. Normalized On-Resistance vs. Temperature at V_{GS} = 12 V and I_D = 50 A

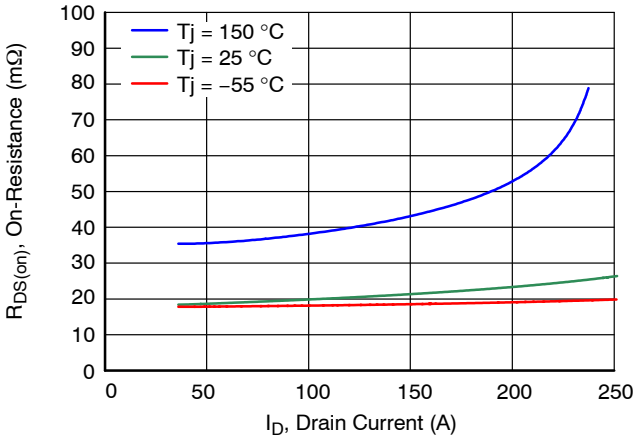


Figure 5. Typical Drain-Source On-Resistances at V_{GS} = 12 V

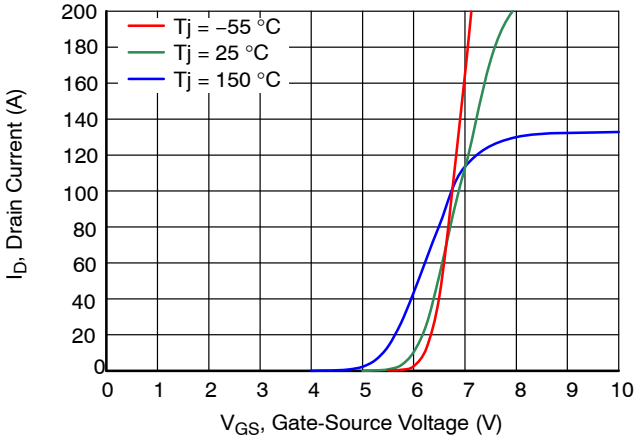


Figure 6. Typical Transfer Characteristics at V_{DS} = 5 V

SiC FET TYPICAL PERFORMANCE DIAGRAMS (continued)

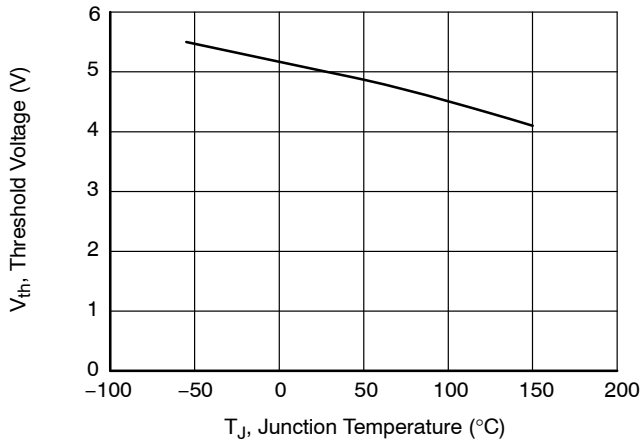


Figure 7. Threshold Voltage vs. Junction Temperature at V_{DS} = 5 V and I_D = 20 mA

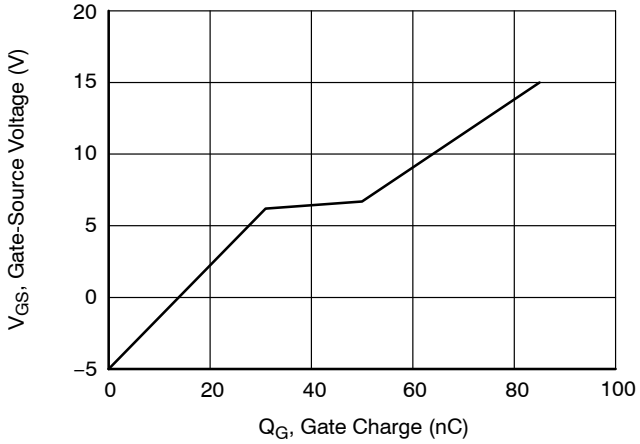


Figure 8. Typical Gate Charge at V_{DS} = 800 V and I_D = 50 A

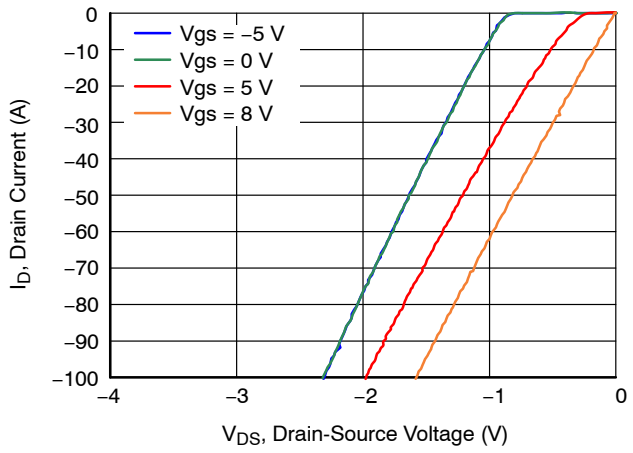


Figure 9. 3rd Quadrant Characteristics at T_J = −55 °C

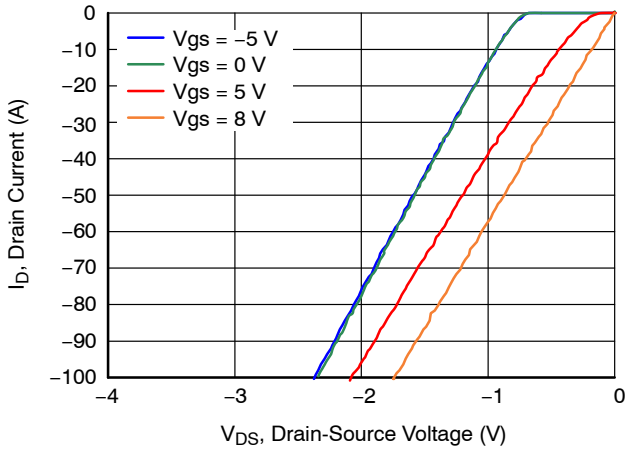


Figure 10. 3rd Quadrant Characteristics at T_J = 25 °C

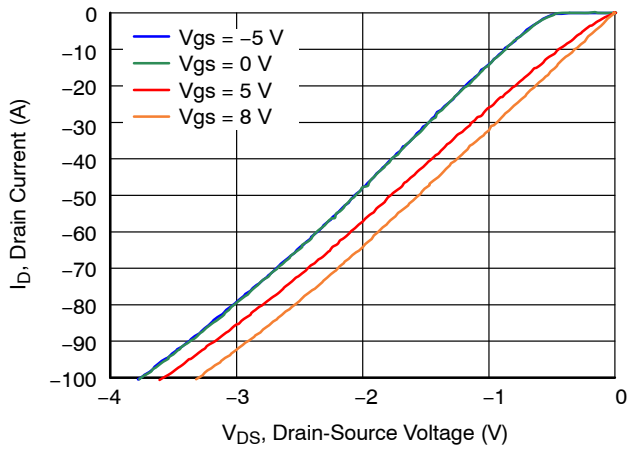


Figure 11. 3rd Quadrant Characteristics at T_J = 150 °C

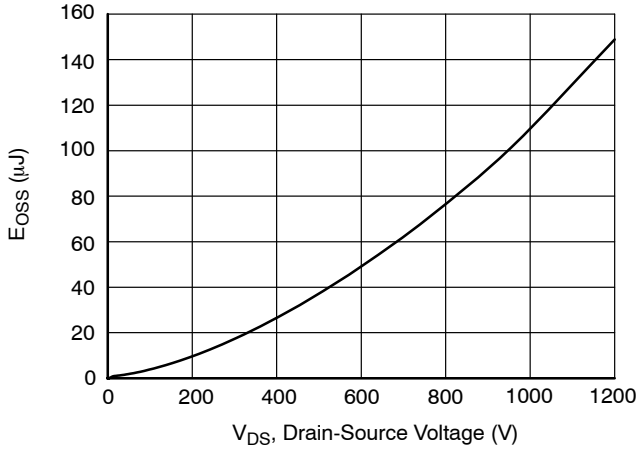


Figure 12. Typical Stored Energy in C_{OSS} at V_{GS} = 0 V

SiC FET TYPICAL PERFORMANCE DIAGRAMS (continued)

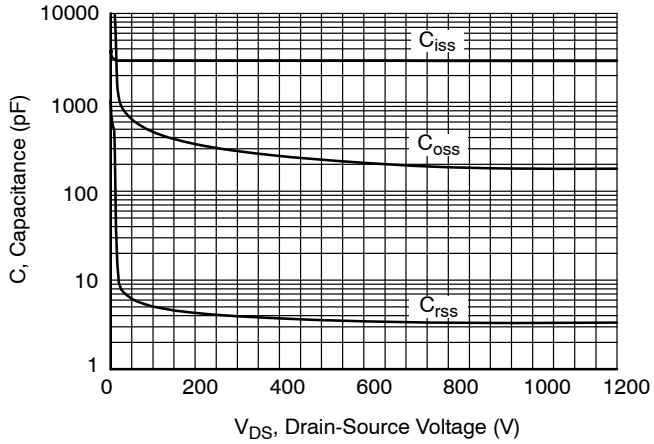


Figure 13. Typical Capacitances at f = 100 kHz and V_{GS} = 0 V

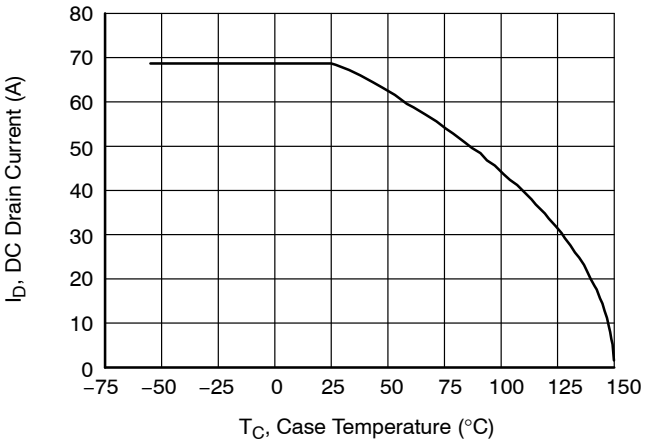


Figure 14. DC Drain Current Derating

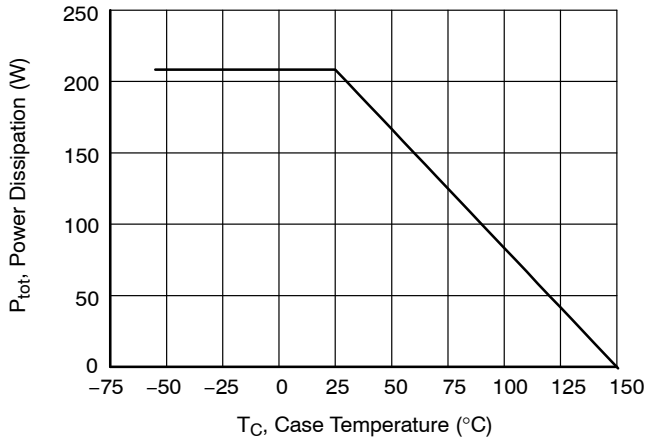


Figure 15. Total Power Dissipation

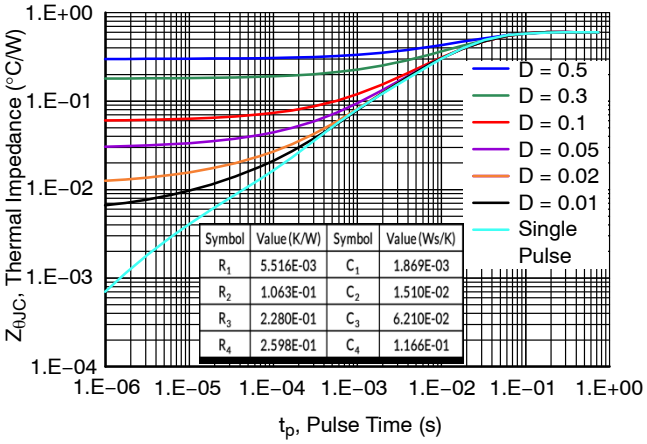


Figure 16. Maximum Transient Thermal Impedance and Parameters for Thermal Equivalent Circuit (Foster) Model

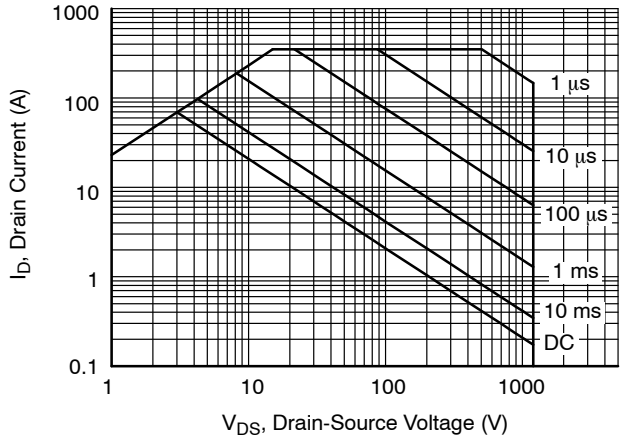


Figure 17. Safe Operation Area at T_C = 25 °C, D = 0, Parameter t_p

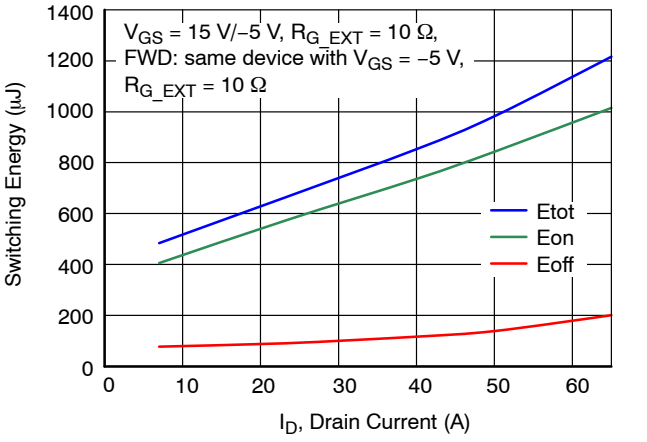


Figure 18. Clamped Inductive Switching Energy vs. Drain Current at V_{DS} = 800 V T_J = 25 °C

SiC FET TYPICAL PERFORMANCE DIAGRAMS (continued)

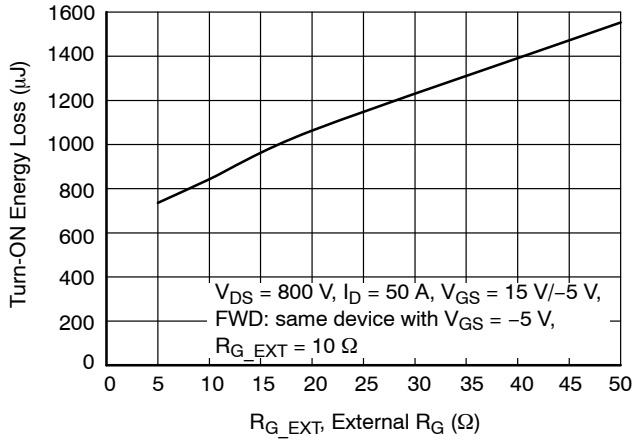


Figure 19. Clamped Inductive Switching Turn-On Energy vs. Turn-On Gate Resistance R_G

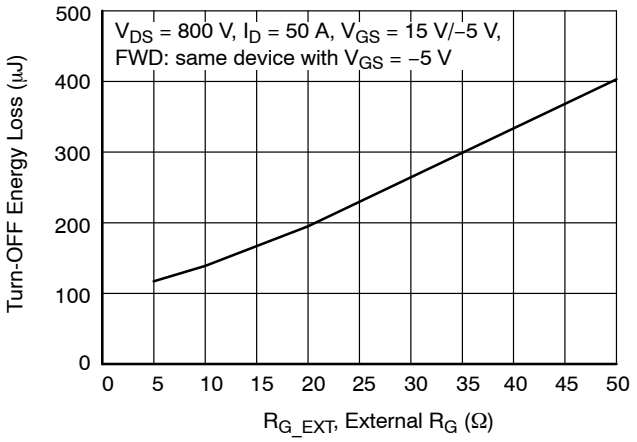


Figure 20. Clamped Inductive Switching Turn-Off Energy vs. Turn-Off Gate Resistance R_G

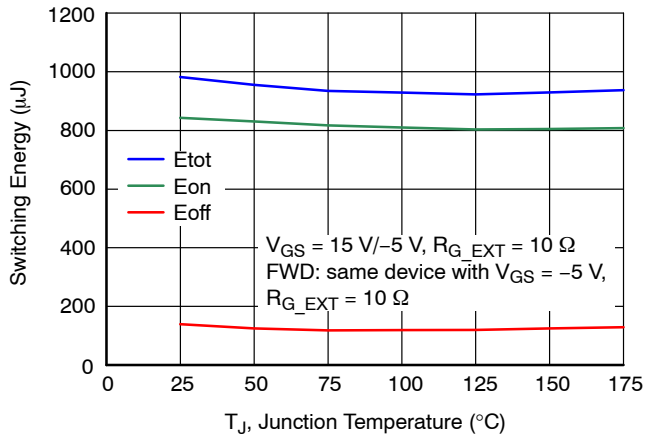


Figure 21. Clamped Inductive Switching Energy vs. Junction Temperature at V_{DS} = 800 V and I_D = 50 A

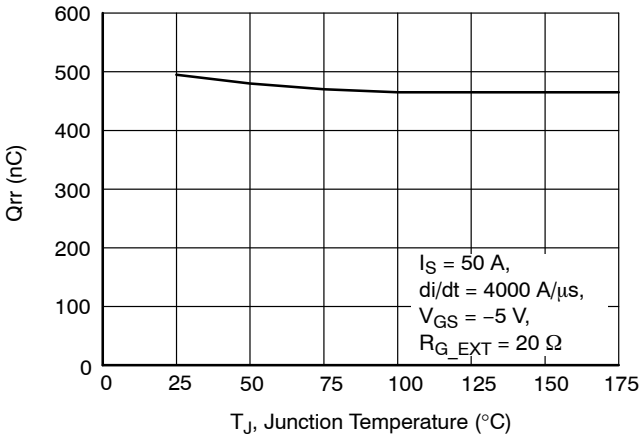


Figure 22. Reverse Recovery Charge Qrr vs. Junction Temperature at V_{DS} = 800 V

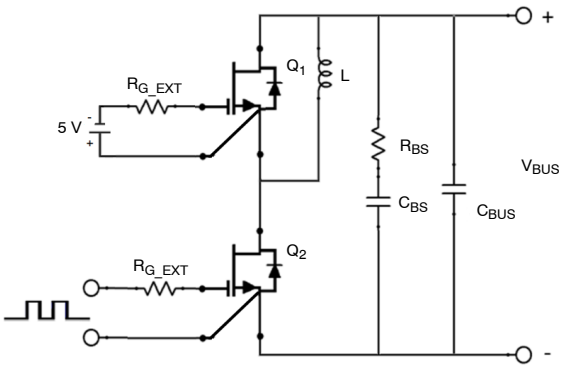


Figure 23. Schematic of the Half−bridge Mode Switching Test Circuit. Note, a Bus RC Snubber (R_{BS} = 2.5 Ω, C_{BS} = 100 nF) Must be Applied to Reduce the Power Loop High Frequency Oscillations

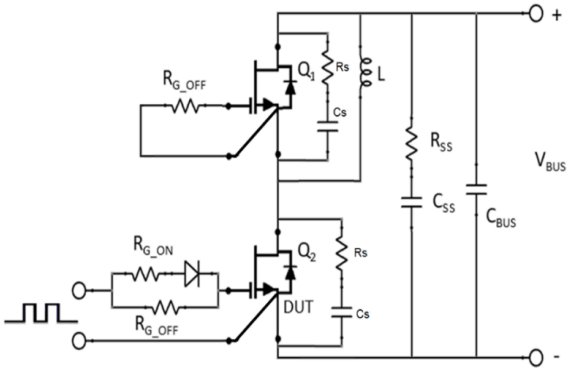


Figure 24. Schematic of the Half−bridge Mode Switching Test Circuit with Device RC Snubbers (Rs = 5 Ω, C_S = 150 pF) and a Bus RC Snubber (R_{SS} = 2.5 Ω, C_{SS} = 100 nF)

IMPORTANT MOUNTING INFORMATION

This product is recommended for use with solder pin attach and phase change thermal interface materials, and not recommended for implementations using press fit and application of thermal grease. Please refer to mounting guidelines and user guide documents associated with this product for detailed information.

APPLICATIONS INFORMATION

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.onsemi.com.

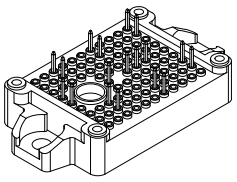
A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the **onsemi** website at www.onsemi.com.

ORDERING INFORMATION

Part Number	Marking	Package	Shipping
UHB50SC12E1BC3N	UHB50SC12E1BC3N	PIM18 33.80x42.50x12.00 E1B HALF BRIDGE (SOLDER PIN) (Pb-Free, Halogen Free)	24 Units / Tray Blister

REVISION HISTORY

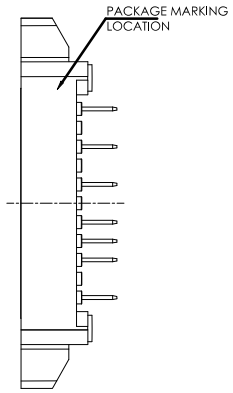
Revision	Description of Changes	Date
D	Acquired the original Qorvo JFET Division Data Sheet and updated the main document title to comply with **onsemi** standards for SiC products.	3/19/2025
4	Converted the Data Sheet to **onsemi** format.	6/10/2025



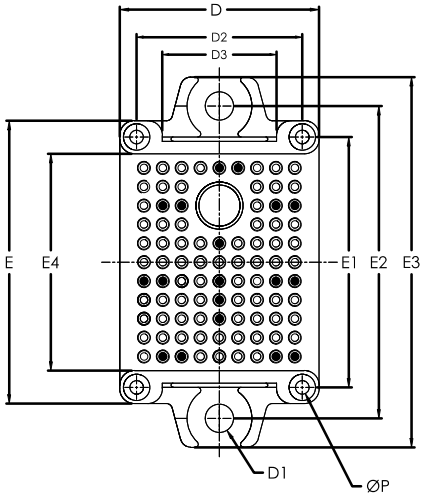
PIM18 33.80x42.50x12.00 E1B HALF BRIDGE (SOLDER PIN)
CASE 180DE
ISSUE O

DATE 21 MAR 2025

NOTES:
1.CONTROLLING DIMENSION: MILLIMETERS
2. PIN POSITION TOLERANCIS ±0.40mm

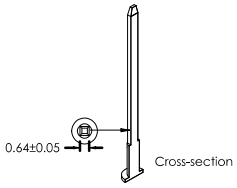


SIDE VIEW

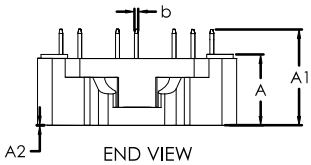


TOP VIEW

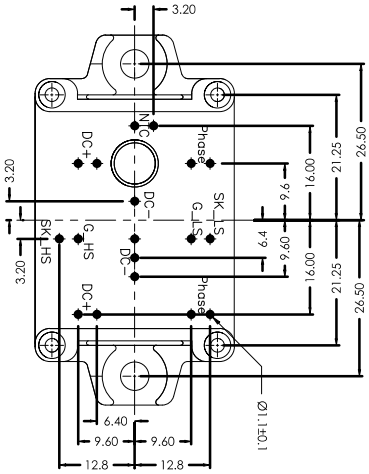
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	11.65	12.00	12.35
A1	15.75	16.25	16.75
A2	0.15	0.50	0.85
b	0.59	0.64	0.69
D	33.50	33.80	34.10
D1	Ø4.7	Ø4.8	Ø4.9
D2	27.90	28.10	28.30
D3	19.20	19.40	19.60
E	47.70	48.00	48.30
E1	42.30	42.50	42.70
E2	52.90	53.00	53.10
E3	62.30	62.80	63.30
E4	36.60	36.80	37.00
P	Ø2.2	Ø2.3	Ø2.4



PIN DETAIL SCALE: NTS



END VIEW
DBC exposal



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DESCRIPTION:	PIM18 33.80x42.50x12.00 E1B HALF BRIDGE (SOLDER PIN)	PAGE 1 OF 1

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