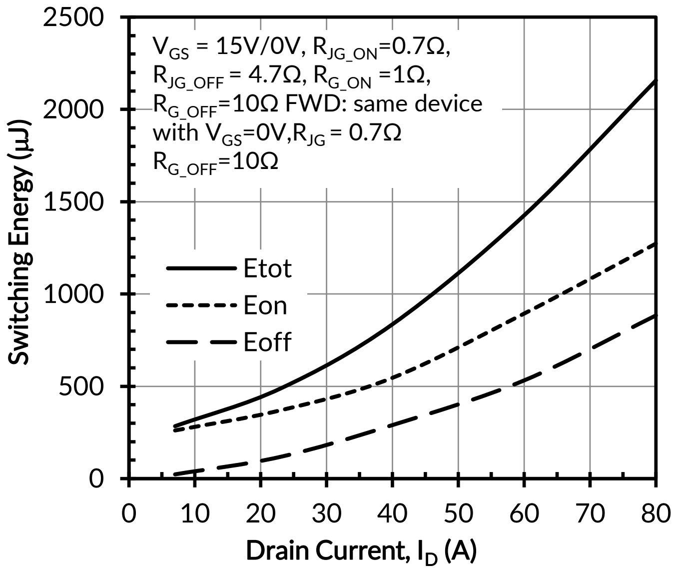

Figure 19. Clamped inductive switching energy vs. drain current at V_{DS} = 400V and T_J = 25°C

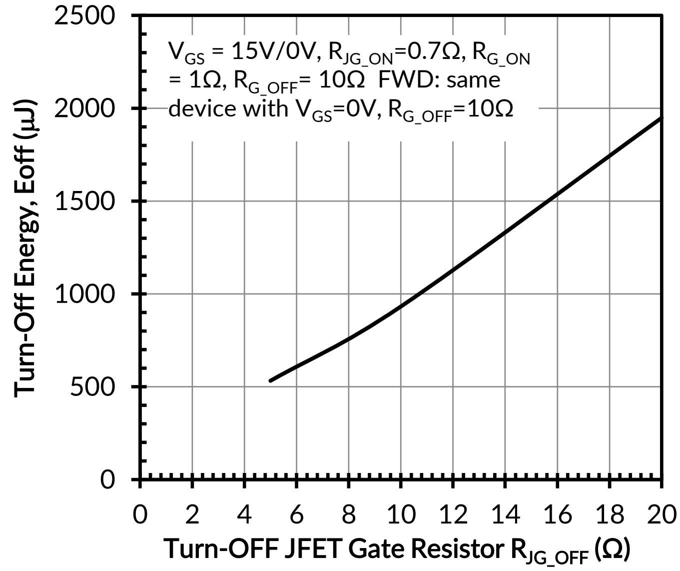

Figure 20. Clamped inductive switching turn-off energy vs. JFET gate resistor R_{JG_OFF} at V_{DS} = 400V, I_D = 60A, and T_J = 25°C

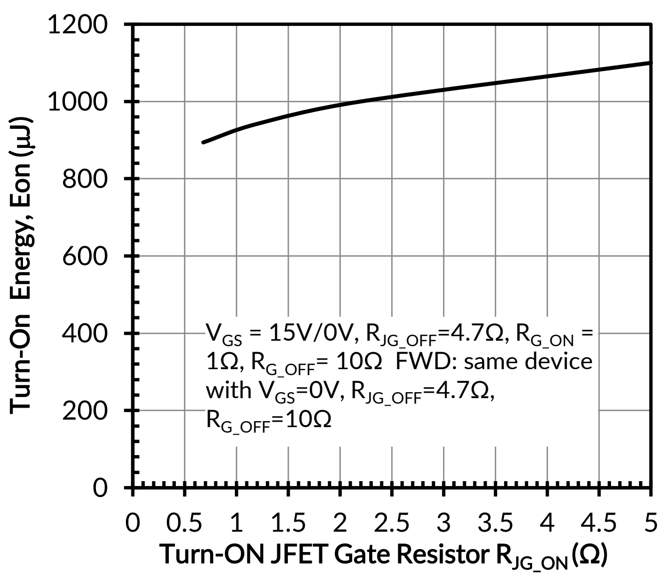

Figure 21. Clamped inductive switching turn-on energy vs. JFET gate resistor R_{JG_ON} at V_{DS} = 400V, I_D = 60A, and T_J = 25°C

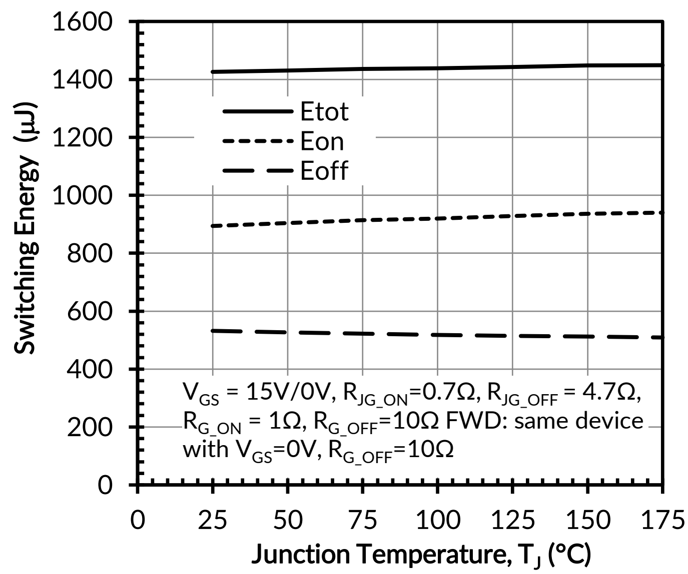

Figure 22. Clamped inductive switching energy vs. junction temperature at V_{DS} = 400V and I_D = 60A

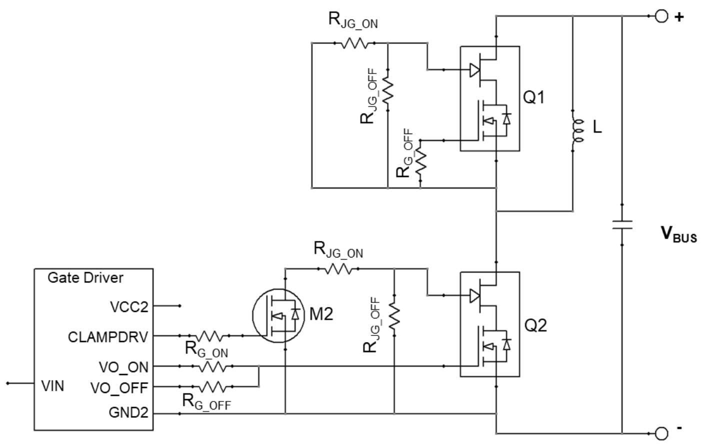

Figure 23. Schematic of the half-bridge mode switching test circuit with ClampDRIVE method.

Typical Performance Diagrams - JFET gate as control terminal and V_{GS}=+12V

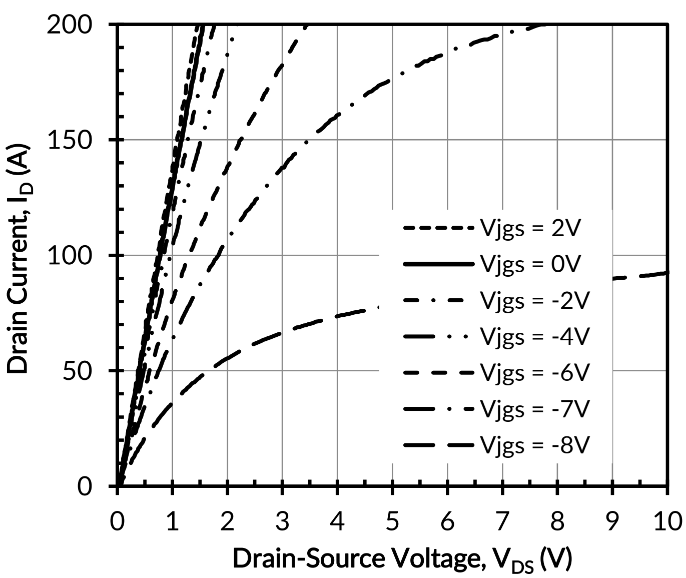

Figure 24. Typical output characteristics with JFET

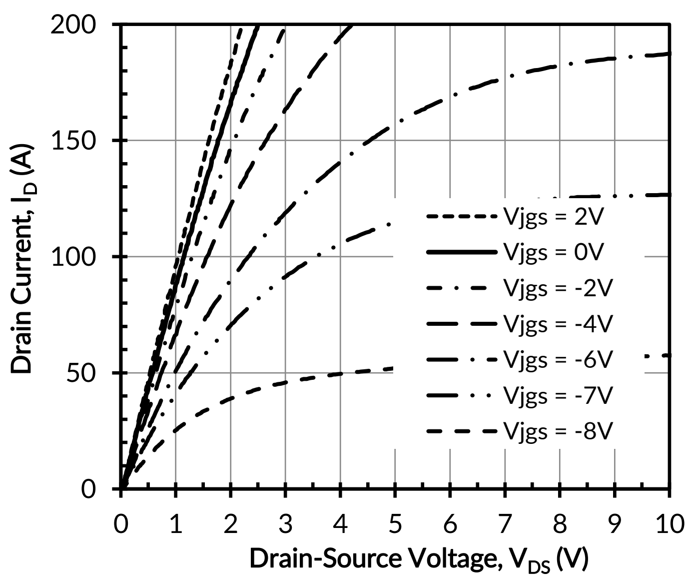

Figure 25. Typical output characteristics with JFET

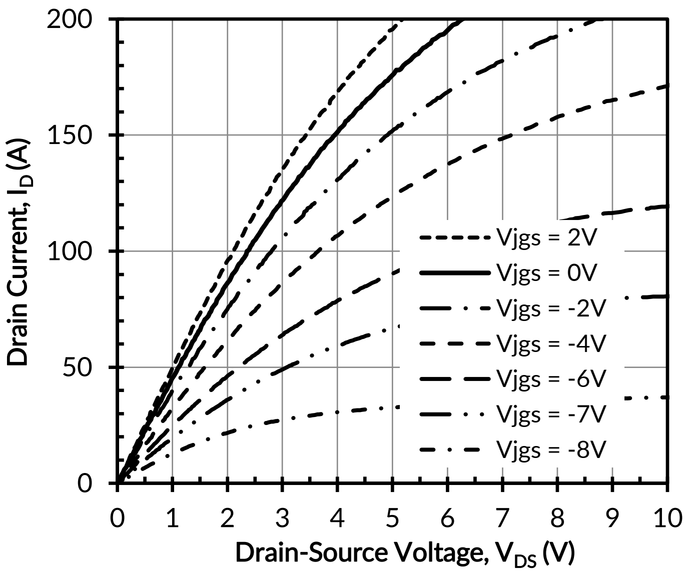

Figure 26. Typical output characteristics with JFET gate as control at T_J = 175°C, t_p < 250µs

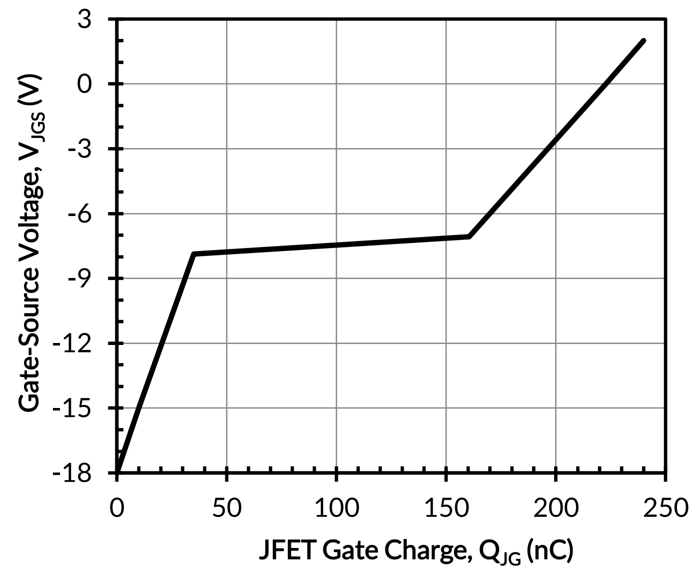

Figure 27. Typical JFET gate charge at V_{DS} = 400V and I_D = 60A

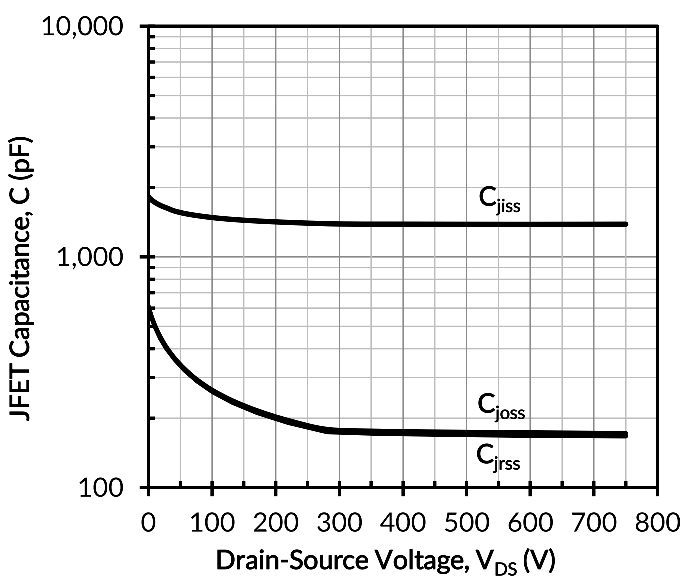

Figure 28. Typical JFET capacitances at f = 100kHz and V_{JGS} = -20V

Recommended Gate Drive Approach: ClampDRIVE method

Since both JFET gate and MOSFET gate are accessible, more parameters and approaches can be used to control the switching behaviors of the device and make the device suitable for a wide range applications from solid state circuit breakers requiring ultra-high current turn-off capability to motor drives requiring fast switching speed. The recommended gate drive approach is the ClampDRIVE method, with which the desired turn-on speed, turn-off speed and reverse recovery performance can be achieved at the same time. The main idea of this method is to dynamically tune the JFET gate resistor value R_{JG} such that, in the off-state, R_{JG} is small enough not to cause a reverse recovery issue, and during turn-off transient, R_{JG} is set to a higher value for the desired turn-off performance. This method can be easily implemented using a commercial off-the-shelf gate driver with miller clamp pre-driver output, as illustrated in Figure A. VIN is the gate driver input signal. VO is the gate driver output and CLAMPDRV is the gate driver miller clamp pre-driver output. M2 is the clamp MOSFET used to control the JFET gate resistance. The MOSFET M2 is directly controlled by the CLAMPDRV signal.

In the on-state, CLAMPDRV is low which turns the MOSFET M2 off, thus, the effective JFET gate resistance is R_{JG_OFF}. During the turn-off transient, CLAMPDRV is kept low until the device is fully off. This means the JFET gate resistance is R_{JG_OFF} during the turn-off process, and R_{GJ_OFF} can be used to effectively control turn-off speed. After the device is fully off, CLAMPDRV is changed to high level, which turns the MOSFET M2 on.

In the off-state, CLAMPDRV is high and the clamp MOSFET M2 is in on-state. The effective JFET gate resistance is equal to the parallel combination of R_{JG_OFF} and R_{JG_ON}. R_{JG_ON} can be selected small enough to prevent the reverse recovery issue. During the turn-on transient, the JFET gate current may flow from the cascode source through the body diode of the MOSFET M2 and R_{JG_ON} into the JFET gate, so, the turn-on process is also determined by R_{JG_ON}.

In summary, the optimum switching performance of the SiC cascode FETs can be realized with the ClampDRIVE method by selecting proper JFET gate resistors R_{JG_ON} and R_{JG_OFF}.

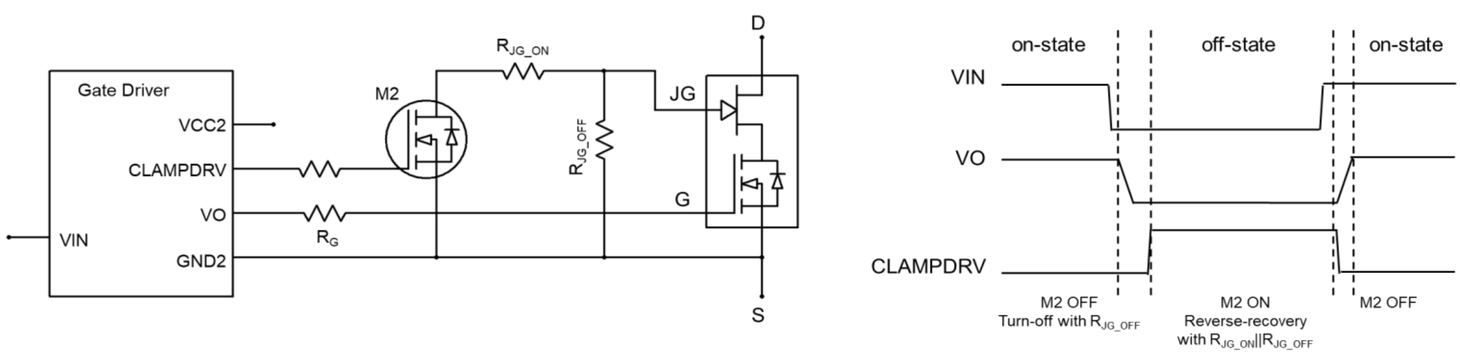

Figure A. Circuit schematic and timing diagram of the ClampDRIVE method

Important notice