

# QORVO

## SiC JFET Division

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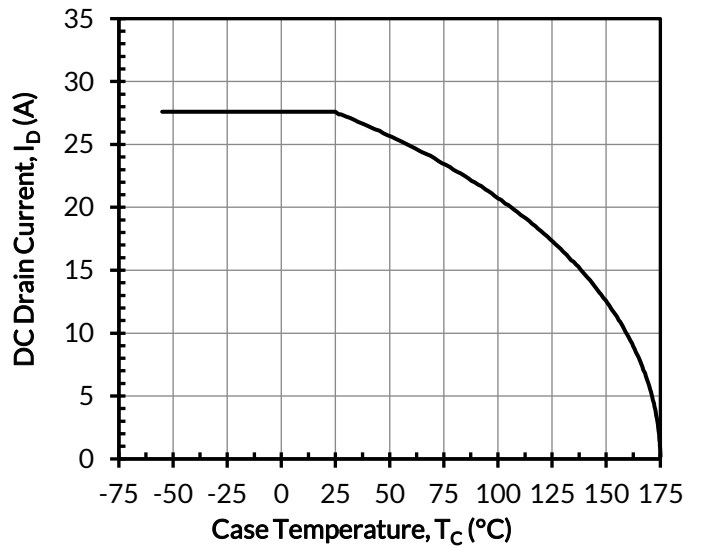
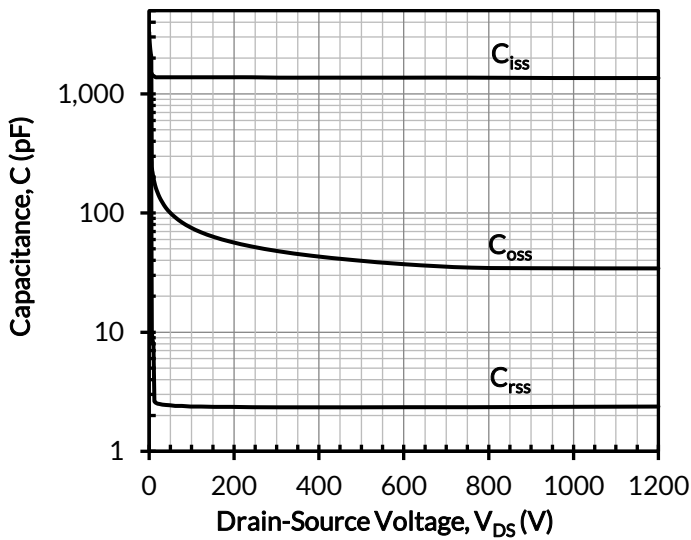


Figure 13. Typical capacitances at  $f = 100\text{kHz}$  and  $V_{GS} = 0\text{V}$

Figure 14. DC drain current derating

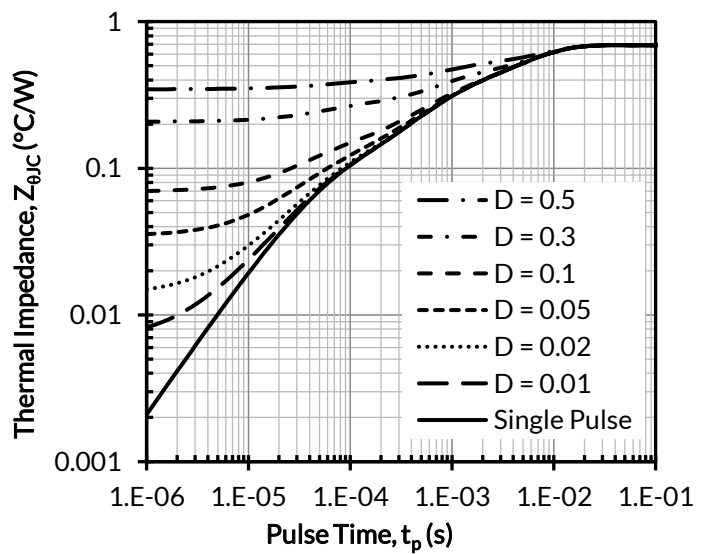
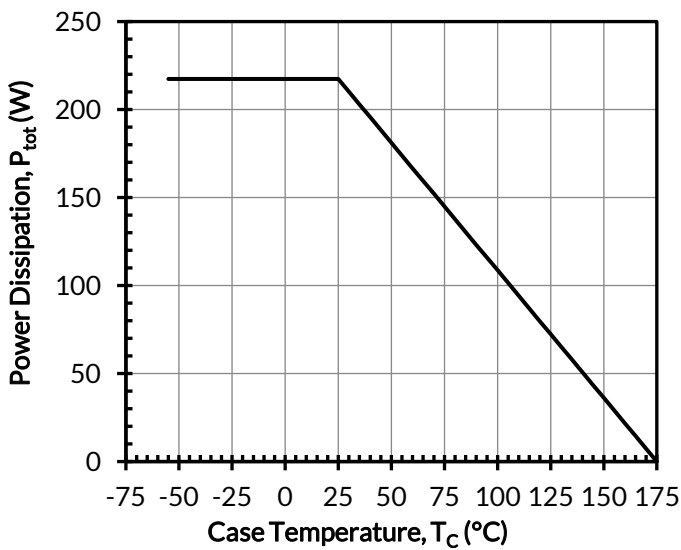


Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance

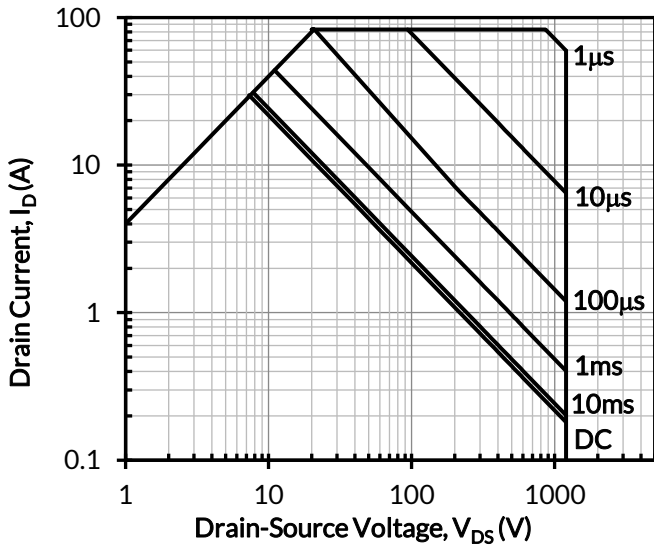


Figure 17. Safe operation area at  $T_C = 25^\circ\text{C}$ ,  $D = 0$ , Parameter  $t_p$

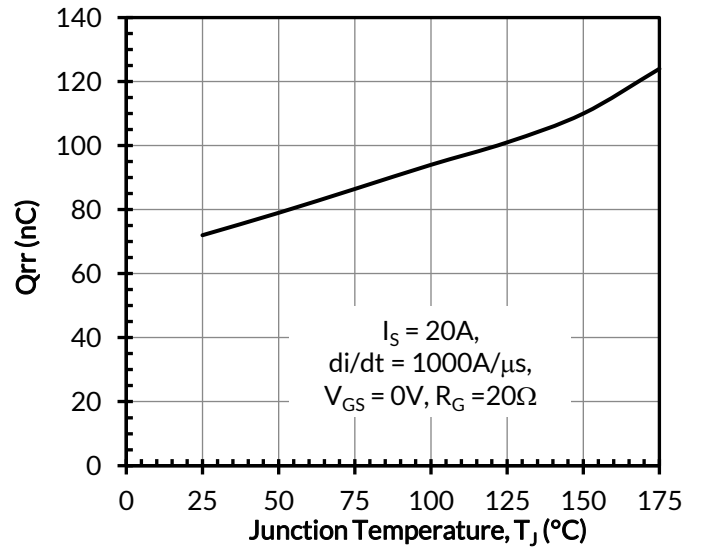


Figure 18. Reverse recovery charge  $Q_{rr}$  vs. junction temperature at  $V_{DS} = 800\text{V}$

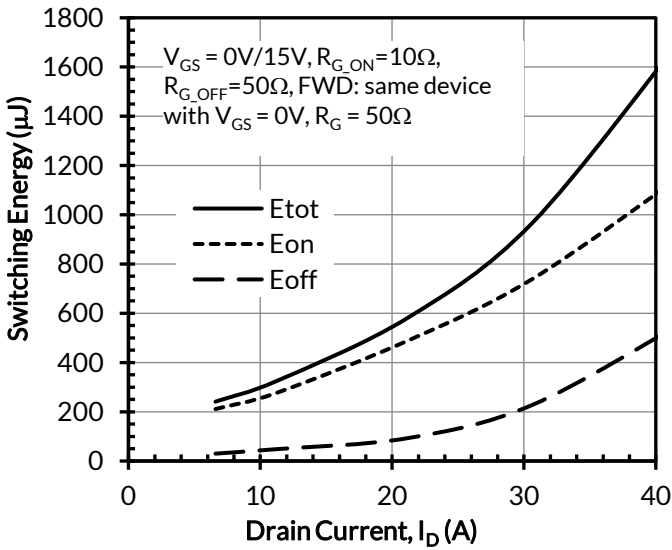


Figure 19. Clamped inductive switching energy vs. drain current at  $V_{DS} = 400\text{V}$  and  $T_J = 25^\circ\text{C}$

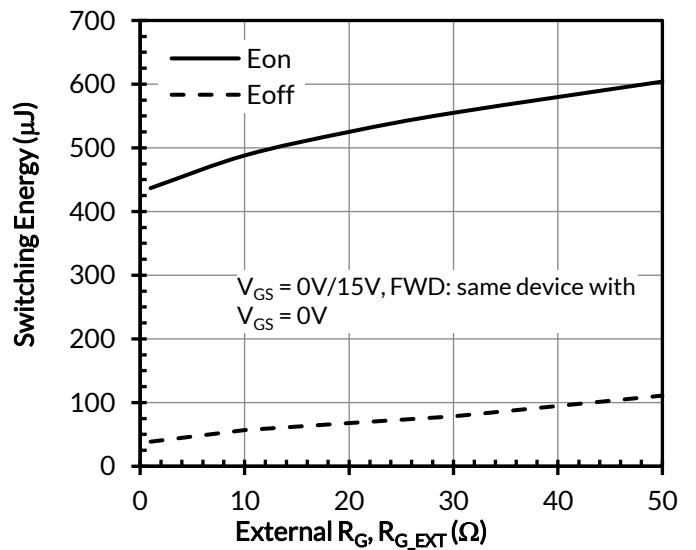


Figure 20. Clamped inductive switching energies vs.  $R_{G,EXT}$  at  $V_{DS} = 800\text{V}$ ,  $I_D = 20\text{A}$ , and  $T_J = 25^\circ\text{C}$

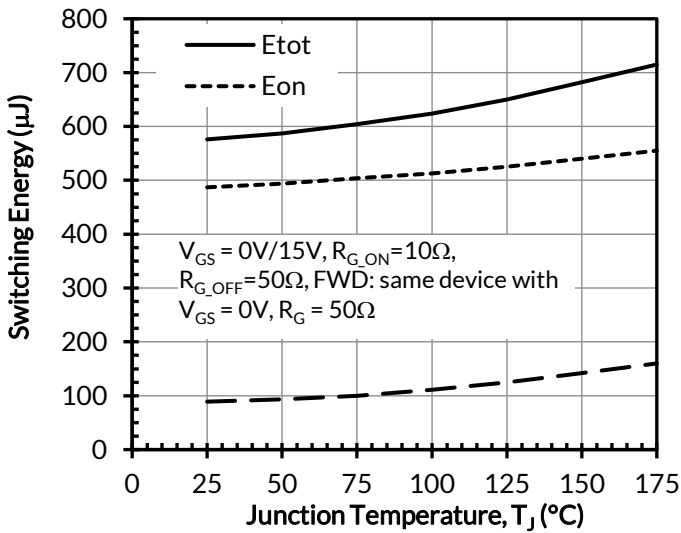


Figure 21. Clamped inductive switching energy vs. junction temperature at  $V_{DS} = 800V$  and  $I_D = 20A$

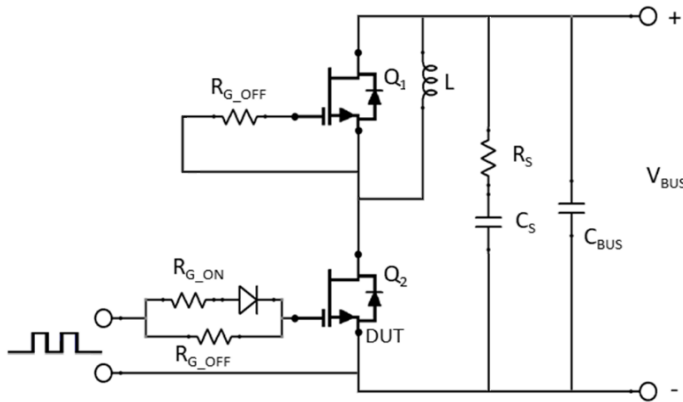


Figure 22. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber ( $R_S = 2.5\Omega$ ,  $C_S = 100nF$ ) is used to reduce the power loop high frequency oscillations.

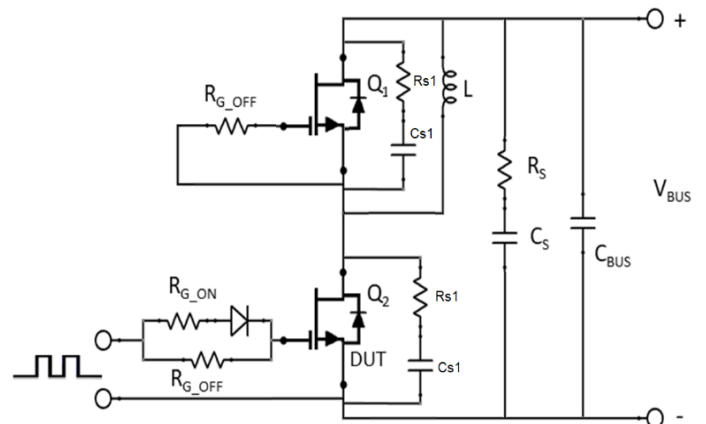


Figure 23. Schematic of the half-bridge mode switching test circuit with device RC snubbers ( $R_{s1} = 10\Omega$ ,  $C_{s1} = 95pF$ ) and a bus RC snubber ( $R_S = 2.5\Omega$ ,  $C_S = 100nF$ ).

## Applications Information

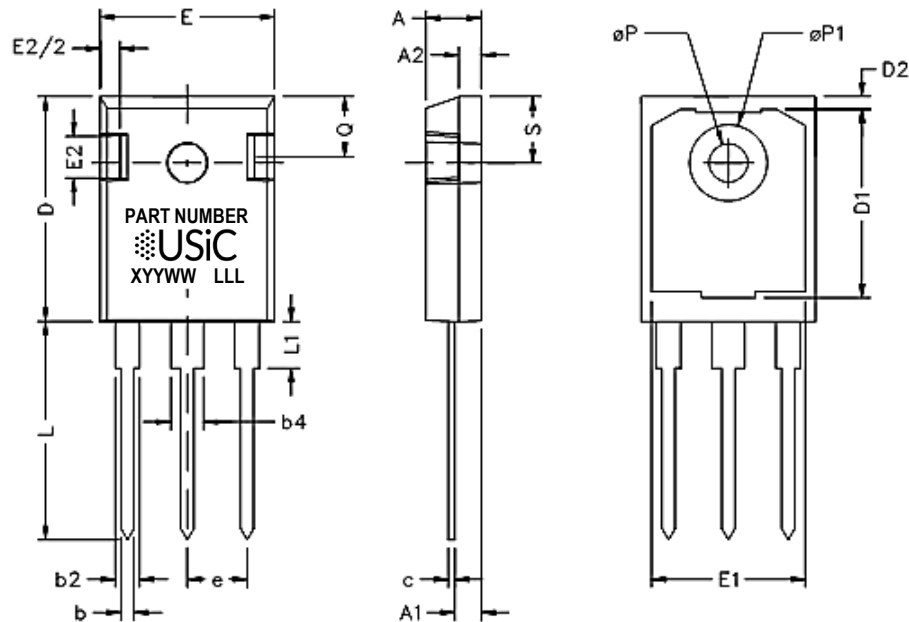
SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ( $R_{DS(on)}$ ), output capacitance ( $C_{oss}$ ), gate charge ( $Q_G$ ), and reverse recovery charge ( $Q_{rr}$ ) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high  $dv/dt$  and  $di/dt$  rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see [www.unitedsic.com](http://www.unitedsic.com).

A snubber circuit with a small  $R_{(G)}$ , or gate resistor, provides better EMI suppression with higher efficiency compared to using a high  $R_{(G)}$  value. There is no extra gate delay time when using the snubber circuitry, and a small  $R_{(G)}$  will better control both the turn-off  $V_{(DS)}$  peak spike and ringing duration, while a high  $R_{(G)}$  will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high  $R_{(G)}$ , while greatly reducing  $E_{(OFF)}$  from mid-to-full load range with only a small increase in  $E_{(ON)}$ . Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at [www.unitedsic.com](http://www.unitedsic.com)

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**PACKAGE OUTLINE**


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.185	0.209	4.699	5.309
A1	0.087	0.102	2.21	2.61
A2	0.059	0.098	1.499	2.489
b	0.039	0.055	0.991	1.397
b2	0.065	0.094	1.651	2.388
b4	0.102	0.135	2.591	3.429
c	0.015	0.035	0.381	0.889
D	0.819	0.845	20.803	21.463
D1	0.515	-	13.081	-
D2	0.02	0.053	0.508	1.346
E	0.61	0.64	15.494	16.256
e	0.214 BSC		5.44 BSC	
E1	0.53	-	13.462	-
E2	0.135	0.157	3.429	3.988
L	0.78	0.8	19.812	20.32
L1	-	0.177	-	4.496
ØP	0.14	0.144	3.556	3.658
ØP1	0.278	0.291	7.061	7.391
Q	0.212	0.244	5.385	6.198
S	0.243 BSC		6.17 BSC	

**PART MARKING****PART NUMBER**  
**XYYYWW LLL**

PART NUMBER = REFER TO  
DS\_PN DECODER FOR DETAILS

X = ASSEMBLY SITE

YY = YEAR

WW = WORK WEEK

LLL = LOT ID

**PACKING TYPE****ANTI-STATIC TUBE****QUANTITY /TUBE : 30 UNITS****DISCLAIMER**

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