

Silicon Carbide (SiC) JFET – EliteSiC, Power N-Channel, D2PAK-7L, 1700 V, 400 mohm

UF3N170400B7S

Description

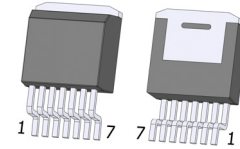
onsemi offers the High-Performance G3 SiC normally-On JFET transistors. This Series Exhibits Ultra-low on resistance ($R_{DS(ON)}$) and Gate charge (Q_G) allowing for Low Conduction and Switching loss. The device Normally-On Characteristics with low $R_{DS(ON)}$ at $V_{GS} = 0$ V is also ideal for current protection circuits without the need for active control, as well as for cascode operation.

Features

- Typical On-Resistance $R_{DS(on)}$, typ of 400 m Ω
- Voltage Controlled
- Maximum Operating Temperature of 175 °C
- Extremely Fast Switching not Dependent on Temperature
- Low Gate Charge
- Low Intrinsic Capacitance
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

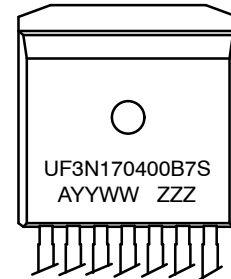
Typical Applications

- Over Current Protection Circuits
- DC-AC Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating



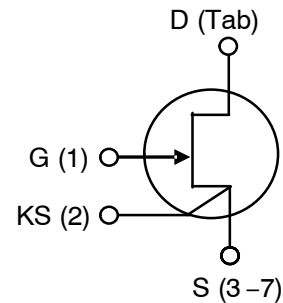
TO263-7
CASE 418BA

MARKING DIAGRAM



UF3N170400B7S = Specific Device Code
A = Assembly Location
YY = Year
WW = Work Week
ZZZ = Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		1700	V
Gate-Source Voltage	V_{GS}	DC	-20 to +3	V
		AC (Note 1)	-30 to +20	
Continuous Drain Current (Note 2)	I_D	$T_C = 25\text{ }^{\circ}\text{C}$	6.8	A
		$T_C = 100\text{ }^{\circ}\text{C}$	5.1	A
Pulsed Drain Current (Note 3)	I_{DM}	$T_C = 25\text{ }^{\circ}\text{C}$	16	A
Power Dissipation	P_{TOT}	$T_C = 25\text{ }^{\circ}\text{C}$	68	W
Maximum Junction Temperature	$T_{J,max}$		175	$^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG}		-55 to 175	$^{\circ}\text{C}$
Reflow Soldering Temperature	T_{solder}	Reflow MSL 1	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. +20 V AC Rating Applies for Turn-on Pulses <200 ns applied with external $R_G > 1\text{ }\Omega$

2. Limited by $T_{J,max}$

3. Pulse width t_p limited by $T_{J,max}$

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Value			
			Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		-	1.7	2.2	$^{\circ}\text{C/W}$

UF3N170400B7S

ELECTRICAL CHARACTERISTICS (T_J = +25 °C Unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC						
Drain-Source Breakdown Voltage	BV _{DS}	V _{GS} = -20 V, I _D = 0.3 mA	1700	–	–	V
Total Drain Leakage Current	I _{DSS}	V _{DS} = 1700 V, V _{GS} = -20 V, T _J = 25 °C	–	2.2	60	μA
		V _{DS} = 1700 V, V _{GS} = -20 V, T _J = 175 °C	–	9	–	
Total Gate Leakage Current	I _{GSS}	V _{GS} = -20 V, T _J = 25 °C	–	0.15	6	μA
		V _{GS} = -20 V, T _J = 175 °C	–	0.8	–	μA
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 2 V, I _D = 5 A, T _J = 25 °C	–	350	–	mΩ
		V _{GS} = 0 V, I _D = 5 A, T _J = 25 °C	–	400	500	
		V _{GS} = 2 V, I _D = 5 A, T _J = 175 °C	–	928	–	
		V _{GS} = 0 V, I _D = 5 A, T _J = 175 °C	–	1040	–	
Gate Threshold Voltage	V _{G(th)}	V _{DS} = 5 V, I _D = 4.5 mA	-11.3	-9	-6.7	V
Gate Resistance	R _G	f = 1 MHz, Open Drain	–	5	–	Ω

TYPICAL PERFORMANCE – DYNAMIC

Input Capacitance	C _{iss}	V _{DS} = 100 V, V _{GS} = -20 V, f = 100 kHz	–	225	–	pF
Output Capacitance	C _{oss}		–	22	–	
Reverse Transfer Capacitance	C _{rss}		–	18	–	
Effective Output Capacitance, Energy Related	C _{oss(er)}	V _{DS} = 0 V to 1200 V, V _{GS} = -20 V	–	11.4	–	pF
C _{oss} stored energy	E _{oss}	V _{DS} = 1200 V, V _{GS} = -20 V	–	8.2	–	μJ
Total Gate Charge	Q _G	V _{DS} = 1200 V, I _D = 5 A, V _{GS} = -18 V to 0 V	–	30	–	nC
Gate-Drain Charge	Q _{GD}		–	17	–	
Gate-Source Charge	Q _{GS}		–	5	–	
Turn-On Delay Time	t _{d(on)}	V _{DS} = 1200 V, I _D = 5 A, Gate Driver = -18 V to + 0 V, R _G = 1 Ω, Inductive Load, FWD: 2x UJ3D1210TS in series T _J = 25 °C	–	5	–	ns
Rise Time	t _r		–	19	–	
Turn-Off Delay Time	t _{d(off)}		–	9	–	
Fall Time	t _f		–	37	–	
Turn-On Energy	E _{ON}	V _{DS} = 1200 V, I _D = 5 A, Gate Driver = -18 V to + 0 V, R _G = 1 Ω, Inductive Load, FWD: 2x UJ3D1210TS in series T _J = 150 °C	–	125	–	μJ
Turn-Off Energy	E _{OFF}		–	38	–	
Total Switching Energy	E _{TOTAL}		–	163	–	
Turn-On Delay Time	t _{d(on)}		–	5	–	ns
Rise Time	t _r		–	16	–	
Turn-Off Delay Time	t _{d(off)}		–	8	–	
Fall Time	t _f		–	34	–	
Turn-On Energy	E _{ON}		–	114	–	μJ
Turn-Off Energy	E _{OFF}		–	31	–	
Total Switching Energy	E _{TOTAL}		–	145	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE DIAGRAMS

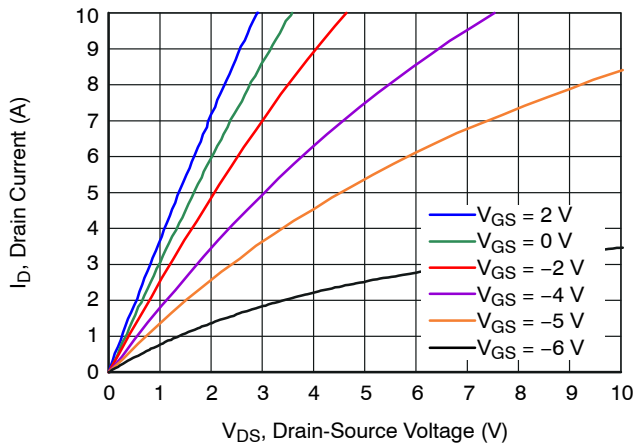


Figure 1. Typical Output Characteristics at $T_J = -55\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

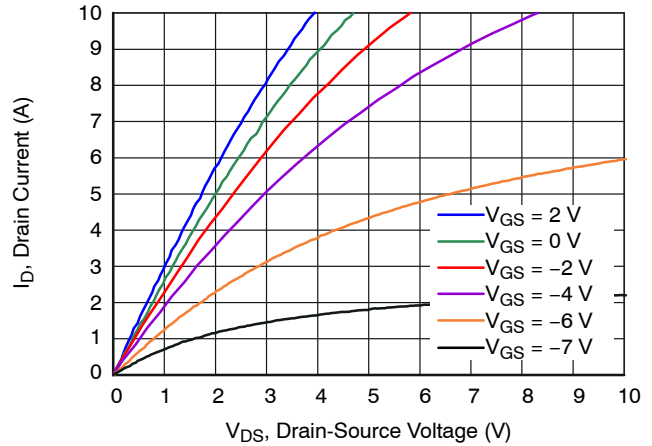


Figure 2. Typical Output Characteristics at $T_J = 25\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

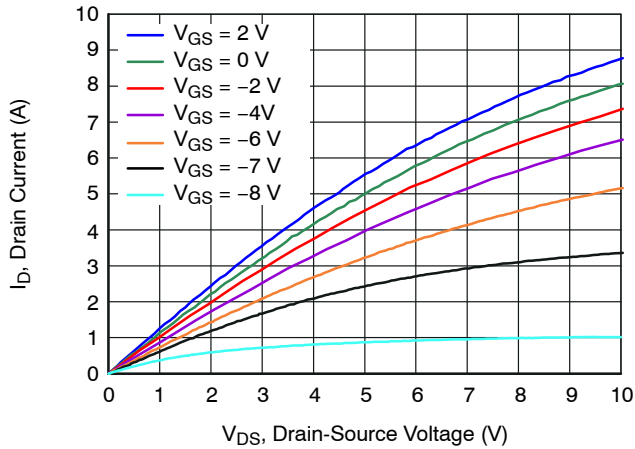


Figure 3. Typical Output Characteristics at $T_J = 175\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

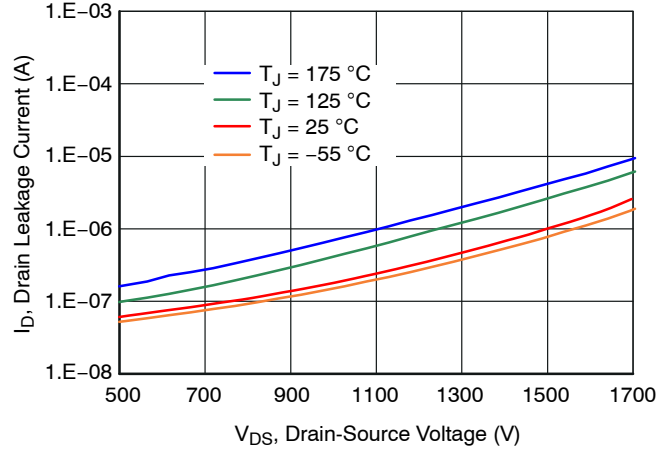


Figure 4. Typical Drain-Source Leakage at $V_{DS} = -20\text{ V}$

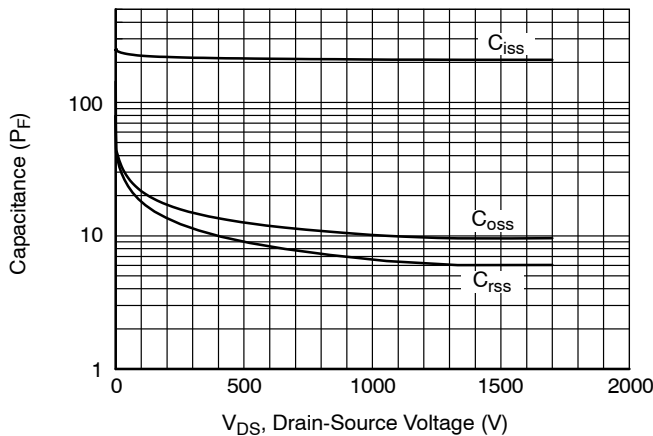


Figure 5. Typical Capacitances at 100 KHz and $V_{GS} = -20\text{ V}$

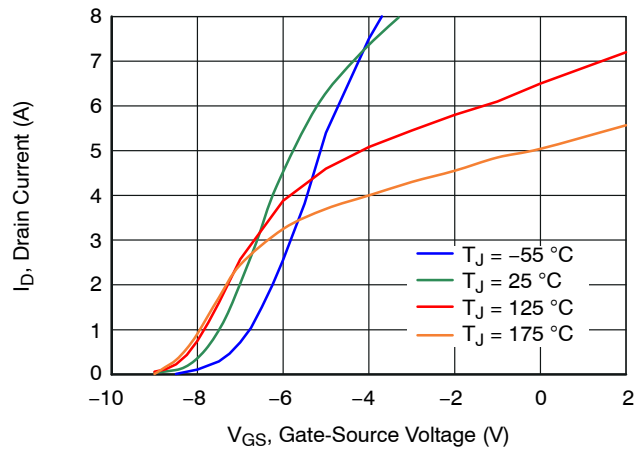


Figure 6. Typical Transfer Characteristics at $V_{DS} = 5\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)

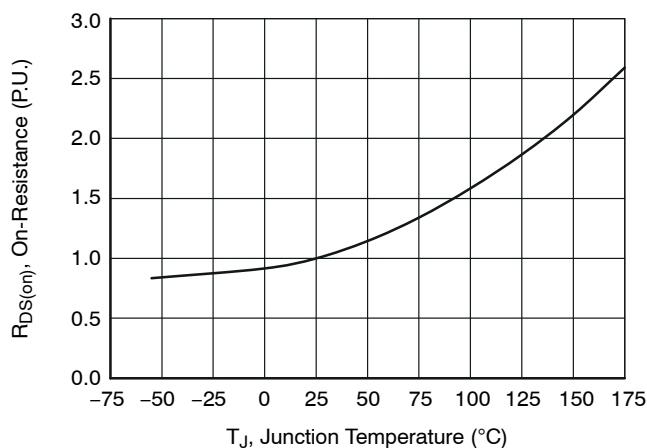


Figure 7. Normalized On-Resistance Vs. Temperature at $V_{GS} = 0\text{ V}$ and $I_D = 5\text{ A}$

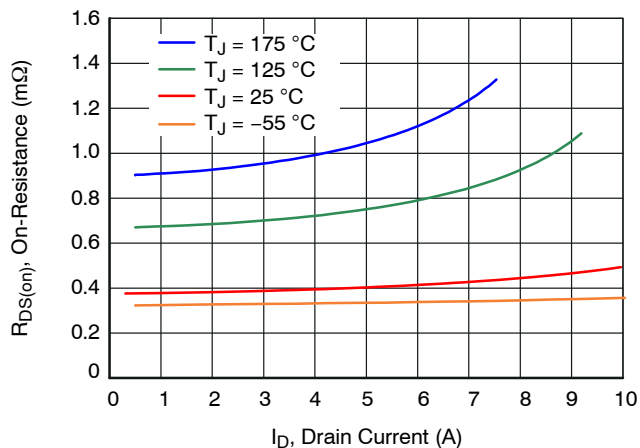


Figure 8. Typical Drain-Source On-Resistance $V_{GS} = 0\text{ V}$

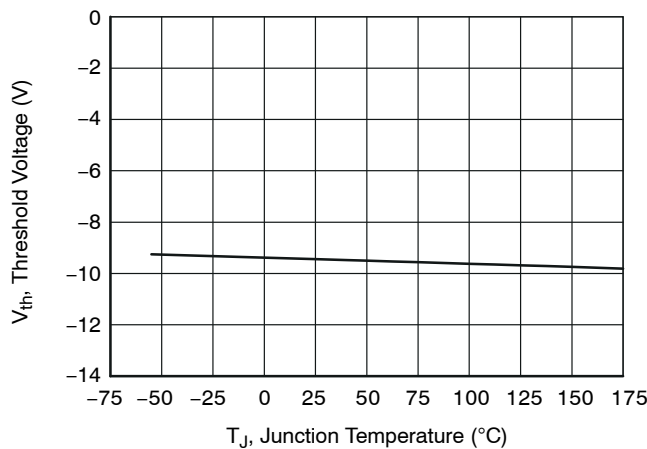


Figure 9. Threshold Voltage vs. Junction Temperature at $V_{DS} = 5\text{ V}$ and $I_D = 4.5\text{ mA}$

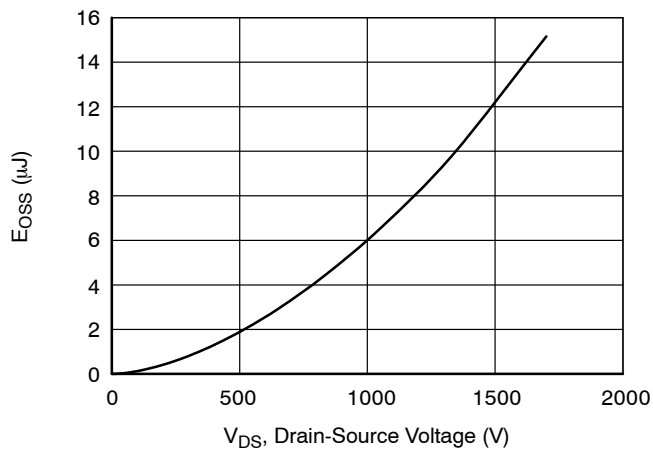


Figure 10. Typical Stored Energy in C_{OSS} at $V_{GS} = -20\text{ V}$

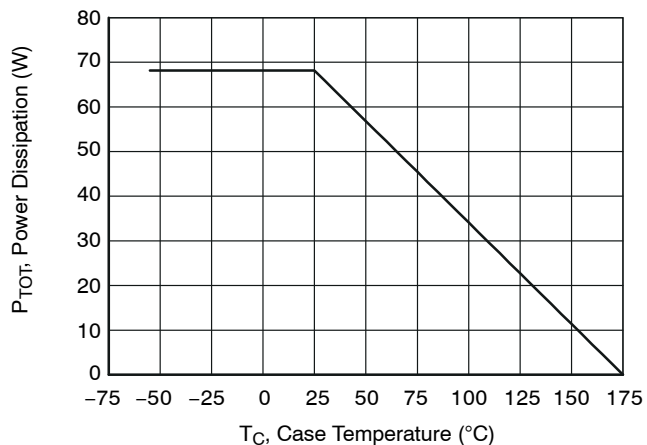


Figure 11. Total Power Dissipation

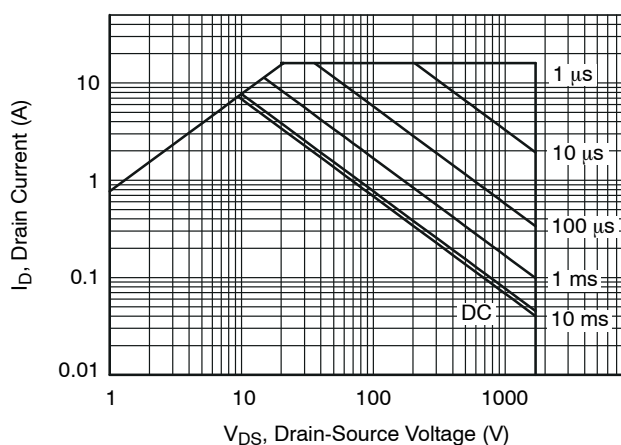


Figure 12. Safe Operation Area at $T_C = 25\text{ °C}$, Parameter t_p

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)

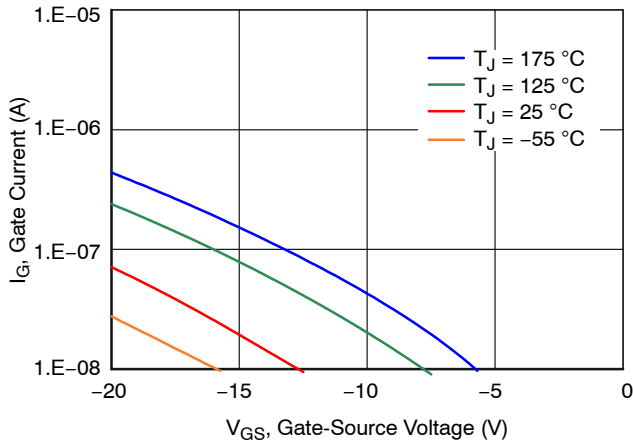


Figure 13. Typical Gate Leakage Current at $V_{DS} = 0$ V

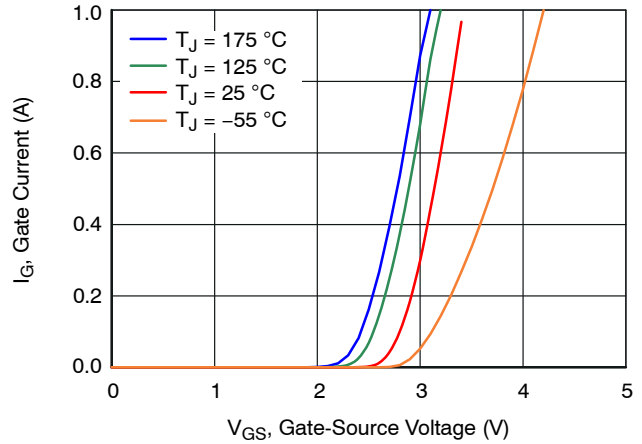


Figure 14. Typical Gate Forward Current at $V_{DS} = 0$ V

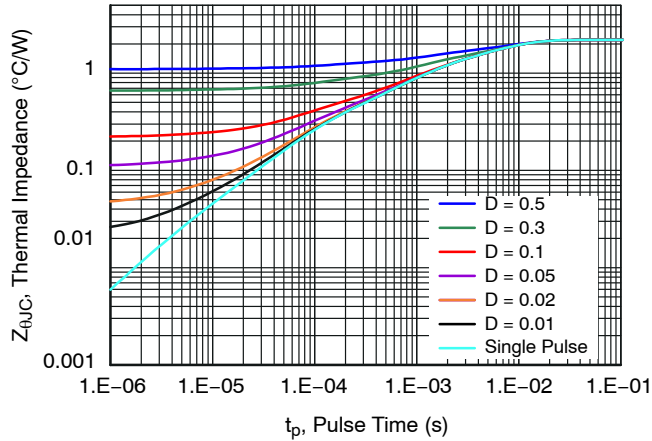


Figure 15. Maximum Transient Thermal Impedance

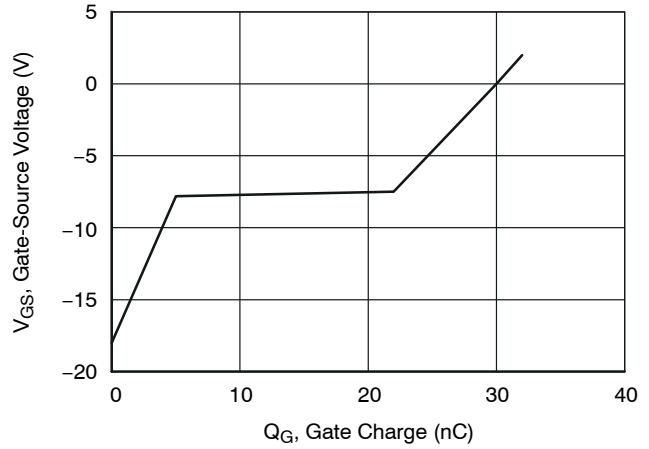


Figure 16. Typical Gate Charge at $V_{DS} = 1200$ V and $I_D = 5$ A

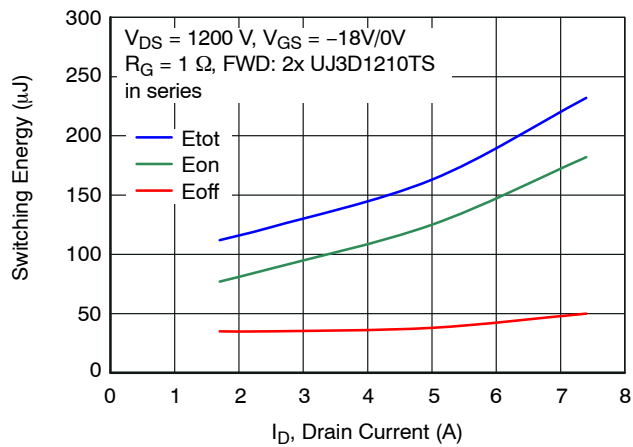


Figure 17. Clamped Inductive Switching Energy vs. Drain Current at $T_J = 25$ °C

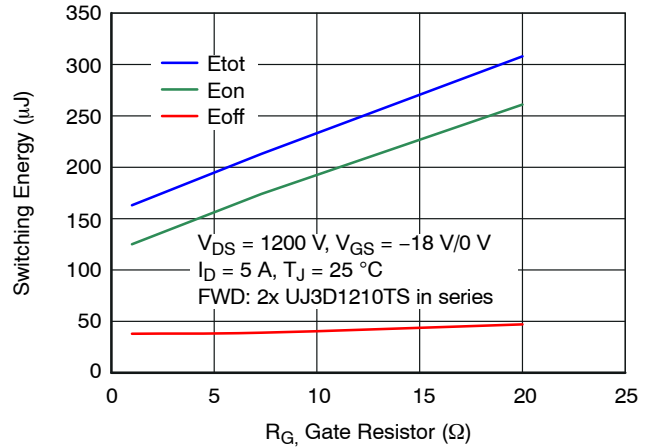


Figure 18. Clamped Inductive Switching Energy vs. Gate Resistor R_G

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)

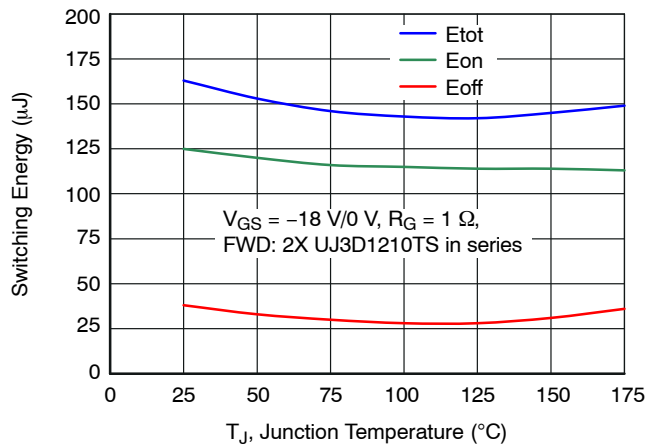
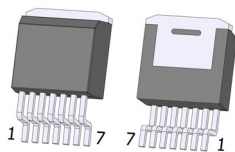


Figure 19. Clamped Inductive Switching Energy vs. Junction Temperature at $V_{DS} = 1200\text{ V}$ and $I_D = 5\text{ A}$

ORDERING INFORMATION

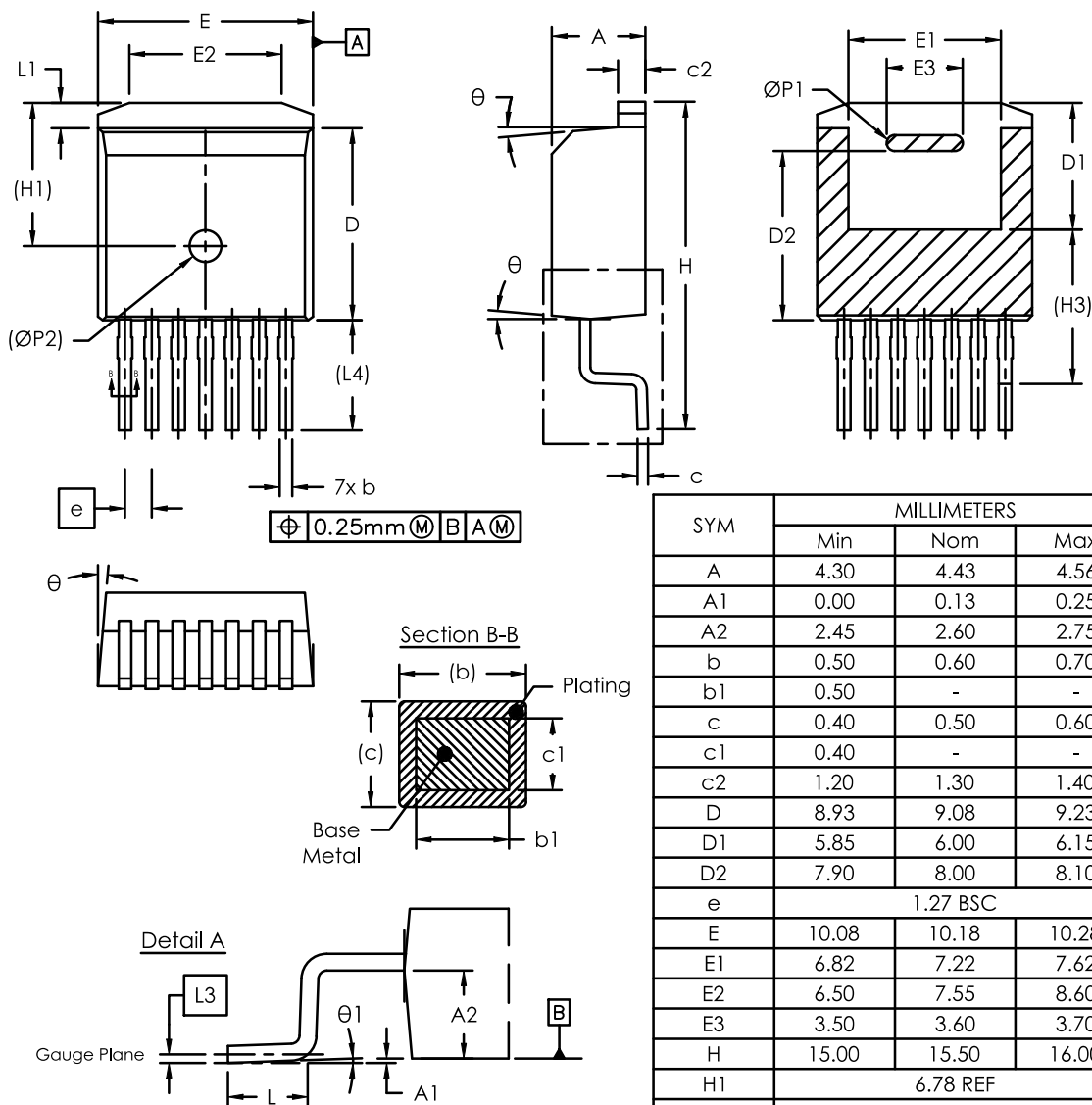
Part Number	Marking	Package	Shipping [†]
UF3N170400B7S	UF3N170400B7S	D ² PAK-7L (Pb-Free, Hlogen Free)	800 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



TO-263-7 10.18x9.08x4.43, 1.27P
CASE 418BA
ISSUE B

DATE 17 APR 2025



SYM	MILLIMETERS		
	Min	Nom	Max
A	4.30	4.43	4.56
A1	0.00	0.13	0.25
A2	2.45	2.60	2.75
b	0.50	0.60	0.70
b1	0.50	-	-
c	0.40	0.50	0.60
c1	0.40	-	-
c2	1.20	1.30	1.40
D	8.93	9.08	9.23
D1	5.85	6.00	6.15
D2	7.90	8.00	8.10
e	1.27 BSC		
E	10.08	10.18	10.28
E1	6.82	7.22	7.62
E2	6.50	7.55	8.60
E3	3.50	3.60	3.70
H	15.00	15.50	16.00
H1	6.78 REF		
H3	7.30 REF.		
L	1.90	2.20	2.50
L1	0.98	1.20	1.42
L3	0.25 BSC		
L4	5.22 REF		
ØP1	0.65	0.75	0.85
ØP2	1.50 REF		
θ	5°		
θ_1	3°		

Notes:

1. Dimensioning and Tolerancing as per ASME Y14.5M, 2018.
2. Controlling Dimension : Millimeters
3. Package body sides exclude mold flash and gate burrs.
4. Dimension L is measured on gauge plane.
5. Dimension c1 and b1 applies to base metal only.

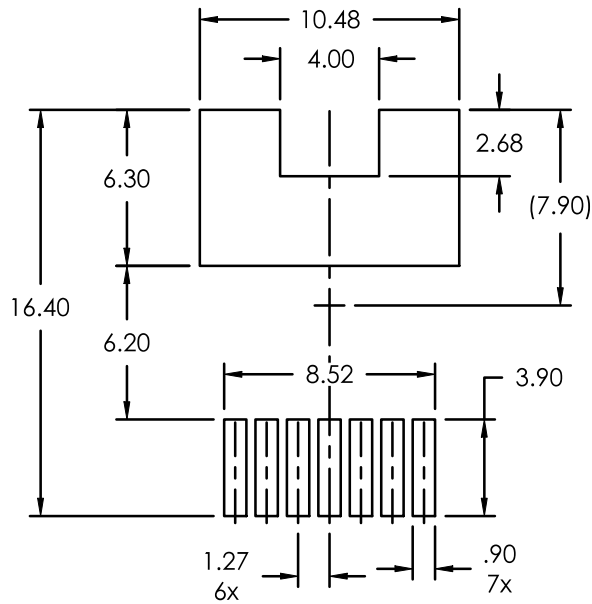
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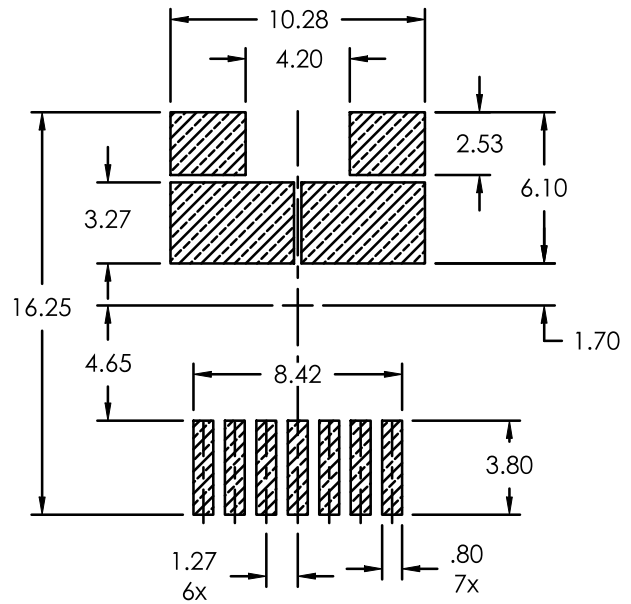
TO-263-7 10.18x9.08x4.43, 1.27P
CASE 418BA
ISSUE B

DATE 17 APR 2025

RECOMMENDED PCB FOOTPRINT

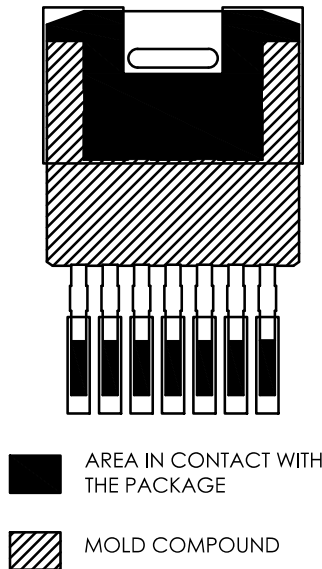


RECOMMENDED STENCIL APERTURE



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PCB FOOTPRINT with PACKAGE OVERLAY



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