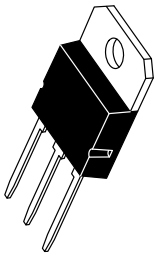
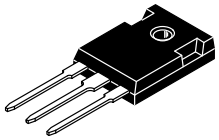
Complementary Silicon High-Power Transistors

TIP35A, TIP35B, TIP35C (NPN); TIP36A, TIP36B, TIP36C (PNP)

Designed for general–purpose power amplifier and switching applications.



SOT–93 (TO–218)
CASE 340D
STYLE 1



TO–247
CASE 340L
STYLE 3

NOTE: Effective June 2012 this device will be available only in the TO–247 package. Reference FPCN# 16827.

Features

- 25 A Collector Current
- Low Leakage Current –
  I_{CEO} = 1.0 mA @ 30 and 60 V
- Excellent DC Gain –
  h_{FE} = 40 Typ @ 15 A
- High Current Gain Bandwidth Product –
  $|h_{fe}|$ = 3.0 min @ I_C
  = 1.0 A, f = 1.0 MHz
- These are Pb–Free Devices*

25 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60–100 VOLTS, 125 WATTS

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MAXIMUM RATINGS

Symbol	Rating	TIP35A TIP36A	TIP35B TIP36B	TIP35C TIP36C	Unit
V_{CEO}	Collector – Emitter Voltage	60	80	100	Vdc
V_{CB}	Collector – Base Voltage	60	80	100	Vdc
V_{EB}	Emitter – Base Voltage	5.0			Vdc
I_C	Collector Current – Continuous – Peak (Note 1)	 25 40			Adc
I_B	Base Current – Continuous	5.0			Adc
P_D	Total Power Dissipation @ T_C = 25°C Derate above 25°C	125			 W W/°C
T_J, T_{stg}	Operating and Storage Junction Temperature Range	–65 to +150			°C
E_{SB}	Unclamped Inductive Load	90			mJ

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

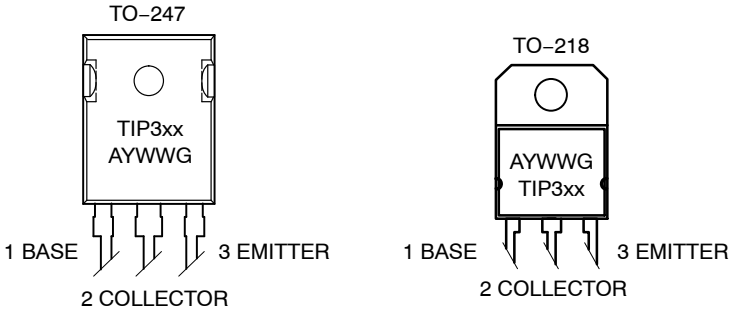
THERMAL CHARACTERISTICS

Symbol	Characteristic	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction–to–Case	1.0	°C/W
$R_{\theta JA}$	Junction–To–Free–Air Thermal Resistance	35.7	°C/W

1. Pulse Test: Pulse Width = 10 ms, Duty Cycle ≤ 10%.

*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MARKING DIAGRAMS



TIP3xx	= Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Max	Unit
OFF CHARACTERISTICS				
$V_{CEO(sus)}$	Collector−Emitter Sustaining Voltage (Note 2) (I_C = 30 mA, I_B = 0) TIP35A, TIP36A TIP35B, TIP36B TIP35C, TIP36C	 60 80 100	 − − −	Vdc
I_{CEO}	Collector−Emitter Cutoff Current (V_{CE} = 30 V, I_B = 0) TIP35A, TIP36A (V_{CE} = 60 V, I_B = 0) TIP35B, TIP35C, TIP36B, TIP36C	 − −	 1.0 1.0	mA
I_{CES}	Collector−Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)	−	0.7	mA
I_{EBO}	Emitter−Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)	−	1.0	mA
ON CHARACTERISTICS (Note 2)				
h_{FE}	DC Current Gain (I_C = 1.5 A, V_{CE} = 4.0 V) (I_C = 15 A, V_{CE} = 4.0 V)	 25 15	 − 75	−
$V_{CE(sat)}$	Collector−Emitter Saturation Voltage (I_C = 15 A, I_B = 1.5 A) (I_C = 25 A, I_B = 5.0 A)	 − −	 1.8 4.0	Vdc
$V_{BE(on)}$	Base−Emitter On Voltage (I_C = 15 A, V_{CE} = 4.0 V) (I_C = 25 A, V_{CE} = 4.0 V)	 − −	 2.0 4.0	Vdc
DYNAMIC CHARACTERISTICS				
h_{fe}	Small−Signal Current Gain (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 kHz)	25	−	−
f_T	Current−Gain — Bandwidth Product (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 MHz)	3.0	−	MHz

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

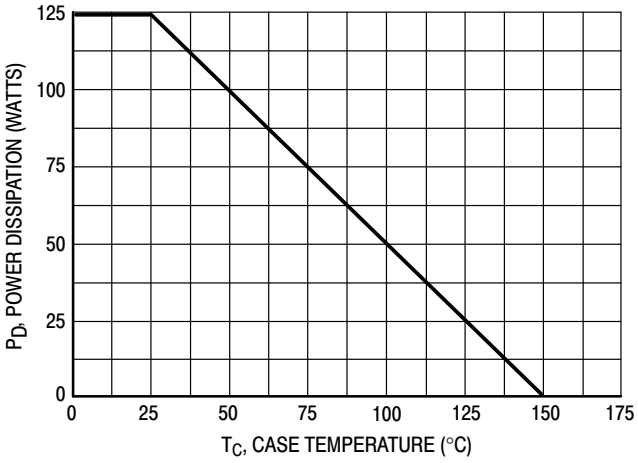
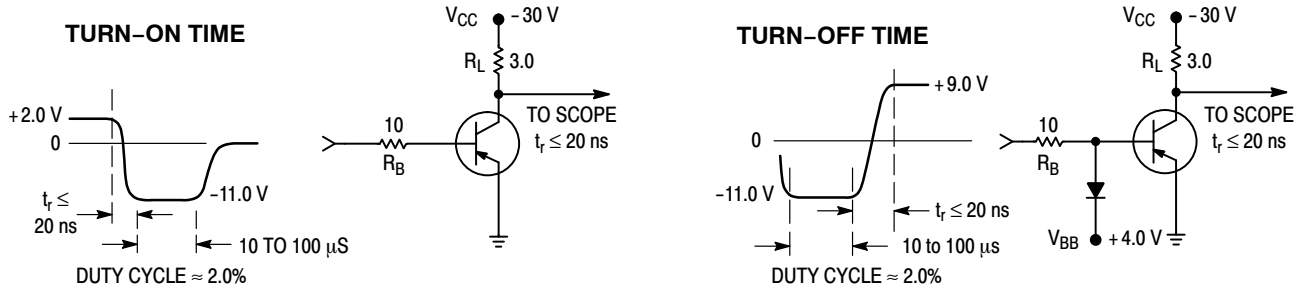


Figure 1. Power Derating



FOR CURVES OF FIGURES 3 & 4, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES.

Figure 2. Switching Time Equivalent Test Circuits

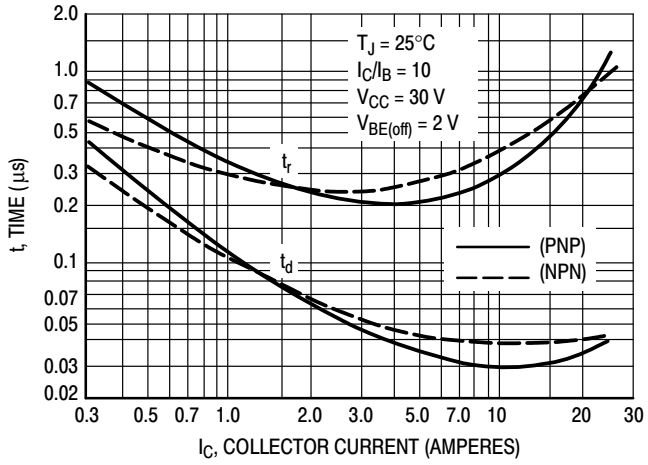


Figure 3. Turn−On Time

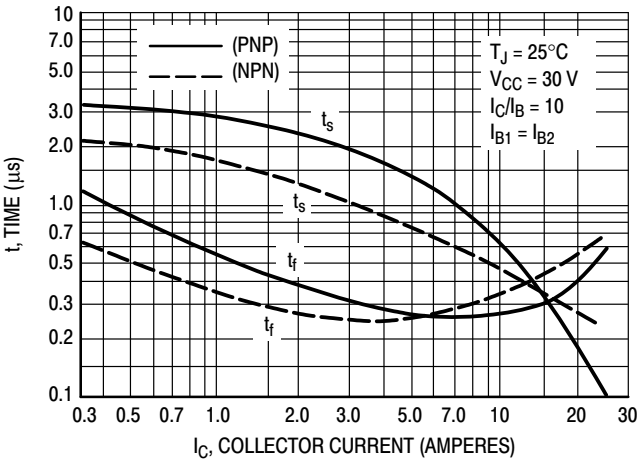


Figure 4. Turn−Off Time

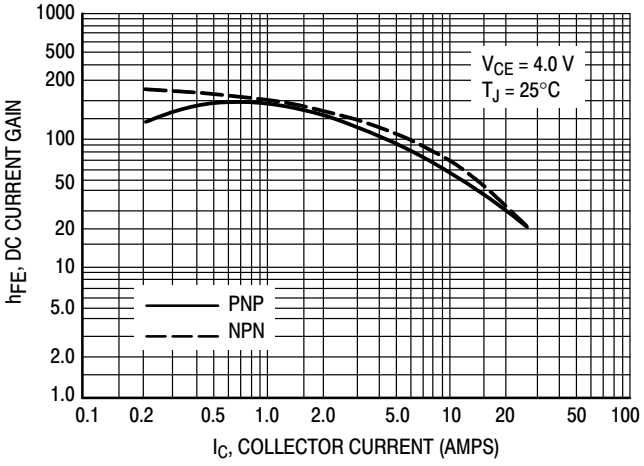


Figure 5. DC Current Gain

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives RBSOA characteristics.

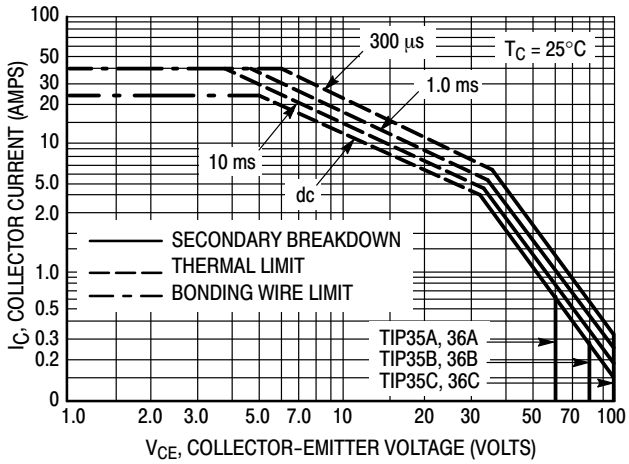


Figure 6. Maximum Rated Forward Bias Safe Operating Area

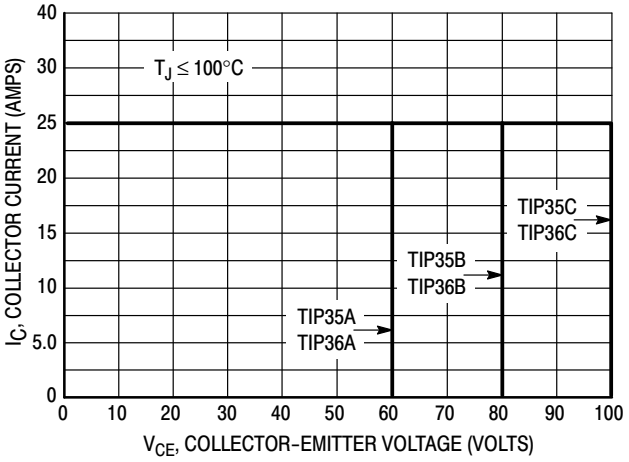
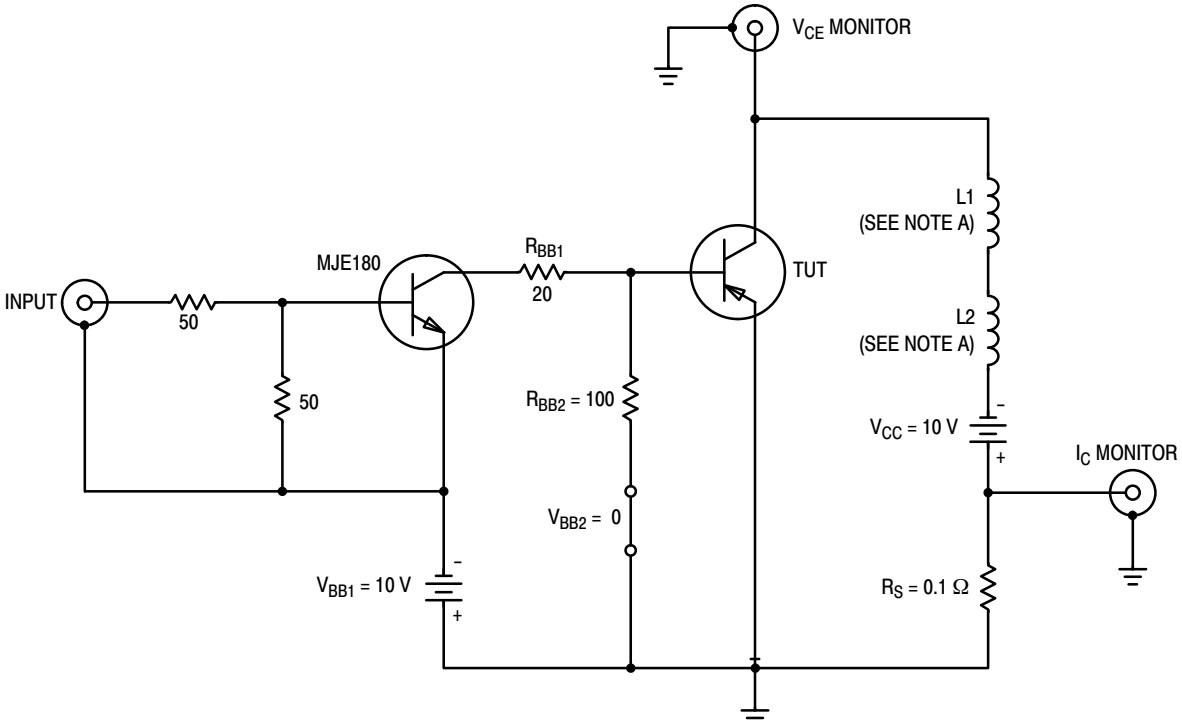
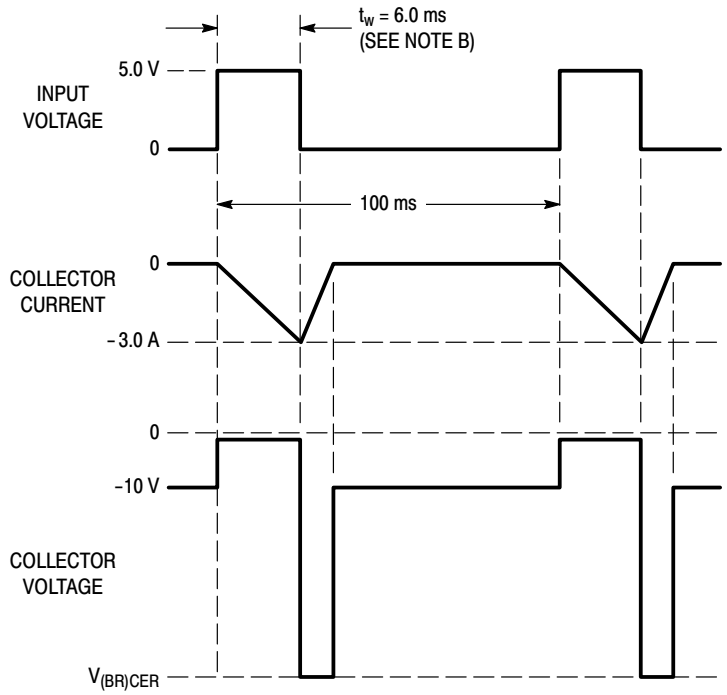


Figure 7. Maximum Rated Forward Bias Safe Operating Area

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



NOTES:

A. L1 and L2 are 10 mH, 0.11 Ω, Chicago Standard Transformer Corporation C−2688, or equivalent.
B. Input pulse width is increased until I_{CM} = −3.0 A.
C. For NPN, reverse all polarities.

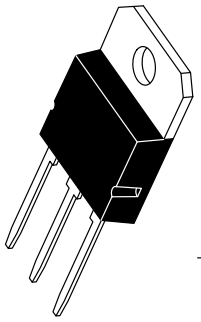
Figure 8. Inductive Load Switching

ORDERING INFORMATION

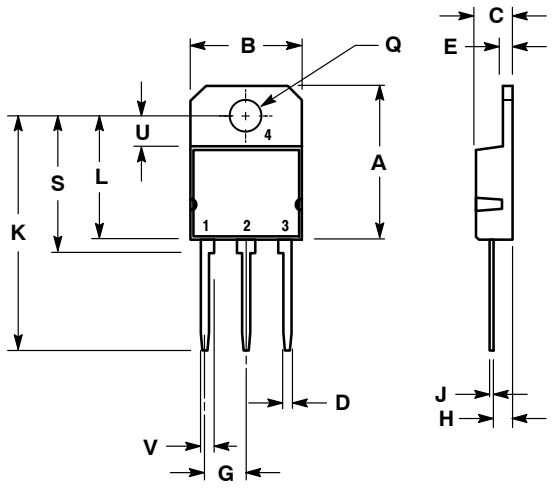
Device	Package	Shipping
TIP35AG	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP35BG	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP35CG	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP36AG	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP36BG	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP36CG	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP35AG	TO−247 (Pb−Free)	30 Units / Rail
TIP35BG	TO−247 (Pb−Free)	30 Units / Rail
TIP35CG	TO−247 (Pb−Free)	30 Units / Rail
TIP36AG	TO−247 (Pb−Free)	30 Units / Rail
TIP36BG	TO−247 (Pb−Free)	30 Units / Rail
TIP36CG	TO−247 (Pb−Free)	30 Units / Rail

SOT−93 (TO−218)
CASE 340D−02
ISSUE E

DATE 03 JAN 2002



SCALE 1:1



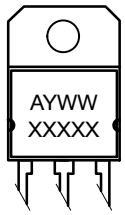
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	20.35	---	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	---	16.20	---	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

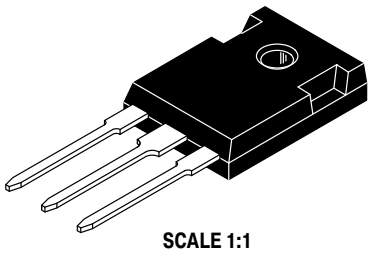
GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
XXXXX = Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

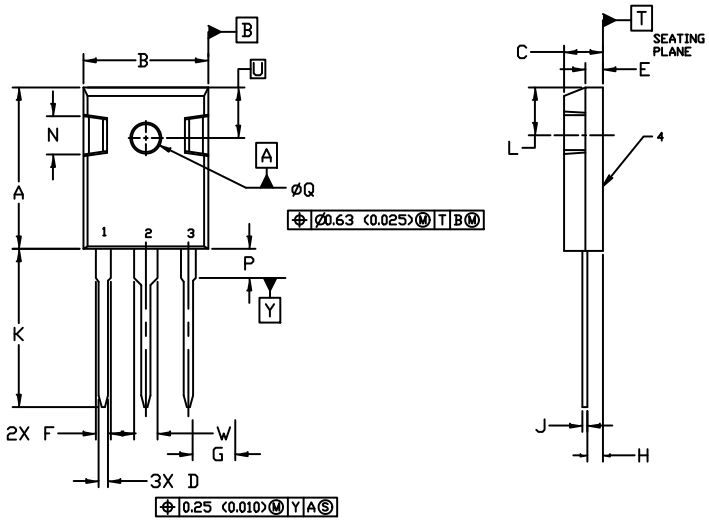
DOCUMENT NUMBER:	98ASB42643B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOT−93 (TO−218)	PAGE 1 OF 1



SCALE 1:1

TO−247
CASE 340L
ISSUE G

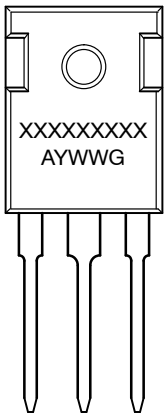
DATE 06 OCT 2021



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER

	MILLIMETERS		INCHES	
DIM	MIN.	MAX.	MIN.	MAX.
A	20.32	21.08	0.800	0.830
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	----	4.50	----	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

GENERIC MARKING DIAGRAM*



STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 6:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TO−247**	**PAGE 1 OF 1**

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