LDO Regulator - 400 mA, Best-in-Class Dropout, with Bias Rail

Product Preview

T30LMPSR132, T30LAPSR132

The T30LxPSR132 is an ultra−fast, **400 mA** bias rail LDO with market−leading dropout voltage (**20 mV @ full load**). Due to its advanced CMOS process, the T30LxPSR132 offers ultra−fast dynamic response and provides very stable output voltage with 1% accuracy over full temperature range. The device also features high PSRR across frequency range and ultra−low noise optimized for noise sensitive applications. The T30LxPSR132 very low bias current makes the device suitable for battery powered applications. The minimum recommended output capacitance (1 x 2.2 μF) and the low profile, WLCSP6 0.99 mm x 0.65 mm, 0.35P Chip Scale package is ideal for space−constrained applications.

Features

- Best−in−Class Dropout: 20 mV (typ.) at 400 mA
- ±1% Accuracy over −40°C to 125°C Temp. Range
- High PSRR across Frequency Range
  - 75 dB at 1 kHz
  - 38 dB at 100 kHz
- Very Low Bias Input Current of Typ. 85 μA
- Ultra Low Noise, 7.5 μV_{RMS} Typ.
- Excellent Load Transient Performance
- Input Voltage Range: up to 2.2 V
- Bias Voltage Range: up to 3.3 V
- Output Voltage Range: 0.5 V to 1.8 V (Fixed), Resolution 25 mV
- 1.2 V Logic Level Enable Input Compatibility

Typical Applications

- Battery−powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

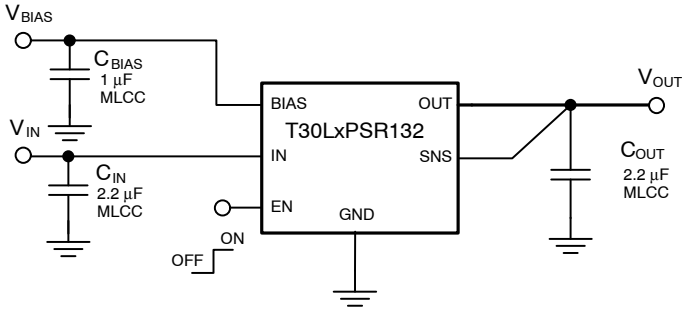
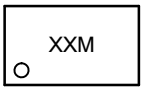


Figure 1. Typical Application Schematics

This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

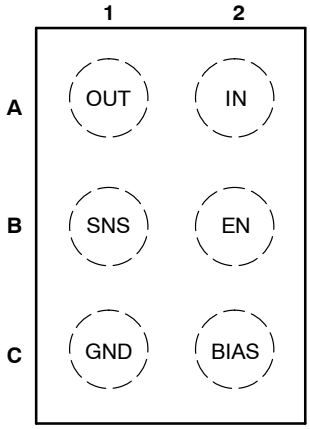
WLCSP6 0.99x0.65x0.29
CASE 567ZT

MARKING DIAGRAM



XX = Specific Device Code
M = Month Code

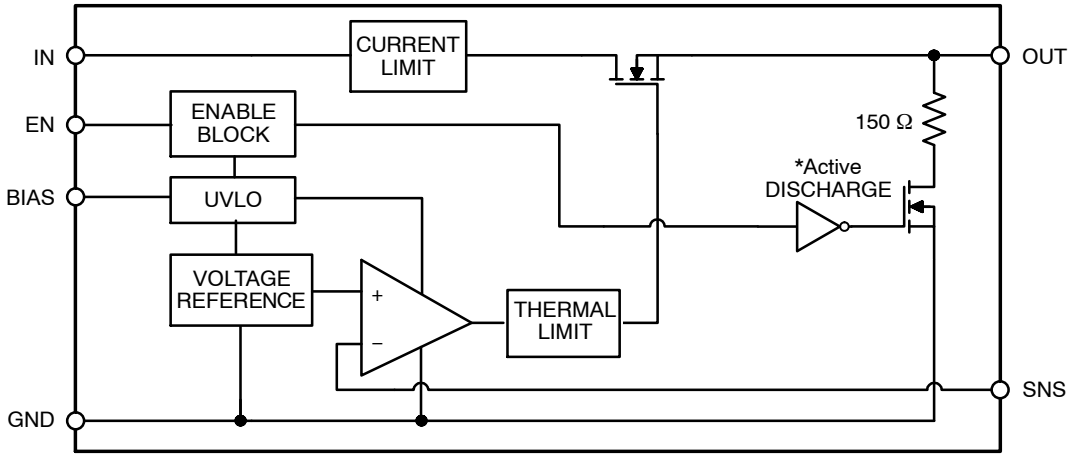
PIN CONNECTIONS



Top View

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.



*Active output discharge function is present only in “A” and “C” option devices.

Figure 2. Simplified Schematic Block Diagram − Fixed Version

PIN FUNCTION DESCRIPTION

Pin No. WLCSP6	Pin Name	Description
A1	OUT	Regulated Output Voltage pin
A2	IN	Input Voltage Supply pin
B1	SNS	Output voltage Sensing Input. Connect to Output on the PCB to output the voltage corresponding to the part version.
B2	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
C1	GND	Ground pin
C2	BIAS	Bias voltage supply for internal control circuits.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 2.5	V
Output Voltage	V_{OUT}	−0.3 to (V_{IN}+0.3) ≤ 2.5	V
Chip Enable, Bias and SNS Input	V_{EN}, V_{BIAS}, V_{SNS}	−0.3 to 3.6	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	750	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114.
   ESD Charged Device Model tested per JS−002−2018.
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WLCSP6 1.145 mm x 0.75 mm Thermal Resistance, Junction-to-Air (Note 3)	$R_{\theta JA}$	69	°C/W

3. This junction−to−ambient thermal resistance under natural convection was derived by thermal simulations based on the JEDEC JESD51 series standards methodology. Only a single device mounted at the center of a high_K (2s2p) 80 mm x 80 mm multilayer board with 1-ounce internal planes and 2-ounce copper on top and bottom. Top copper layer has a dedicated 1.6 mm^2 copper area.

ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 125°C$; V_{BIAS} = 2.7 V or (V_{OUT} + 1.6 V), whichever is greater, $V_{IN} = V_{OUT(NOM)}$ + 0.1 V, I_{OUT} = 1 mA, V_{EN} = 1 V, C_{IN} = 2.2 μF, C_{OUT} = 2.2 μF, C_{BIAS} = 1 μF, unless otherwise noted. Typical values are at T_J = +25°C. Min/Max values are for $-40°C \le T_J \le 125°C$ unless otherwise noted. (Note 4)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage Range			V_{IN}	V_{OUT} + V_{DO}		2.2	V
Operating Bias Voltage Range			V_{BIAS}	(V_{OUT} + 1.50) ≥ 2.5		3.3	V
Undervoltage Lock−out	V_{BIAS} Rising Hysteresis		$UVLO_{(BIAS)}$		2.1 0.1		V
	V_{IN} Rising Hysteresis		$UVLO_{(IN)}$		0.8 x V_{OUT} 0.1		
Output Voltage Accuracy	$-40°C \le T_J \le 85°C$, $V_{OUT(NOM)}$ + 0.1 V ≤ V_{IN} ≤ $V_{OUT(NOM)}$ +1.0 V, 2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 3.3 V, 1 mA < I_{OUT} < 400 mA		V_{OUT}	−0.8		+0.8	%
Output Voltage Accuracy	$-40°C \le T_J \le 125°C$, $V_{OUT(NOM)}$ + 0.1 V ≤ V_{IN} ≤ $V_{OUT(NOM)}$ + 1.0 V, 2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 3.3 V, 1 mA < I_{OUT} < 400 mA		V_{OUT}	−1		+1	%
V_{IN} Line Regulation	$V_{OUT(NOM)}$ + 0.1 V ≤ V_{IN} ≤ 2.2 V		$Line_{Reg}$		0.01		%/V
V_{BIAS} Line Regulation	2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 3.3 V		$Line_{Reg}$		0.01		%/V
Load Regulation	I_{OUT} = 1 mA to 400 mA		$Load_{Reg}$		1		mV
V_{IN} Dropout Voltage	I_{OUT} = 400 mA (Note 5)		V_{DO}		20	50	mV
V_{BIAS} Dropout Voltage	I_{OUT} = 400 mA, $V_{IN} = V_{BIAS}$ (Notes 5, 6)		V_{DO}		1.1	1.5	V
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$		I_{CL}	530	660	800	mA
SNS Pin Operating Current			I_{SNS}		0.1	0.5	μA
Bias Pin Quiescent Current	V_{BIAS} = 3.3 V, I_{OUT} = 0 mA		I_{BIASQ}		85	130	μA
Bias Pin Disable Current	V_{EN} ≤ 0.325 V		$I_{BIAS(DIS)}$		0.5	TBD	μA
Input Pin Disable Current			$I_{VIN(DIS)}$		0.5	TBD	μA
EN Pin Threshold Voltage	EN Input Voltage “H”		$V_{EN(H)}$	0.77			V
	EN Input Voltage “L”		$V_{EN(L)}$			0.325	
EN Pull Down Current	V_{EN} = 3.3 V		I_{EN}		0.3	TBD	μA
Power Supply Rejection Ratio	V_{IN} to V_{OUT}, $V_{IN} = V_{OUT}$ + 0.1 V, I_{OUT} = 150 mA, C_{OUT} = 2.2 μF, 0201	f = 100 Hz	$PSRR(V_{IN})$		75		dB
		f = 1 kHz			80		
		f = 10 kHz			60		
		f = 100 kHz			40		
	V_{BIAS} to V_{OUT}, $V_{IN} = V_{OUT}$ + 0.1 V	f = 1 kHz	$PSRR(V_{BIAS})$		80		dB
Output Noise Voltage	$V_{IN} = V_{OUT}$ + 0.1 V, f = 10 Hz to 100 kHz	I_{OUT} = 10 mA	V_N		9		μV_{RMS}
		I_{OUT} = 400 mA			7.5		
Thermal Shutdown Threshold	Temperature increasing				160		°C
	Temperature decreasing				140		
Output Discharge Pull−Down	V_{EN} ≤ 0.325 V, V_{OUT} = 0.5 V, Active Discharge Version Only		R_{DISCH}		150		Ω

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.
6. For fixed output voltages below 1.5 V, V_{BIAS} dropout does not apply due to a minimum Bias operating voltage of 2.5 V.

ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 125°C$; V_{BIAS} = 2.7 V or (V_{OUT} + 1.6 V), whichever is greater, $V_{IN} = V_{OUT(NOM)}$ + 0.1 V, I_{OUT} = 1 mA, V_{EN} = 1 V, C_{IN} = 2.2 μF, C_{OUT} = 2.2 μF, C_{BIAS} = 1 μF, unless otherwise noted. Typical values are at T_J = +25°C. Min/Max values are for $-40°C \le T_J \le 125°C$ unless otherwise noted. (Note 4)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Delay time	From assertion of V_{EN} to output voltage increase	'A' option	t_{DELAY}		120		μs
		'C' option			120		
Rise time	V_{OUT} rise from 10% to 90% $V_{OUT(NOM)}$	'A' option	t_{RISE}		21		
		'C' option			100		
Turn−On Time	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$	'A' option	t_{ON}		140		
		'C' option			220		

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.
6. For fixed output voltages below 1.5 V, V_{BIAS} dropout does not apply due to a minimum Bias operating voltage of 2.5 V.

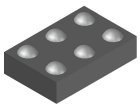
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Device	Output Voltage	Marking	Option	Package	Shipping†
T30LxPSR132CFCT080T2G (**Consult onsemi sales**)	0.80 V	TBD	Output Active Discharge, Slow Turn−On Slew Rate	WLCSP6 Case 567ZT (Pb−Free) UBM: 210 μm Bump Type: (98.2% Sn/1.8% Ag) Plate	10,000 / Tape & Reel
T30LxPSR132CFCT120T2G (**Consult onsemi sales**)	1.20 V	TBD	Output Active Discharge, Slow Turn−On Slew Rate		

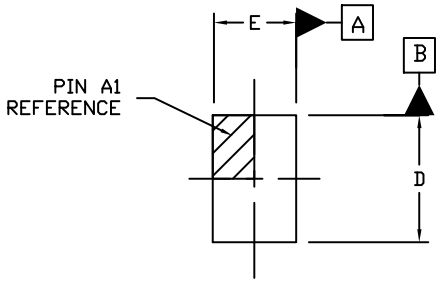
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

7. To order other package and voltage variants, please contact your **onsemi** sales representative.

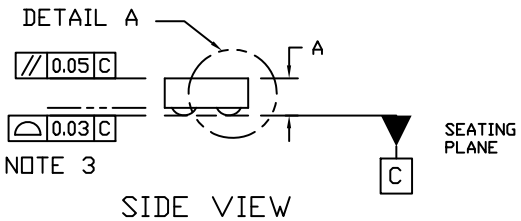


WLCSP6 0.99x0.65x0.29
CASE 567ZT
ISSUE B

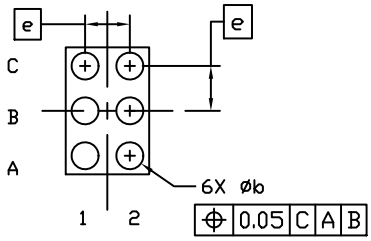
DATE 21 JAN 2022



TOP VIEW

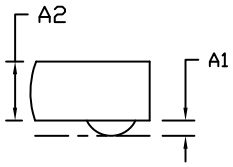


SIDE VIEW



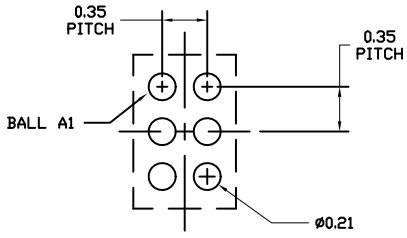
BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM BALL DIAMETER, PARALLEL TO DATUM C.



DETAIL A

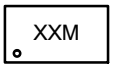
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.250	0.290	0.330
A1	0.040	0.060	0.080
A2		0.23 REF	
b	0.180	0.210	0.240
D	0.940	0.990	1.040
E	0.600	0.650	0.700
e		0.35 BSC	



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON27334H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
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