

SIS5452

+5 Volt Electronic Fuse

The SIS5452 is a cost effective, resettable fuse. It is designed to buffer the load device from excessive input voltage which can damage sensitive circuits. It also includes an overvoltage clamp circuit that limits the output voltage during transients but does not shut the unit down, thereby allowing the load circuit to continue operation.

Features

- Integrated Power Device
- 33 mΩ Typical
- Internal Charge Pump
- Internal Undervoltage Lockout Circuit
- Internal Overvoltage Clamp
- These are Pb-Free Devices and are RoHS Compliant

Typical Applications

- Mother Board
- Hard Drives
- Fan Drives



ON Semiconductor®

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4 AMP, 5 VOLT ELECTRONIC FUSE



WDFN10
CASE 522AA

MARKING DIAGRAM

Pin	Function
1-5	SOURCE
6	NC
7	ILIMIT
8	Enable/Fault
9	dv/dt
10	GND
11 (flag)	VCC

XXX = Specific Device Code

A = Assembly Location

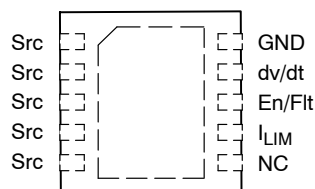
Y = Year

W = Work Week

▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENTS



(Top View)

ORDERING INFORMATION

Device	Features	Marking	Package	Shipping†
SIS5452MT1TXG	Thermal Latching $V_{\text{clamp}} = 5.85 \text{ V}$, $I_{\text{LIM}} = 2.1 \text{ A @ } 18 \text{ }^{\circ}\text{C}$	S52	WDFN10 (Pb-Free)	3000 / Tape & Reel
SIS5452MT1TWG	Thermal Latching $V_{\text{clamp}} = 5.85 \text{ V}$, $I_{\text{LIM}} = 2.1 \text{ A @ } 18 \text{ }^{\circ}\text{C}$	S52W	WDFN10 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

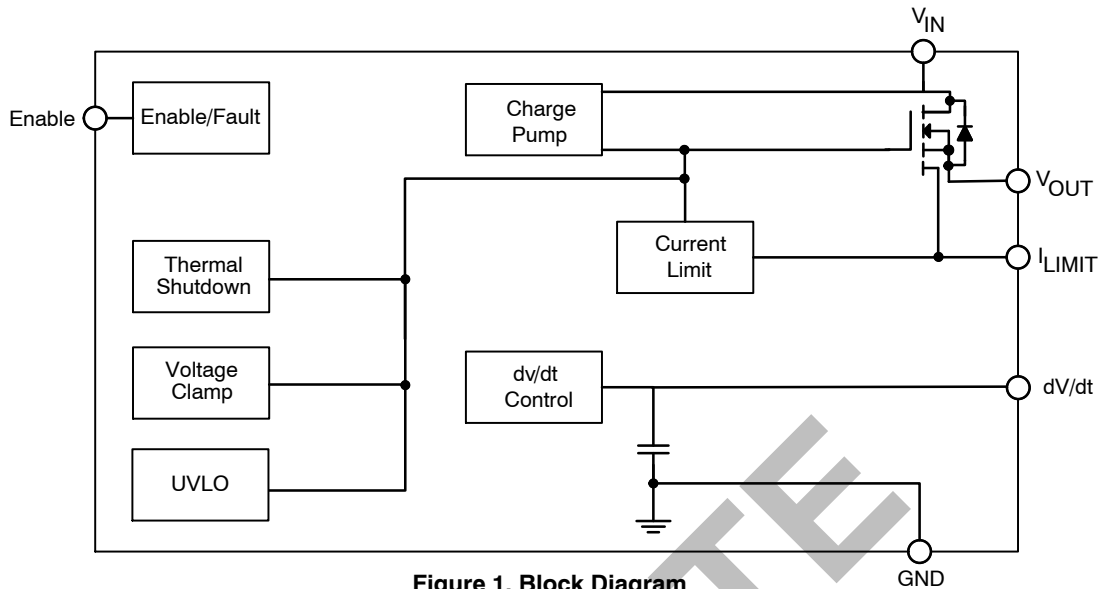


Figure 1. Block Diagram

Table 1. FUNCTIONAL PIN DESCRIPTION

Pin	Function	Description
1–5	Source	This pin is the source of the internal power FET and the output terminal of the fuse.
7	I_{Limit}	A resistor between this pin and the source pin sets the overload and short circuit current limit levels.
8	Enable/Fault	The enable/fault pin is a tri-state, bidirectional interface. It can be used to enable or disable the output of the device by pulling it to ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin will go to an intermediate state to signal a monitoring circuit that the device is in thermal shutdown. It can also be connected to another device in this family to cause a simultaneous shutdown during thermal events.
9	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over a period of 1.4 ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left open.
10	Ground	Negative input voltage to the device. This is used as the internal reference for the IC.
11 (belly pad)	V_{CC}	Positive input voltage to the device.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage, operating, steady-state (V_{CC} to GND, Note 1)	V_{IN}	–0.6 to 10	V
Thermal Resistance, Junction-to-Air 0.1 in ² copper (Note 2) 0.5 in ² copper (Note 2)	θ_{JA}	154 93	°C/W
Thermal Resistance, Junction-to-Lead (Pin 1)	θ_{JL}	49	°C/W
Thermal Resistance, Junction-to-Case	θ_{JC}	20	°C/W
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (operating) Max transient power	P_{max}	1.3 25	W W
Operating Temperature Range (Notes 3 and 4)	T_J	–40 to 150	°C
Nonoperating Temperature Range	T_J	–55 to 155	°C
Lead Temperature, Soldering (10 Sec)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Negative voltage will not damage device provided that the power dissipation is limited to the rated allowable power for the device.
2. 1 oz copper, double-sided FR4.
3. Thermal limit is set above the maximum thermal rating. It is not recommended to operate this device at temperatures greater than the maximum ratings for extended periods of time.
4. Exceeding T_J will thermally destroy the FET. See AND9042/D.

SIS5452

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted: $V_{CC} = 5.0\text{ V}$, $C_{in} = 2.2\text{ }\mu\text{F}$, $C_L = 70\text{ }\mu\text{F}$, dv/dt pin open, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
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POWER FET

Delay Time (enabling of chip to $I_D = 100\text{ mA}$ with 1 A resistive load) (Note 9)	T_{dly}		200		μs
ON Resistance (Note 5) $T_J = 140^\circ\text{C}$ (Note 6)	$R_{DS(on)}$	25	33 60	50	$\text{m}\Omega$
Off State Output Voltage ($V_{CC} = 8\text{ V}_{dc}$, $V_{GS} = 0\text{ V}_{dc}$, $R_L = 100\text{ k}\Omega$) (Note 9)	V_{off}		10	200	mV
Output Capacitance ($V_{DS} = 5\text{ V}_{DC}$, $V_{GS} = 0\text{ V}_{DC}$, $R_L = \infty$)	C_{out}		230		pF
Continuous Current ($T_A = 25^\circ\text{C}$, 0.5 in ² pad) (Note 6) ($T_A = 80^\circ\text{C}$, minimum copper, Maximum Transient Dissipated Power 25W)	I_D I_D		4.0 1.7		A

THERMAL LATCH

Shutdown Temperature (Note 6)	T_{SD}	150	175	200	$^\circ\text{C}$
Thermal Hysteresis (Decrease in die temperature for turn on, does not apply to latching parts)	T_{Hyst}		45		$^\circ\text{C}$

UNDER/OVERVOLTAGE PROTECTION

V_{OUT} Maximum ($V_{CC} = 10\text{ V}$)	SIS5452	$V_{out-clamp}$	5.5	5.85	6.25	V
Undervoltage Lockout (Turn on, Voltage Going High)		V_{UVLO}	2.2	2.5	2.8	V
UVLO Hysteresis (Note 9)		V_{Hyst}		0.145		V

CURRENT LIMIT

Kelvin Short Circuit Current Limit (Note 7)	SIS5452 ($R_{Limit} = 18\text{ }\Omega$)	I_{LIM}	1.6	2.1	2.8	A
Overload Current Limit (Note 7)	SIS5452 ($R_{Limit} = 18\text{ }\Omega$)	I_{LIM}		2.7		A

dv/dt CIRCUIT

Output Voltage Ramp Time (Enable to $V_{OUT} = 4.7\text{ V}$) (Note 9)	t_{slew}	0.70	1.4	2.4	ms
Maximum Capacitor Voltage	V_{max}			V_{CC}	V

ENABLE/FAULT

Logic Level Low (Output Disabled)	V_{in-low}	0.35	0.58	0.81	V
Logic Level Mid (Thermal Fault, Output Disabled)	V_{in-mid}	0.82	1.4	1.95	V
Logic Level High (Output Enabled) (Note 9)	$V_{in-high}$	1.96	2.2	2.50	V
High State Maximum Voltage	V_{in-max}	2.51	3.3	5.2	V
Logic Low Sink Current ($V_{enable} = 0\text{ V}$)	I_{in-low}		-12	-20	μA
Logic High Leakage Current for External Switch ($V_{enable} = 3.3\text{ V}$)	$I_{in-leak}$			1.0	μA
Maximum Fanout for Fault Signal (Total number of chips that can be connected to this pin for simultaneous shutdown)	Fan			3.0	Units

TOTAL DEVICE

Bias Current (Operational) (Note 9)	I_{Bias}		400	750	μA
Bias Current (Shutdown) (Note 9)	I_{Bias}		100		μA
Minimum Operating Voltage (Notes 6 and 8)	V_{min}			2.8	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Pulse test: Pulse width 300 μs , duty cycle 2%.
- Verified by design.
- Refer to explanation of short circuit and overload conditions in application note AND8140/D.
- Device will shut down prior to reaching this level based on actual UVLO trip point.
- Guaranteed by characterization or design.

SIS5452

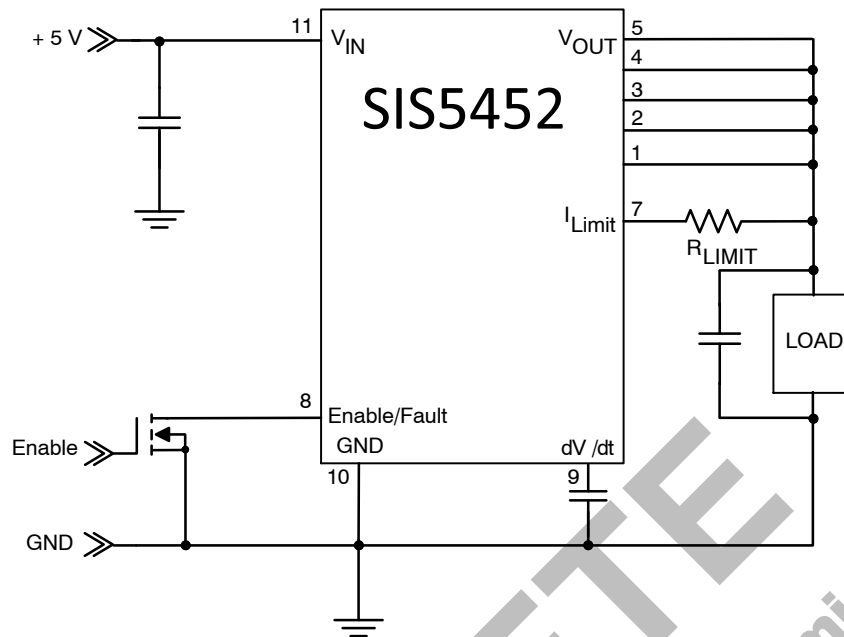


Figure 2. Application Circuit with Direct Current Sensing

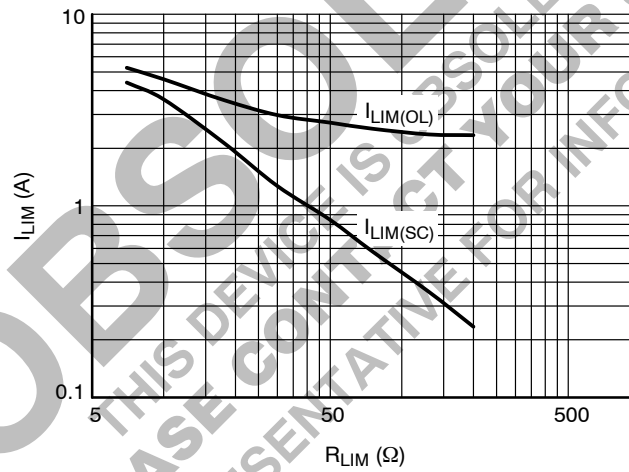


Figure 3. I_{LIM} Direct vs. R_{LIM}

SIS5452

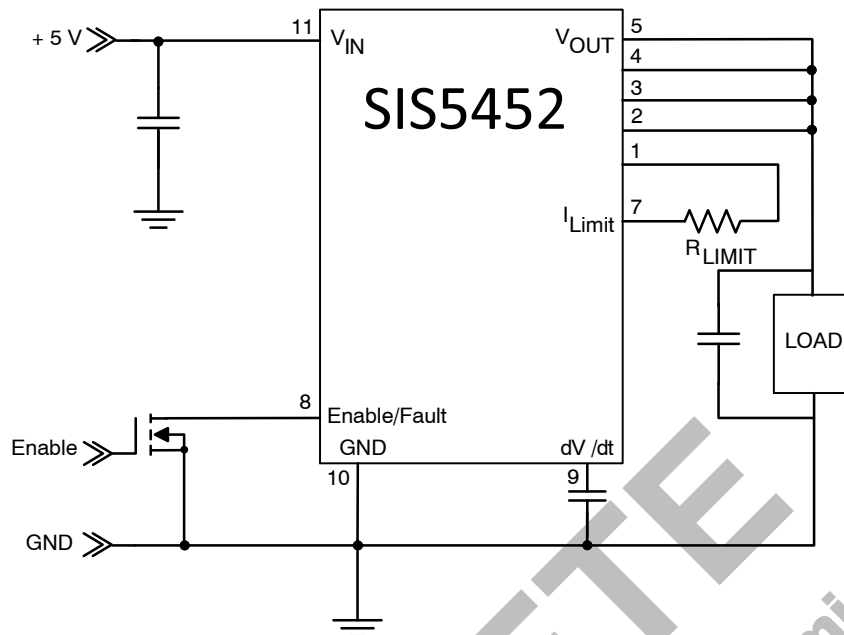


Figure 4. Application Circuit with Kelvin Current Sensing

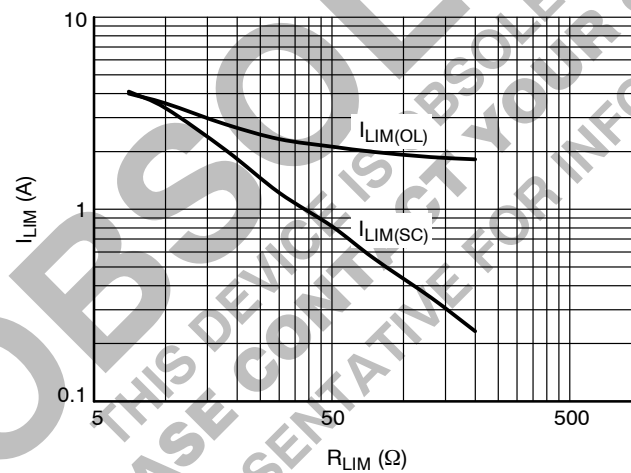


Figure 5. I_{LIM} Kelvin vs. R_{LIM}

APPLICATION INFORMATION

Overvoltage Clamp

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the input voltage exceeds the specified Vout maximum for the device, the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for many seconds, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device.

Undervoltage Lockout

The undervoltage lockout circuit uses a comparator with hysteresis to monitor the input voltage. If the input voltage drops below the specified level, the output switch will be switched to a high impedance state.

dv/dt Circuit

The dv/dt circuit brings the output voltage up under a linear, controlled rate regardless of the load impedance characteristics. An internal ramp generator creates a linear ramp, and a control circuit forces the output voltage to follow that ramp, scaled by a factor.

The default ramp time is approximately 1.4 ms. This can be modified by adding an external capacitor at the dv/dt pin. This pin includes an internal current source of approximately 1 μ A. Since the current level is very low, it is important to use a ceramic cap or other low leakage capacitor. Aluminum electrolytic capacitors are not recommended for this circuit.

The ramp time from 0 to the nominal output voltage can be determined by the following equation, where t is in seconds:

$$t_{0-5} = 1.25 \text{ E6} \cdot C_{\text{ext}}$$

Where:

C is in Farads

t is in Seconds

Any time that the unit shuts down due to a fault, enable shut-down, or recycling of input power, the timing capacitor will be discharged and the output voltage will ramp from 0 at turn on.

Enable/Fault

The Enable/Fault Pin is a multi-function, bidirectional pin that can control the output of the chip as well as send information to other devices regarding the state of the chip. When this pin is low, the output of the fuse will be turned off. When this pin is high the output of the fuse will be turned-on. If a thermal fault occurs, this pin will be pulled low to an intermediate level by an internal circuit.

To use as a simple enable pin, an open drain or open collector device should be connected to this pin. Due to its tri-state operation, it should not be connected to any type of logic with an internal pullup device.

If the chip shuts down due to the die temperature reaching its thermal limit, this pin will be pulled down to an intermediate level. This signal can be monitored by an external circuit to communicate that a thermal shutdown has occurred. If this pin is tied to another device in this family (NIS5232), a thermal shutdown of one device will cause both devices to disable their outputs. Both devices will turn on once the fault is removed for the auto-retry devices.

For the latching thermal device, the outputs will be enabled after the enable pin has been pulled to ground with an external switch and then allowed to go high or after the input power has been recycled. For the auto retry devices, both devices will restart as soon as the die temperature of the device in shutdown has been reduced to the lower thermal limit. The thermal options are listed in the ordering table.

Thermal Protection

The SIS5452 includes an internal temperature sensing circuit that senses the temperature on the die of the power FET. If the temperature reaches 175°C, the device will shut down, and remove power from the load. Output power can be restored by either recycling the input power or toggling the enable pin. Power will automatically be reapplied to the load for auto-retry devices once the die temperature has been reduced by 45°C.

The thermal limit has been set high intentionally, to increase the trip time during high power transient events. It is not recommended to operate this device above 150°C for extended periods of time.

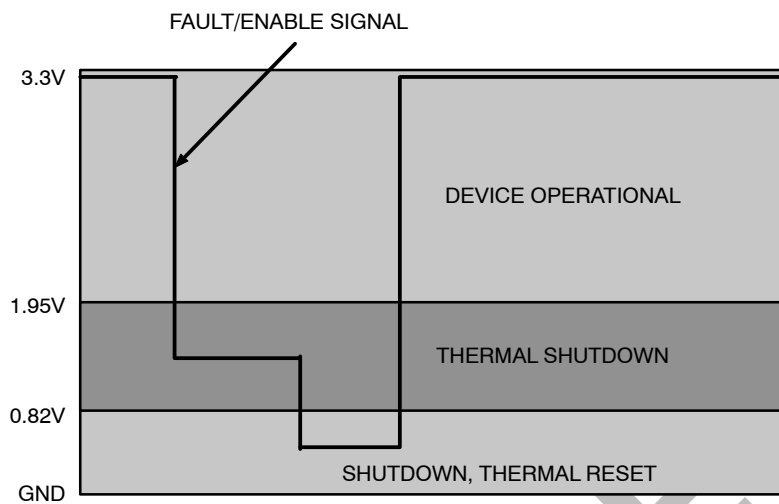


Figure 7. Enable/Fault Signal Levels

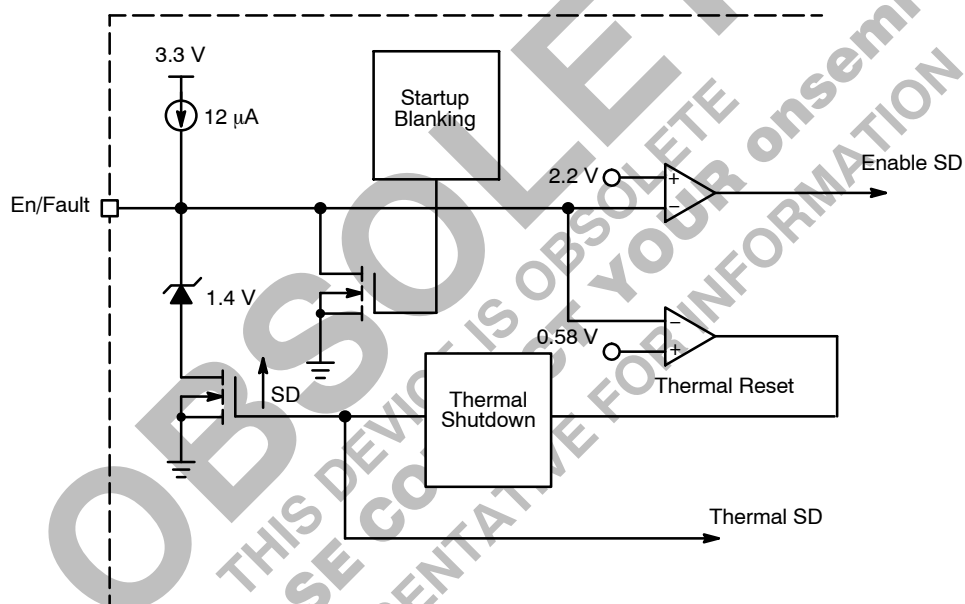
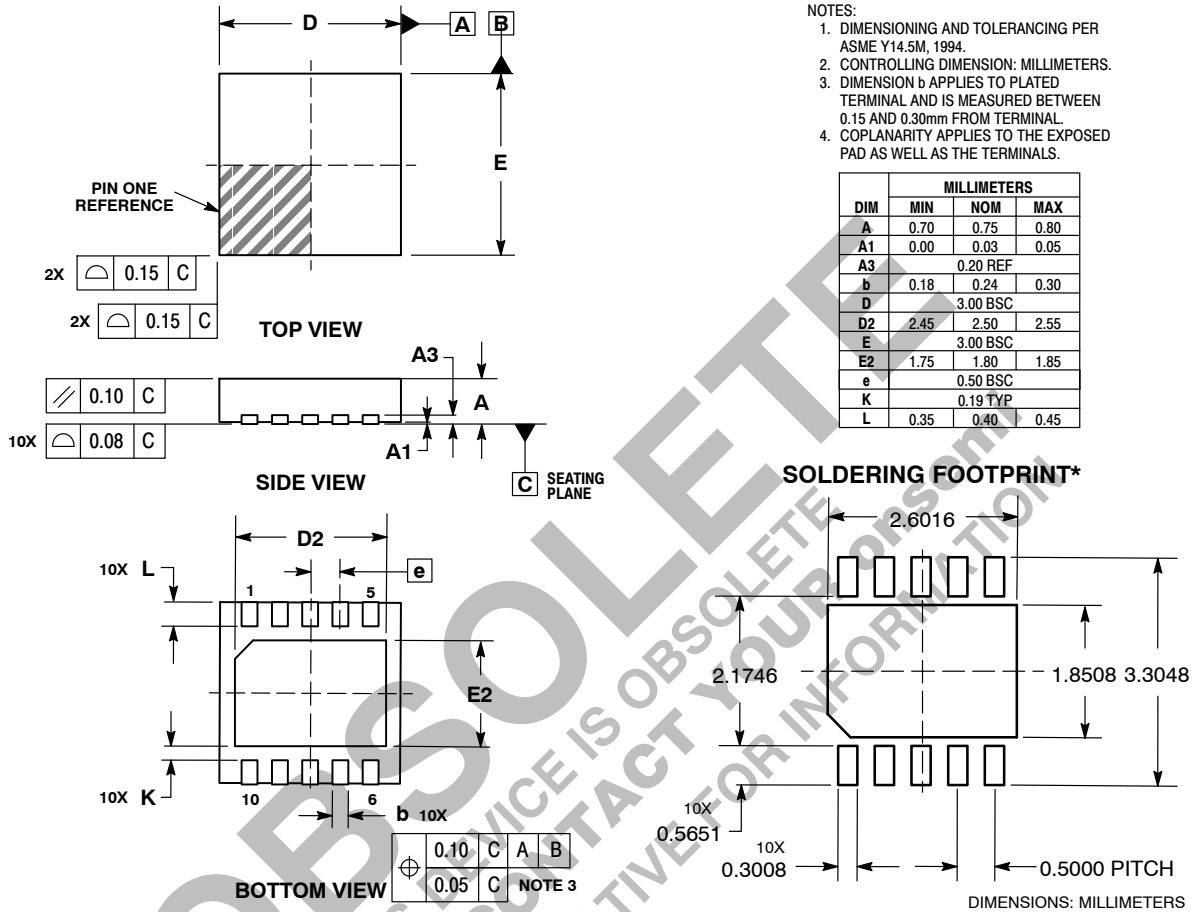


Figure 8. Enable/Fault Simplified Circuit

PACKAGE DIMENSIONS

WDFN10, 3x3, 0.5P
CASE 522AA
ISSUE A



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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