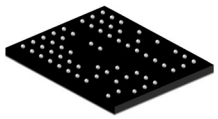
Ultra-low Power Radio for Hearing Aids and Earbuds

RSL20



WLCSP62 3.004x2.419
CASE 567XF

Introduction

RSL20 is an Ultra-Low Power 2.4 GHz radio supporting Bluetooth® Audio specifically designed for use in high-performance hearing aids and earbuds.

RSL20 is a versatile Bluetooth Audio radio. It is a Dual-Mode Bluetooth device as it supports both Bluetooth Classic (BR and EDR) and Bluetooth Low Energy, with compliance with the Bluetooth Core Specification Version 5.3. RSL20 supports LE audio with Auracast™, the new Bluetooth Low Energy broadcast audio streaming feature and Unicast streaming. It also supports Bluetooth Classic profiles such as A2DP and HFP.

RSL20 includes a Near Field Magnetic Induction (NFMI) RF front-end, capable of streaming audio content and control messages at very low power and low latency. The NFMI link can be used to support binaural algorithms and True Wireless Stereo (TWS).

RSL20 is optimized for audio applications. It includes a two-channel DMIC input and one audio Output Driver. The Audio Sink Clock Counters (ASCC) and the Asynchronous Sample Rate Converter (ASRC) can be used to synchronize audio with a peer Bluetooth device, or with the other earpiece of a true wireless stereo system, or with an external DSP.

The Arm® Cortex®-M33 processor is included on RSL20. It is a 32-bit RISC processor providing support for general processing and interfacing to external components. It comes with security features such as the Arm CryptoCell™ CC-312 and the Arm® TrustZone®.

Two LPDSP32 DSPs are included. The LPDSP32 is an open-programmable dual-Harvard 32-bit DSP, optimized for low power audio signal processing. Also, the Neural Network Accelerator allows the RSL20 to perform neural network computations in a highly efficient and flexible way.

MARKING DIAGRAM

WLCSP62

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
CCC = Country of Origin

ORDERING INFORMATION

Device	Package	Shipping†
NCH-RSL20-103WC61-ABG	WLCSP	5000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Key Features

- **Dual Mode Bluetooth**: support Bluetooth Classic and Bluetooth Low Energy (BLE) with LE Audio.
- **RF Operation**: Bluetooth 5.3 certified baseband and protocol stack.
- **Best in class power consumption metrics**: for audio streaming use cases and advertising or connection modes.
- **Integrated NFMI Front-end**: supports low-power and low-latency ear-to-ear communication as well as audio forwarding for TWS applications.
- **Arm Cortex-M33 Processor**: a complete subsystem used to host customer's applications, clocked up to 48 MHz.
- **Dual LPDSP32 DSP cores**: highly cycle-efficient, programmable cores that use a 32-bit fixed-point, dual-MAC, dual-Harvard architecture, clocked up to 48 MHz. Also used to host CODECs such as LC3, SBC, G722 and CVSD.
- **Neural Network Accelerator (NNA)**: a configurable hardware accelerator dedicated to support neural networks with high energy efficiency.
- **Flexible Power Management Unit**: supports direct supply from ZnAir and Li-Ion battery.
- **Versatile Memory Architecture**: a total of 587 kB of memory, shared between the Arm Cortex-M33 Processor, the LPDSP32s and the NNA, among others.
- **2 MB of on-chip NVM (Non Volatile Memory)**: available to store the customer's application code as well as the protocol stack.
- **Programmable Flexibility**: the LPDSP32 and the Arm Cortex-M33 Processor are fully open-programmable. Algorithms and features can be developed based on customer's needs.
- **Highly-integrated SoC**: the 4 processing cores (NNA, 2 x LPDSP32 and Arm Cortex-M33 Processor) are complemented with NVM, RAM memory, the 2.4 GHz RF front-end, the NFMI front-end, the Power Management Unit, as well as peripherals and interfaces to form a complete System on Chip (SoC).
- **Asynchronous Sample Rate Converter (ASRC)**: provides a mean of synchronizing the audio sample rate between a peer Bluetooth device, an external DSP or the other earpiece of a true wireless stereo system and the RSL20 when audio data are transferred.
- **Audio Sink Clock Counters**: Can be used to measure the timing of the frame periods of the audio samples shared over the RSL20 radio link and the audio sampling rate of an external companion DSP chip.
- **Highly Configurable Interfaces**: one PCM interface, one I2C interface, one I3C® interface, two SPI interfaces, two UART interfaces, up to 16 GPIOs (General-Purpose Input/Output) and 8 LSAD (Low-Speed A/D converters) inputs.
- **High Throughput Communication Interface**: applications executed on the Arm Cortex-M33 processor can be debugged through the SWJ-DP, which can be configured for either serial wire or JTAG debug port communications. Each LPDSP32 core is supported by a 4-wire JTAG debug port that is mapped onto the GPIOs. It is also possible to use SWD (two wire debug) for the Arm Cortex-M33 and the two LPDSP32 cores at the same time.
- **Audio IO interface**: allows to directly connect digital microphones and multiple types of speakers to RSL20.
- **Flexible Clocking**: Two crystal oscillators, based on a 48 MHz crystal and on a 32 kHz crystal and two internal RC oscillators are available on RSL20 to offer many clocking configurations.
- **Cybersecurity Platform**: The Cortex-M33 processor comes with the Arm® TrustZone® CryptoCell 312, which is a security subsystem providing root of trust (RoT) and cryptographic services for the RSL20.
- **Integrated Development Environment (IDE)**: a graphical user interface with the capabilities to edit, build and debug applications supporting Visual Studio Code and CMake. It is the main programming interface for the Software Development Kit (SDK).
- **Complete C-development tool chain for the LPDSP32**. Includes a C-compiler, an instruction set simulator, an assembler/disassembler, a linker and the IDE debugger integrated in the RSL20 SDK.
- **Sample Codes**: The SDK includes several sample applications and libraries to demonstrate key features of RSL20.
- **Pb-Free**, Halogen Free/BFR Free and are RoHS Compliant

ARCHITECTURE OVERVIEW

Detailed Block Diagram

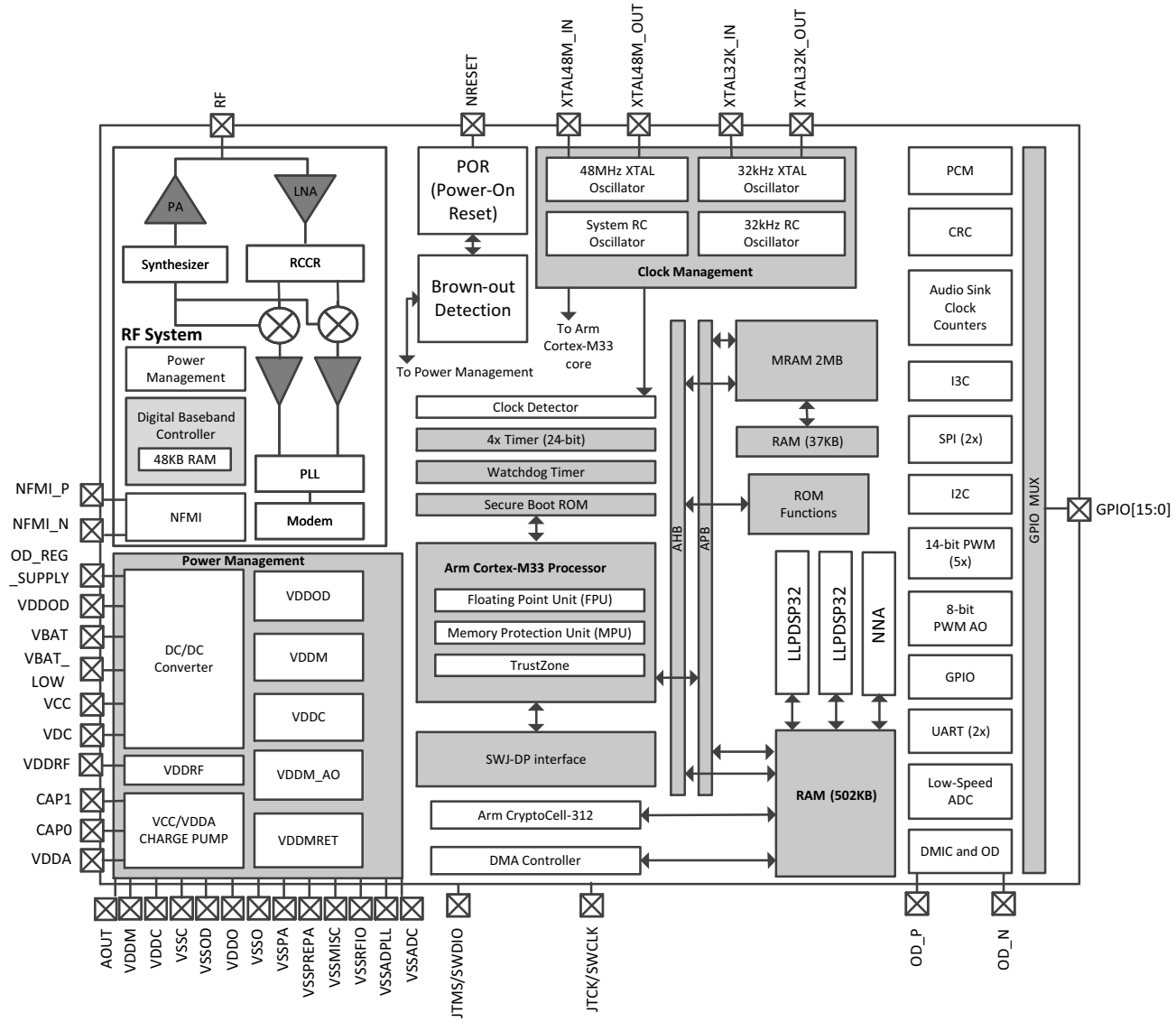


Figure 1. RSL20 Detailed Block Diagram

Arm Cortex-M33 Processor

The Cortex-M33 32-bit Armv8-M processor is designed for embedded applications that require high performance, power efficiency and security. The processor has many features to execute high performance applications such a Floating-Point Unit (FPU), DSP extensions and Memory Protection Unit (MPU).

Secure debug is done through the SWJ-DP which combines JTAG-DP and SW-DP for either JTAG probe or Serial Wire Debug (SWD) connection.

Integrated IoT Cybersecurity Platform

The Arm Cortex-M33 processor with TrustZone Armv8-M security extensions forms the basis of the security platform. The Arm CryptoCell-312 allows for end-to-end product security, with Secure Boot with Root of Trust, secure lifecycle management, secure key management, a true random number generator (TRNG), and application and data encryption using symmetric or asymmetric cryptography. Arm TrustZone enables secure software access control.

LPDSP32

RSL20 contains two LPDSP32 processors. Each is a low-power, programmable DSP that uses a dual-Harvard, dual-MAC architecture to efficiently process 32-bit signal data.

RSL20's two LPDSP32 processors are included in the design to efficiently support digital signal processing tasks, such as audio codecs, low-delay path audio processing, and deep learning applications using the Neural Network Accelerator (NNA). Each LPDSP32 core is identified by its core ID, either 0 or 1.

RSL20's two LPDSP32 processors are contained within two separate DSP subsystems.

Each DSP subsystem contains the following:

- LPDSP32 processor
- LPDSP32 program memory loop cache
- Interrupt controller
- Arm Cortex-M33 sub-system and other LPDSP32 command generator

Debugging each LPDSP32 core is supported by a 4-wire JTAG debug port that is mapped onto the GPIOs. It is also possible to use SWD (two wire debug) for the Arm Cortex-M33 and the two LPDSP32 cores at the same time.

Software development on the LPDSP32 is done in C.

NNA

The Neural Network Accelerator (NNA) is a hardware accelerator block that allows complex neural networks to run in an energy efficient manner. The accelerator can execute a single layer of a fully populated or sparsely populated neural network in a single task without any processor intervention. Layers with up to 1023 inputs and 1023 outputs are supported.

The NNA contains 16 multipliers, 16 accumulators, 16 input registers and 16 coefficient registers. It includes input and coefficient "fetchers" that, once configured, manage the data and coefficients memory access automatically. Support for coefficient compression/decompression and pruning is included and help minimize the amount of coefficient needed.

Memory Structure and Instances

The memory systems provided by RSL20 are constructed using a number of memories (RAM instances), memory buses, memory controllers, and memory arbiters. These memories are all addressable by the Arm Cortex-M33 processor, DMA and MRAM copier, while part of the memory is addressable by the baseband controller, the LPDSP32s, and the NNA.

The memory space is subdivided into four main segments:

- The program memory used for storing and/or executing code on the Arm Cortex-M33 processor and/or the LPDSP32
- The data memory used for storing data and intermediate variables of the Arm Cortex-M33 processor and/or the LPDSP32
- The Arm Cortex-M33 processor subsystem's peripheral registers
- The Arm Cortex-M33 processor's system registers (not shown in this documentation)

MEMORY INSTANCES

Instance Name	Size	Type	Description
Boot ROM (Program ROM)	18 KB	ROM	Responsible for ensuring that an RSL20 device correctly performs a controlled boot sequence allowing application code to execute. Takes into account the possible life cycle states of the device, the active power modes, and any required security functionality.
MRAM	2 MB	NVM	Shared between the Arm Cortex-M33 processor and the LPDSP32. The MRAM is used for storing program code for all three processor cores, user data, and calibration settings.
BB_DRAM	48 KB	RAM	Acts as the exchange memory between the Arm Cortex-M33 core and the baseband controller. The BB DRAM is subdivided into 3 logical instances (BB_DRAM0 – BB_DRAM2), respectively 32, 8 and 8KB in size, which are independently attributed to the Arm Cortex-M33 processor or the baseband controller via dynamic arbitration.
Data RAM	176 KB	RAM	Shared between the BT stack software and the user application. The DRAM is subdivided into 9 logical instances (DRAM0 – DRAM8, respectively 8, 8, 32, 32, 32, 16, 16, 16,and 16 KB in size).
LPDSP32 ARAM	128 KB	RAM	Shared between the Arm Cortex-M33 processor and the LPDSP32. The LPDSP32 ARAM is subdivided into 8 logical instances of 16 KB (DSS_ARAM0 – DSS_ARAM7), which are independently attributed to the Arm Cortex-M33 processor or the LPDSP32 via dynamic arbitration.
LPDSP32 BRAM	32 KB	RAM	Shared between Arm Cortex-M33 processor and the LPDSP32. The LPDSP32 BRAM is subdivided into 4 logical instances of 8 KB each (DSS_BRAM0 – DSS_BRAM3).
LPDSP32 P0RAM	128 KB	RAM	Shared between the Arm Cortex-M33 processor and the LPDSP32. The LPDSP32 P0RAM is subdivided into 8 logical instances of 16 KB each (DSS_P0RAM0 – DSS_P0RAM7), which are independently attributed to the ARM CORTEX-M33 PROCESSOR or the LPDSP32 via dynamic arbitration.

MEMORY INSTANCES (continued)

Instance Name	Size	Type	Description
LPDSP32 P1RAM	32 KB	RAM	Shared between the Arm Cortex-M33 processor and the LPDSP32. The LPDSP32 P1RAM is subdivided into 2 logical instances of 16 KB (DSS_P1RAM0 – DSS_P1RAM1) that are independently attributed to the Arm Cortex-M33 processor or the LPDSP32 via dynamic arbitration.
LPDSP32 PM0 emulated	160 KB	Emulated memory space	Emulated program memory space of the LPDSP32 #0 onto the Arm Cortex-M33 core memory space for loading LPDSP32 programs.
LPDSP32 PM1 emulated	160 KB	Emulated memory space	Emulated program memory space of the LPDSP32 #1 onto the Arm Cortex-M33 core memory space for loading LPDSP32 programs.
LPDSP32 DM emulated	16 MB	Emulated memory space	Emulated data memory space of the LPDSP32s and NNA onto the Arm Cortex-M33 core memory space for loading and retrieving data.

Audio IO (DMIC / OD)

RSL20 provides one Digital Microphone (DMIC) two-channel input and one Output Driver (OD) one-channel output.

The DMIC and OD always have the same sampling rate, but the DMIC interface and OD can be clocked with different clock sources, namely DMICCLK and ODCLK. This allows having different clock frequencies on the DMIC and OD bit streams.

External Interface

- **General-Purpose Input/Output**: RSL20 contains 16 general purpose input/output (GPIO) pads that can be configured for the following purposes:
  - To support the sensor and communications interfaces (see list below), output clocks, and other I/Os.
  - As general-purpose I/Os controllable from the Arm Cortex-M33 core.
- **PCM Interface**: RSL 20 includes a highly-configurable pulse code modulation (PCM) interfaces that can be used to stream signal, control and configuration data in and out of the device. The PCM interface can be configured in I2S mode.
- **SPI Interface**: RSL20 includes two Serial Peripheral Interfaces (SPIs). Each SPI interface supports single and dual I/O modes, as well as the ability to add two additional I/O pins in a quad I/O mode. The SPI interfaces support controller/peripheral configuration as well as half/full duplex mode.
- **UART Interface**: RSL20 includes two general-purpose UART interfaces provides support for communicating with devices that use standard UART and RS-232 transmission protocols.
- **LSAD**: RSL20 includes Low-Speed A/D Converters (LSAD) used to sample voltages that typically change slowly, such as the voltage associated with a potentiometer-based volume control. The LSADs provide an analog to digital conversion of up to eight signals, from a combination of four internal signals and four external signals.
- **I2C Interface**: RSL20 includes an I2C interface which is compatible with the UM10204 I2C specification. I2C uses a two-wire interface that includes a bidirectional clock line (SCL) and a bidirectional data line (SDA). The I2C interface is typically used for communication with external sensors and storage devices, and as control signals for radios.
- **I3C Interface**: RSL20 includes an I3C interface which is compatible with the Improved Inter-IC Bus Specification from the MIPI Alliance. The I3C interface uses a two-wire interface including a bidirectional clock line (SCL) and bidirectional data line (SDA). The I3C interface is designed to ease sensor system design architectures in mobile wireless products by providing a fast, low cost, low power, two-wire digital interface for sensors.
- **PWM drivers**: RSL20 contains five pulse-width modulator (PWM) drivers, each of which can be configured to generate a single output signal with a specified period and duty cycle.

RF Front-end

The RSL20 RF front-end is an ultra-low-power 2.4 GHz RF transceiver, which handles data rates up to 3 Mbit/s. It supports several wireless protocols, such as:

- Bluetooth Classic PHY layer version 5.3, including Basic Rate (BR) and Enhanced Data Rate (EDR) 2 Mbps and 3 Mbps
- Bluetooth Low Energy PHY layer version 5.3, including 2 Mbps, both Long Range (LR) and Direction Finding options
- Flexible PHY with data rates ranging from several kbps up to 3Mbps and programmable baseband settings for supporting proprietary modes (e.g. FSK with programmable pulse shape and modulation index, π/4 DQPSK & D8PSK)

The RSL20 RF front-end implements a flexible architecture relying on a software programmable sequencer executing generic controlling sequences, and software programmable TX and RX packet handlers responsible for the data processing.

Bluetooth Dual Mode Baseband Controller

RSL20 handles the Bluetooth protocol through the Bluetooth stack, which is executed in software on the Arm Cortex-M33 processor, and the baseband controller, which is implemented in hardware.

The Bluetooth stack is in charge of the upper protocol layers, while the baseband controller is responsible for the low level operations and the data processing. From a network protocol layer point of view, the Bluetooth stack is responsible for scheduling, configuring, and managing the Bluetooth events, while the baseband controller processes the actual events, controls the RF front-end, and handles real time bit stream processing.

From one side, the baseband controller communicates with the RF front-end through an internal SPI interface for TX/RX programming and radio FSM control, along with internal signals for the TX/RX data/clock and IQ data.

From the other side, the hardware communicates with the Arm Cortex-M33 processor, through exchange memory, interrupts, and hardware registers.

NFMI Subsystem

The NFMI subsystem includes the necessary digital and analog hardware to implement a low latency, low power solution for transmitting audio or control data from ear to ear.

The NFMI subsystem provides low power / low latency half duplex transmission of audio signals on short distances (typically ear-to-ear), at a configurable carrier frequency, using OQPSK (Offset Quadrature Phase Shift Keying) modulation.

In a system with a pair of RSL20 devices, one RSL20 is the central device, initiating communication, and the other is the peripheral, waiting for that initiation of communication.

Peripherals

- **Activity counters**: used for accurately measuring the execution time of processes between user-defined start and stop points. This helps firmware developers to analyze how actively the Arm Cortex-M33 processor, the MRAM memory, and the DSPs are being used by a user application.
- **Asynchronous Sample Rate Converter (ASRC)**: provides a means of synchronizing the audio sample rate between the radio and a local source or sink, for transferred audio data.
- **Audio Sink Clock Counters (ASCC)**: allow to measure the timing of a connected external device's clock, the internal DMIC and output driver sampling rate, the internal RCCLK (divided by 64), or STANDBYCLK. More specifically, the audio sink clock counters allow to measure the number of clock cycles for a configurable audio sink clock within a configurable synchronization frame.
- **Cyclic Redundancy Check (CRC) generator**: provides support for two standard cyclic redundancy check algorithms (CRC-CCITT and CRC-32, defined by the IEEE 802.3 Ethernet standard). The calculated outputs from this generator can be employed by a user application to ensure data integrity of communications and non-volatile memory information.
- **Direct Memory Access (DMA) controller**: includes 12 independent configurable channels, that allow background transfers to and from memories and components on the peripheral bus, without any processor intervention. This allows the processors to be used for other computational needs while enabling high speed sustained transfers between the components and the memories.
- **MRAM Copier**: copy data from the MRAM into any DMA-accessible memory or the CRC block.
- **Timers**: The RSL20 system provides five timers, including the SysTick timer from the Arm Cortex-M33 core, and four general-purpose timers
- **Watchdog timer**: a safety mechanism for resetting a system that has malfunctioned. This safety system uses a timer that must be periodically renewed by writing into a specific register.
- **Time of flight**: is designed to enable measurement of the time it takes for certain operations to complete, especially RF operations.

Power Management Unit (PMU)

The PMU of RSL20 is a critical component of the system. Supplied power has significant effects on the RF and on other types of system performance. The PMU includes the following components:

- **VCC/VDDA DC-DC Converter, VDDA Charge Pump, VDDA LDO, VCC LDO**: This block is used to reduce the battery voltage from high value (up to 4.5 V) to a lower voltage value VCC and to generate a doubled voltage VDDA with high efficiency.
  This configuration can also be inverted, where the high value supply is regulated down to VDDA level and the charge pump is used to halve VDDA to generate VCC. This converter is used as input for the different voltage regulators that supply the RF front-end, the digital block, and the analog blocks such as the LSAD and non-volatile memory.
  The DC-DC block usually uses two external components for charge transferring and filtering, and two external components for the charge pump.
- **VDDRF LDO**: Regulated power supply for the RF front-end.
- **Output Driver Voltage Regulator (VDDOD)**: This block is used to provide a regulated power supply to the output drivers. The VDDOD regulator is supplied from

the OD_REG_SUPPLY pin.
If the application uses an external supply to overdrive the VDDOD pin, the regulator needs to be disabled to save current.

- **Digital Supply Voltages (VDDC, VDDM)**: VDDC and VDDM each provide a regulated voltage derived from the VCC pin (DC-DC converter). These two regulated voltages are trimmable. To guarantee a correct operation of their respective regulators, a voltage margin of at least 50 mV must be respected between the output of VCC and each regulator. The VDDC block provides a regulated voltage for the digital core (standard-cells-VDDC). The VDDM block provides a regulated voltage for the RAM, ROM and pads (VDDM). Note that the VDDM and VDDC regulators are not shown in the Power Management Unit figure below.

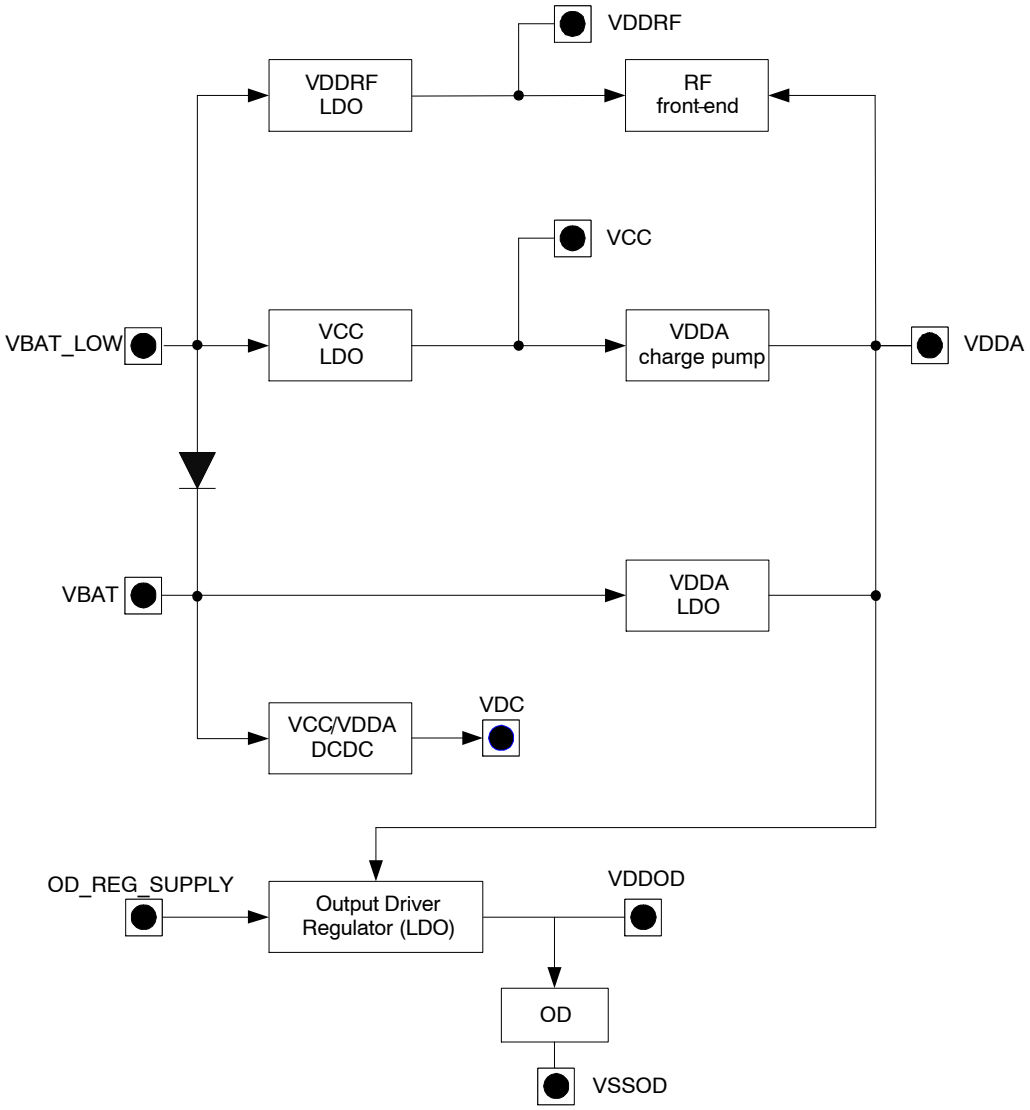


Figure 2. Power Management Unit

Clock Generation and Distribution

SYSCLK is the primary RSL20 system clock and can be generated from:

- The internal startup system RC clock (RCCLK)
- The XTAL 48 MHz (XTAL48M) from the RF front-end optionally divided to 16 MHz (RFCLK)
- The STANDBYCLK (coming from XTAL32K or from the RC32K)
- The SWCLK pad from the SWJ-DP
- EXTCLK, provided at a selected GPIO

The clock generation module provides clocks for the digital blocks, many of which have configurable prescalers based on SYSCLK.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit	Notes
VBAT		4.95	V	Battery supply voltage
VBAT_LOW		2.2	V	Battery supply voltage
VDDO		1.98	V	IO supply voltage
VDDA		1.98	V	MRAM, RF front-end and analog block supply
OD_REG_SUPPLY		1.98	V	Supply voltage for the regulator of the OD. Max voltage should be equal or less than VDDA level.
VDDOD		OD_REG_SUPPLY	V	Supply for the output driver
VCC		0.99	V	DC-DC, LDO or charge pump output voltage for RF front-end and analog blocks supply voltages
VDDC		0.88	V	Digital supply voltage
VDDM		0.88	V	Memories supply voltage
VDDRF		1.32	V	Supply voltage for the low voltage part of RF front-end
VSSRF	−0.3		V	RF front-end ground
VSSA	−0.3		V	Analog ground
VSSO	−0.3		V	IO ground
VSSC	−0.3		V	Digital ground
Vin	VSSO − 0.3 V	VDDO + 0.3 V	V	Digital input pin voltage
T_functional	−40	55	°C	Functional temperature range. Operation at this temperature range requires the use of a 32 kHz XTAL, when wakeup from sleep mode is based on the internal counter.
T_storage	−40	85	°C	Storage temperature range

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

WARNING: Class 2 ESD Sensitivity: HBM ±2 kV on all pins, except XTAL48M_OUT which only withstands 1 kV (JESD22_A114_B)
CDM ESD compliance on all pins: 250 V (JESD22-A114)

Table 2. OVERALL OPERATING CONDITIONS

Parameter	Min	Typ	Max	Unit	Notes
VBAT	0.9	1.25	4.5	V	Supply voltage, measured at the VBAT pin. (Note 1)
VBAT_LOW	0.9	1.2	2	V	Supply voltage measured at VBAT_LOW (Note 1)
VDDRF	0.84	0.85	1.2	V	Supply voltage for RF front-end.
OD_REG_SUPPLY	1.0	1.7	1.8	V	Supply voltage for the VDDOD regulator. The max voltage should be equal or lower than VDDA voltage level.
VDDO	0.9	1.25	1.8	V	I/O voltage
VCC	0.81	0.84	0.99	V	Internal supply voltage used to supply the analog blocks, VDDC and VDDM supply voltages. (Note 2)
VDDA	1.62	1.68	1.98	V	Internal supply voltage used to supply the NVM, the analog blocks and the RF front-end. (Note 2)
VDDM	0.72	0.76	0.88	V	Internal memory supply voltage, generated from VCC
VDDC	0.45	0.76	0.88	V	Internal digital supply voltage, generated from VCC
VDDOD	0.8		OD_REG_SUPPLY	V	Internal supply for the audio output driver
System Clock		16	48	MHz	System clock frequency (referred as SYSCLK in the RSL20 documentation)

1. This value depends on the power management configurations. See section POWER MANAGEMENT CONFIGURATIONS for more details.
2. The generation of VCC and VDDA depends on the power management configuration. See Section POWER MANAGEMENT CONFIGURATIONS for more details.

Table 3. RSL20 ELECTRICAL SPECIFICATIONS
Unless otherwise noted, the specifications mentioned in the table below are valid at 25 °C, and for all supply mode described in section POWER MANAGEMENT CONFIGURATIONS

VCC GENERATION (THROUGH LDO OR DCDC)

Parameter	Min	Typ	Max	Unit	Notes
VCC voltage trimming range	0.75	0.84	1.065	V	
VCC voltage headroom (VBAT_LOW – VCC_TRIM)	30			mV	LDO mode
VCC trimming step		5		mV	
VCC Load current		10	50	mA	At 0.85 V output voltage, LDO and DCDC modes
VCC Load regulation		0.2	0.7	mV/mA	Iload 1 mA to 50 mA, LDO and DCDC modes
VCC Line regulation			2	mV/V	At 5 mA load, LDO mode
VCC Line regulation	–5		5	mV/V	At 5 mA load, DCDC mode
Voltage ripple			10	mVrms	Nominal components, voltage and load, LDO and DCDC modes

VDDA GENERATION (THROUGH LDO OR DCDC)

Parameter	Min	Typ	Max	Unit	Notes
VDDA voltage trimming range	1.5	1.68	2.13	V	
VDDA trimming step		10		mV	
VDDA Load current		10	50	mA	At 1.7 V output voltage, LDO and DCDC modes
VDDA Load regulation		0.3	0.7	mV/mA	Iload 1 mA to 50 mA, LDO and DCDC modes
VDDA Line regulation			3	mV/V	At 5 mA load, LDO mode
VDDA Line regulation	–5		5	mV/V	At 5 mA load, DCDC mode
Voltage ripple			10		Nominal components, voltage and load, LDO and DCDC modes

VDDA/VCC CHARGE PUMP: VDDA GENERATION FROM VCC (2*), VCC GENERATION FROM VDDA (/2)

Parameter	Min	Typ	Max	Unit	Notes
Charge pump clock Frequency		100	1000	kHz	50% duty cycle
Charge pump output current			10	mA	VCC = 0.90 V, fclk = 100 kHz
Charge pump maximum output current			25	mA	VCC = 0.95 V, fclk = 1000 kHz
Charge pump (x2) Zout		7	10	Ω	VDDA generation, VCC = 0.95 V, fclk = 1000 kHz, Iload 1 mA to 25 mA
Charge pump (/2) Zout		1.5	2	Ω	VCC generation, VDDA = 1.90 V, fclk = 1000 kHz, Iload 1 mA to 25 mA

VDDRF LDO

Parameter	Min	Typ	Max	Unit	Notes
VDDRF voltage trimming range	0.75	0.85	1.385	V	
VDDRF voltage headroom (VBAT_LOW – VR_TRIM)	30			mV	
VDDRF trimming step		5		mV	
VDDRF Load current		5	25	mA	At 0.85 V output voltage
VDDRF Load regulation		0.4	1.1	mV/mA	Iload 1 mA to 25 mA

VDDRF LDO (continued)

Parameter	Min	Typ	Max	Unit	Notes
VDDRF Line regulation	−10		10	mV/V	At 5 mA load, with constant VCC and VDDA voltages
PSRR	35	45			@10 kHz, at 10 mA load, VBAT_LOW = 1.2 V, VDDRF = 0.85 V.

VDDC REGULATOR

Parameter	Min	Typ	Max	Unit	Notes
VDDC voltage trimming range	0.3		0.91	V	
VDDC trimming step		2.5		mV	
VDDC Load current			10	mA	
VDDC Load regulation			0.1	mV/mA	1 mA < Iload < 10 mA
VDDC Line regulation			10	mV/V	At 5 mA load
PSRR	30			dB	@1 kHz, unloaded vs VCC

VDDM REGULATOR

Parameter	Min	Typ	Max	Unit	Notes
VDDM voltage trimming range	0.3		0.91	V	
VDDM trimming step		2.5		mV	
VDDM Load current			10	mA	
VDDM Load regulation			0.1	mV/mA	1 mA < Iload < 10 mA
VDDM Line regulation			10	mV/V	At 5 mA load
PSRR	30			dB	@1 kHz, unloaded vs VCC

VDDOD REGULATOR

Parameter	Min	Typ	Max	Unit	Notes
Trimming range	0.8		2.06	V	
Trimming steps		20		mV	
VDDOD load current			25	mA	OD_REG_SUPPLY > 1.2 V
			10	mA	OD_REG_SUPPLY < 1.2 V
VDDOD Load regulation		0.8	2	mV/mA	1 mA < Iload < 10 mA
VDDOD Line regulation		1.5	5	mV/V	At 5 mA load
PSRR	10			dB	VDDA = 1.9 V, OD_REG_SUPPLY = 1.9 V, output load = 15 mA, output voltage VDDOD = 1.5 V, spot frequency = 1 kHz

NOTE: We recommend to enable the VDDOD regulator. It improves the PSRR when large transient currents are drawn elsewhere in the application using RSL20 and gives an audio output level that is independent of the battery voltage. Alternatively, a clean supply available in the application can be used on OD_REG_SUPPLY.

RF FRONT-END: GENERAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit	Notes
RF Input Impedance		50		Ω	Single ended
Input Reflection Coefficient			−8	dB	All channels
Data Rate FSK / MSK / GFSK		1000	3000	kbps	OQPSK as MSK

RF FRONT-END: CRYSTAL AND CLOCK SPECIFICATIONS (48 MHz XTAL)

Parameter	Min	Typ	Max	Unit	Notes
48 MHz XTAL Frequency		48		MHz	Fundamental
48 MHz XTAL Start-up Time		200	700	μs	Typical value achieved with XTAL_TRIM setting < 110, with 48 MHz XTAL (ESR = 50, C_L = 6 pF).
48 MHz XTAL Frequency Tolerance	−20		+20	ppm	The frequency tolerance specified here must be guaranteed over the operating temperature range of end customer's device application. Aging of the 48 MHz XTAL must be taken into account. Please refer to Application Note called "XXX".
Equivalent series resistance (ESRXTAL)	20		80	Ω	
Differential equivalent load capacitance (CLXTAL)*	4.0	6.0	10.0	pF	

* The effective differential capacitance (XTAL and parasitics) must be <1 pF, the remaining being capacitance to ground (parasitic completed by on-chip load capacitance).

RF FRONT-END: SYNTHESIZER SPECIFICATIONS

Parameter	Min	Typ	Max	Unit	Notes
Frequency Range	4720		5000	MHz	Supported carrier frequencies
Frequency Resolution			1500	Hz	

RF FRONT-END: RECEIVE AND TRANSMIT MODES SPECIFICATIONS

Parameter	Min	Typ	Max	Unit	Notes
RX Sensitivity, 1 Mbps, Bluetooth Low Energy		−98		dBm	0.1% BER, LE1M modulation
RX Sensitivity, 2 Mbps, Bluetooth Low Energy		−95		dBm	0.1% BER, LE2M modulation
RX Sensitivity, Bluetooth Low Energy LR 125 kbps		−104		dBm	0.1% BER, LE Long Range
RX Sensitivity, Bluetooth Low Energy LR 500 kbps		−100		dBm	0.1% BER, LE Long Range
RX Sensitivity, BT BR 1 Mbps		−95		dBm	0.1% BER, GFSK 1 Mbps modulation
RX Sensitivity, BT EDR 2 Mbps		−93		dBm	0.01% BER, π/4-DQPSK 2 Mbps modulation
RX Sensitivity, BT EDR 3 Mbps		−85		dBm	0.01% BER, 8-DPSK 3 Mbps modulation
Transmit Power Range	−35		See Max TX Power Tables of the POWER MANAGEMENT CONFIGURATIONS section.	dBm	
Transmit Power Step Size		1		dB	
Max TX Power		+10		dBm	Bluetooth Low Energy. See Notes 3, 4 and 5.
		+10		dBm	BR, GFSK. See Notes 3, 4, and 5.
		+10		dBm	EDR2, DPSK Peak. See Notes 3, 4, 5 and 6.
		+7		dBm	EDR2, DPSK RMS (Pseudo Random Payload). See Notes 3, 4, 5 and 6.
		+10		dBm	EDR3, DPSK Peak. See Notes 3, 4, 5 and 6.
		+7		dBm	EDR3, DPSK RMS (Pseudo Random Payload). See Notes 3, 4, 5 and 6.

RF FRONT-END: RECEIVE AND TRANSMIT MODES SPECIFICATIONS (continued)

Parameter	Min	Typ	Max	Unit	Notes
TX Power Accuracy		±1		dBm	TX power accuracy can be enhanced when a specific calibration is made on the end-application's PCB. The calibration routines are available from RSL20 SDK 1.3.
Power in 1st Harmonic [no external filter]		−40		dBm	0 dBm output power setting
Power in 2nd Harmonic [no external filter]		−26		dBm	0 dBm output power setting
Power in 3rd Harmonic [no external filter]		−49		dBm	0 dBm output power setting
Power in 4th Harmonic [no external filter]		−53		dBm	0 dBm output power setting
Power in 1st Harmonic [with external filter]		−65		dBm	0 dBm output power setting, 50 Ω load
Power in 2nd Harmonic [with external filter]		< −67		dBm	0 dBm output power setting, 50 Ω load
Power in 3rd Harmonic [with external filter]		< −67		dBm	0 dBm output power setting, 50 Ω load
Power in 4th Harmonic [with external filter]		< −67		dBm	0 dBm output power setting, 50 Ω load
Power in 1st Harmonic [no external filter]		−22		dBm	10 dBm output power setting
Power in 2nd Harmonic [no external filter]		−12		dBm	10 dBm output power setting
Power in 3rd Harmonic [no external filter]		−28		dBm	10 dBm output power setting
Power in 4th Harmonic [no external filter]		−36		dBm	10 dBm output power setting
Power in 1st Harmonic [with external filter]		−50		dBm	10 dBm output power setting, 50 Ω load
Power in 2nd Harmonic [with external filter]		−65		dBm	10 dBm output power setting, 50 Ω load
Power in 3rd Harmonic [with external filter]		< −67		dBm	10 dBm output power setting, 50 Ω load
Power in 4th Harmonic [with external filter]		< −67		dBm	10 dBm output power setting, 50 Ω load

3. The TX Power values indicated in the data sheet is the power available at the RSL20 RF output pin. A TX Power drop due to the external filter needs to be taken into account. An external filter is required to conform with ETSI/FCC compliance. Also, the RX sensitivity is measured at the RSL20 RF pin.
4. TX Power limitations depends on the RSL20 Power Management Configuration. See Section "POWER MANAGEMENT CONFIGURATION AND POWER CONSUMPTIONS" for more details.
5. TX power in other locations of the data sheet are provided in RMS, unless specified differently.
6. In order to comply with the In Band Emission (IBE) requirements of the Bluetooth specification, the TX power in EDR2 and EDR3 should be limited to +3 and −3 dBm respectively. The RSL20 includes a HW mechanism that can limit the TX power for EDR2 and EDR3 at a value selected in the RSL20's application.
7. Harmonics measured using BLE 1 Mbps on 2440 MHz.

LSAD

Parameter	Min	Typ	Max	Unit	Notes
LSAD Resolution	8	12	14	bits	Depends on frequency setting
Input Signal Level	0		1.8	V	If VDDA < 1.8 V, the maximum value is equal to VDDA
Channel Sampling Frequency		5		kHz	For a sample clock of 100 kHz (20 cycles per measurement)

LSAD (continued)

Parameter	Min	Typ	Max	Unit	Notes
lsad_clk Frequency		100	128	kHz	
INL	–2		+2	mV	
DNL	–1		+1	mV	
Input Impedance	1			MΩ	

IOs

Parameter	Min	Typ	Max	Unit	Notes
Voltage level of high input		0.5	0.65	V	For low VDDO (HIGH_VDDO = 0). See Note 8
		0.75	1	V	For high VDDO (HIGH_VDDO = 1). See Note 8
Voltage level of low input	0.2	0.35		V	For low VDDO (HIGH_VDDO = 0). See Note 8
	0.4	0.55		V	For high VDDO (HIGH_VDDO = 1). See Note 8
Voltage level of high output	VDDO – 0.4			V	
Voltage level of low output			0.4	V	
Drive Strength	2			mA	1x drive strength
	4			mA	2x drive strength
Weak pull up		100		kΩ	
Strong pull up		10		kΩ	
Weak pull down		250		kΩ	

8. Use HIGH_VDDO = 0 for VDDO < 1.2 V
   Use HIGH_VDDO = 1 for VDDO > 1.2 V

NFMI

Parameter	Min	Typ	Max	Unit	Notes
Carrier frequency	8	10.56	22	MHz	OQPSK (Offset Quadrature Phase Shift Keying) modulation.
RX & TX LPF cutoff frequency	2.3	2.5	2.7	MHz	Adjustable using a 6-bit trimming (50 kHz resolution)
RX & TX LPF frequency trimming step		39.25	65	kHz	LPF Cutoff frequency trimming steps.
RX & TX BPF cutoff frequency trimming step		2	3	MHz	BPF Cutoff frequency trimming steps.
Power amplifier differential output voltage	0.3	3	14	Vpp	For typical NFMI coil parameters (10.6 MHz, 3.7 μH, 5 kΩ)
Power amplifier drive control		16		step	For output power control
LNA gain	60	80		dB	Total LNA gain
LNA input referred noise		6	10	μVrms	Entire operating frequency range
Interference rejection		40		dB	For typical resonator parameters (10.6 MHz, 3.7 μH, 5 kΩ), interferer frequency at 6.8 MHz
System bandwidth	500			kHz	for a data rate of 1 Mbps
Antenna peak voltage	–7		7	V	
Ear to ear audio Latency		5		ms	20 kHz sampling frequency, block mode

NVM (MRAM) SPECIFICATIONS

Parameter	Min	Typ	Max	Unit	Notes
Data retention period	20			Yr	
Data endurance	100,000			Cycles	A cycle corresponds to programming and erasing a bit cell.
Standby magnetic immunity	±550			Oe	No read/write. BER < 1E-7.
Active magnetic immunity, read.	±900			Oe	For BER < 1E-6
Active magnetic immunity, write.	±250			Oe	For BER < 1E-6

AUDIO OUTPUT STAGE

Parameter	Min	Typ	Max	Unit	Notes
Output resistance	–	2	–	Ω	ILOAD = 1 mA. High and Low side combined.
Output Dynamic Range	98	100	–	dB	High impedance load (>1 kΩ), XSDM0 mode
	–	95	–	dB	Low impedance speaker mode, 36R load, XSDM0 mode
	90	95	–	dB	High impedance load (>1 kΩ), OD_DELAY mode
Peak THD+N	–	−62	−55	dB	@ 1 kHz, high impedance load, (>1 kΩ), XSDM0 mode
	–	−59		dB	@ 1 kHz, low impedance speaker mode, 36R load, XSDM0 mode
	–	−71	−66	dB	@ 1 kHz, high impedance load (>1 kΩ), OD_DELAY mode
Output noise RMS	–	–	7.5	μV	At 1.25 V VDDOD; scales linearly with VDDOD.
Output Bandwidth	–	–	24	kHz	
Maximum output current	–	–	25	mA	This current can be drawn but with degraded audio quality.
Power supply rejection ratio (PSRR)		−85		dB	Using VDDOD regulator

NOTE:
- Output stage specifications are A-weighted, bandwidth 100 Hz-fs/2, sampling frequencies 16/32/48 kHz, with VDDOD = 1.25 V
- The output stage will operate at 0.9 V but with degraded specifications (the achievable acoustic output level will be lowered).
- When the radio front-end block is enabled, the Dynamic Range is reduced by ~6 dB. At TX power higher than +8 dBm, Dynamic Range reduced by ~9 dB
- When the NFMI block is enabled, the Dynamic Range is reduced by ~6 dB.

32 kHz CRYSTAL OSCILLATOR (XTAL32K)

Parameter	Min	Typ	Max	Unit	Notes
Output frequency		32.768		kHz	depends on xtal parameters
Start-up time		0.2	1	s	VBAT applied to stabilization
Temperature coefficient			200	ppm/°C	−40 °C to 85 °C
			100	ppm/°C	−10 °C to 50 °C
Internal load Capacitance			25.2	pF	Internal capacity to match crystal unit load capacity. Steps of 0.4 pF
External load Capacitance			3.5	pF	Maximum external capacity allowed (package, routing, etc.)
Internal ESR			100	kΩ	
Duty cycle	40	50	80	%	

SLOW RC OSCILLATOR (RC32K)

Parameter	Min	Typ	Max	Unit	Notes
Clock frequency	20	32.768	50	kHz	Untrimmed frequency (default values)
Trimming steps		1.5		%	
Start-up time			2	ms	VBAT applied to stabilization
Temperature coefficient			500	ppm/°C	–40 °C to 85 °C
			300	ppm/°C	–10 °C to 50 °C
Frequency stability			300	ppm	100 ms window, constant temperature
			350	ppm	30 ms window, constant temperature
			450	ppm	7.8 ms window, constant temperature
Duty cycle	40	50	60	%	

FAST RC OSCILLATOR (RCCLK)

Parameter	Min	Typ	Max	Unit	Notes
Clock frequency	4		32	MHz	Frequency trimming range
Untrimmed startup frequency	3	6	8	MHz	
Calibrated frequency	7.60	8	8.40	MHz	At ambient temperature
	15.20	16	16.80	MHz	At ambient temperature
	20.90	22	23.10	MHz	At ambient temperature
	30.40	32	33.60	MHz	At ambient temperature
Frequency stability in temperature	–0.25		0.25	%/°C	
Coarse trimming steps	0.5		2.5	MHz	From to Fmin to Fmax
Fine trimming steps		0.15	0.3	%	Relative to the targeted frequency
Duty cycle	40	50	60	%	
Start-up time		20	40	µs	From enable signal to the first rising clock edge
Frequency stability after start-up		500	1000	µs	From enable signal to target frequency at steady state
Clock Jitter @ 10.5 MHz		150	500	ps	RMS cycle jitter (Jc)
		1500	5000	ps	peak-to-peak jitter (BER = 1e-6) (~10 x Jc)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

POWER MANAGEMENT CONFIGURATIONS

RSL20 supports multiple power management configurations. This section provides information on the three most used configurations:

- RSL20 supplied by a Zn-Air battery, VCC in LDO mode from VBAT_LOW, VDDA in CP mode from VCC (Zn-Air Supply).
- RSL20 supplied by a Li-Ion battery, VDDA in DC-DC mode from VBAT, VCC in CP mode (inversed) from VDDA (Li-Ion Supply).
- RSL20 supplied by a Li-Ion battery, VDDA in LDO mode from VBAT, VCC in CP mode (inversed) from VDDA (Li-Ion LDO Supply)

For information about other possible configurations, please contact your **onsemi** representative.

Table 4. VBAT AND VBAT_LOW RANGE FOR DIFFERENT POWER SUPPLIES

Mode	Definition in SW	VBAT Range	VBAT_LOW Range
Zn-Air Supply	ZN-AIR_VCC_LDO_VDDA_CP	0.9 – 4.5 V	0.9 – 2.0 V
Li-Ion Supply	LI-ION_VCC_CP_VDDA_BUCK	2.5 – 4.5 V	= VCC
Li-Ion LDO Supply	LI-ION_VCC_CP_VDDA_LDO	2.0 – 4.5 V	= VCC

RSL20 supplied by Zn-Air battery, VCC in LDO mode from VBAT, VDDA in CP mode from VCC (Zn-Air Supply)

While many hearing aid manufacturers are moving to rechargeable Li-Ion based systems, there are still a decent numbers of hearing aids that will use disposable Zn-Air batteries. In this configuration, the RSL20 will not require the connection to an external inductor to save real estate in super small systems.

In this configuration, the following connections will need to be made at the PCB level:

- VBAT = Zinc-Air battery.
- VBAT_LOW = Zinc-Air battery.
- OD_REG_SUPPLY = Zinc-Air battery when OD is used.
  - When the OD is not used, the OD_REG_SUPPLY pin can either be left floating or connected to VDDA. Both the OD and VDDOD must be disabled in the application.

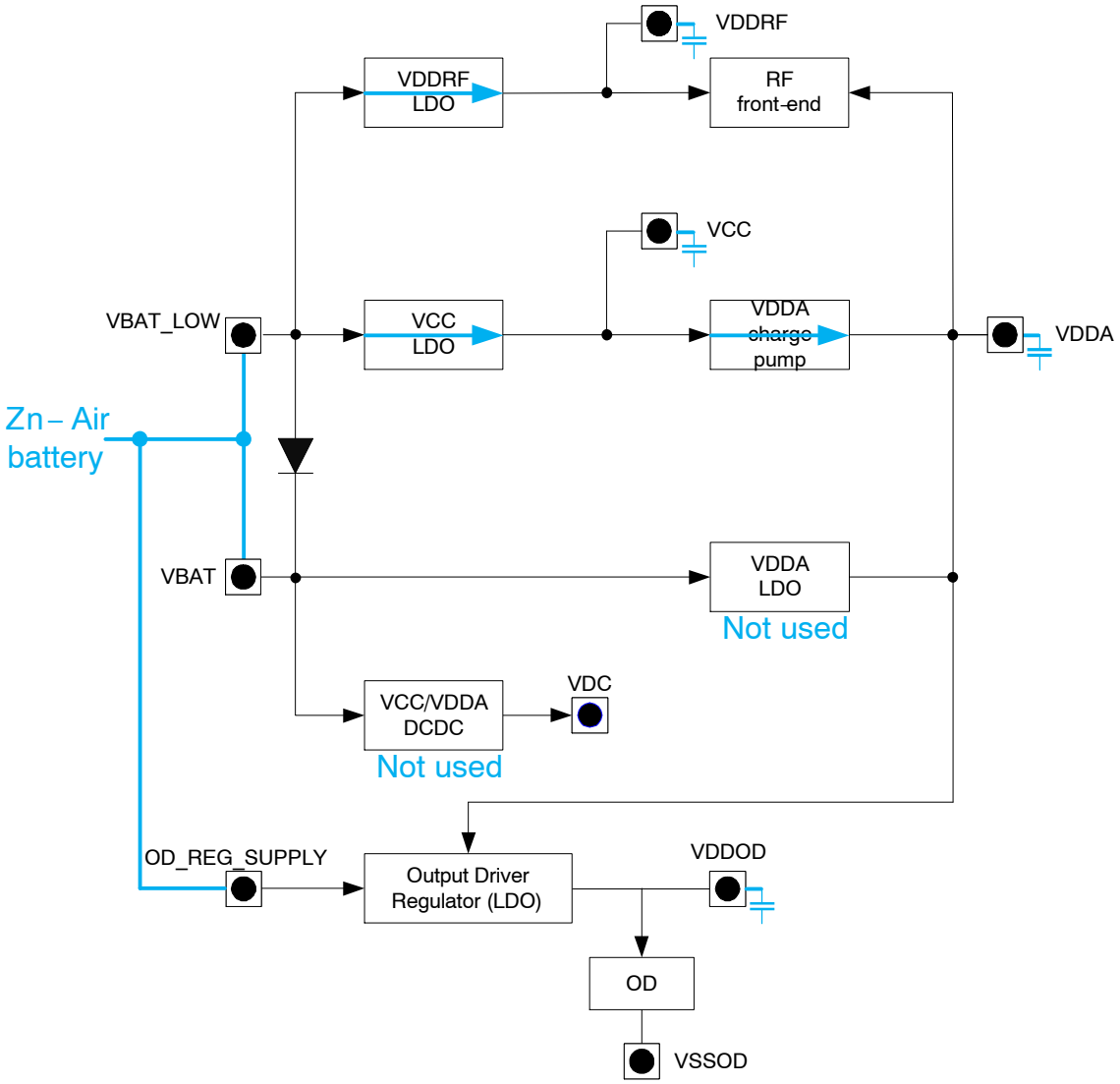


Figure 3. Zn-Air Supply Configuration Diagram

In the configuration, the min Vbat depends on TX power as follows:

Table 5. MIN VBAT VALUES FOR DIFFERENT TX POWERS

	TX Level [dBm]	Min VBAT, [V]	Comments
BR/BLE	0	0.90	RF front-end low power mode (most of the current is drawn on VDDRF supply)
	1	0.90	
	2	0.90	
	3	1.07	
	4	1.07	
	5	1.07	
	6	1.07	
EDR2	0	1.07	
	1	1.07	
	2	1.07	
	3	1.07	

POWER CONSUMPTION FOR VARIOUS AUDIO STREAMING USE CASES (25 °C, VBAT = VBAT_LOW = 1.25 V)

Parameter	Min	Typ	Max	Unit	Notes
$I_{BTCLASSIC}$, audio streaming*, **		3.80		mA	Primary earpiece: 48 kHz SF, 328 kbps with SBC, EDR2, TX = 0 dBm + NFMI TX
		1.02		mA	Secondary earpiece: NFMI RX
		2.41		mA	Average
		4.00		mA	Primary earpiece: 48 kHz SF, 328 kbps with SBC, EDR2, TX = 3 dBm + NFMI TX
		1.02		mA	Secondary earpiece: NFMI RX
		2.51		mA	Average
$I_{BTCLASSIC}$, audio streaming, no NFMI forwarding*		2.44		mA	48 kHz SF, 328 kbps with SBC, EDR2, TX = 0 dBm
		2.44		mA	48 kHz SF, 328 kbps with SBC, EDR2, TX = 3 dBm
$I_{BTCLASSIC}$, phone call**		2.21		mA	Primary earpiece: 16 kHz SF bi-directional, 60.8 kbps with mSBC, EDR2, TX = 0 dBm + NFMI TX
		0.53		mA	Secondary earpiece: NFMI RX
		1.37		mA	Average
		2.40		mA	Primary earpiece: 16 kHz SF bi-directional, 60.8 kbps with mSBC, EDR2, TX = 3 dBm + NFMI TX
		0.53		mA	Secondary earpiece: NFMI RX
		1.46		mA	Average
		3.43		mA	Primary earpiece: 16 kHz SF bi-directional, 60.8 kbps with mSBC, BR, TX = 6 dBm + NFMI TX
		0.53		mA	Secondary earpiece: NFMI RX
		1.98		mA	Average
$I_{BTCLASSIC}$, phone call, no NFMI forwarding		2.85		mA	16 kHz SF bi−directional, 60.8 kbps with mSBC, EDR2, TX = 0 dBm
		2.85		mA	16 kHz SF bi−directional, 60.8 kbps with mSBC, EDR2, TX = 3 dBm
		2.89		mA	16 kHz SF bi−directional, 60.8 kbps with mSBC, EDR2, TX = 6 dBm
		3.39		mA	16 kHz SF bi−directional, 60.8 kbps with mSBC, BR, TX = 6 dBm

POWER CONSUMPTION FOR VARIOUS AUDIO STREAMING USE CASES (25 °C, VBAT = VBAT_LOW = 1.25 V)

Parameter	Min	Typ	Max	Unit	Notes
I_{BLE}, audio streaming, CIS		1.38		mA	48 kHz SF, 80 kbps with LC3, 2 Mbps, TX = 0 dBm
		1.47		mA	48 kHz SF, 80 kbps with LC3, 2 Mbps, TX = 6 dBm
		1.28		mA	24 kHz SF, 48 kbps with LC3, 2 Mbps, TX = 0 dBm
		1.35		mA	24 kHz SF, 48 kbps with LC3, 2 Mbps, TX = 6 dBm
		1.22		mA	16 kHz SF, 32 kbps with LC3, 2 Mbps, TX = 0 dBm
		1.30		mA	16 kHz SF, 32 kbps with LC3, 2 Mbps, TX = 6 dBm
I_{BLE}, audio streaming, BIS, sink		1.42		mA	48 kHz SF, 80 kbps with LC3, 2 Mbps
		1.22		mA	24 kHz SF, 48 kbps with LC3, 2 Mbps
		1.15		mA	16 kHz SF, 32 kbps with LC3, 2 Mbps
I_{BLE}, phone call		2.14		mA	Primary earpiece: 16 kHz SF bi-directional, 32 kbps with LC3, 2 Mbps, TX = 0 dBm
		1.85		mA	Secondary earpiece: 16 kHz SF RX, 32 kbps with LC3, 2 Mbps, TX = 0 dBm
		2.30		mA	Primary earpiece: 16 kHz SF bi-directional, 32 kbps with LC3, 2 Mbps, TX = 6 dBm
		1.89		mA	Secondary earpiece: 16 kHz SF RX, 32 kbps with LC3, 2 Mbps, TX = 6 dBm
		2.35		mA	Primary earpiece: 32 kHz SF bi-directional, 64 kbps with LC3, 2 Mbps, TX = 0 dBm
		1.69		mA	Secondary earpiece: 32 kHz SF RX, 64 kbps with LC3, 2 Mbps, TX = 0 dBm
		2.70		mA	Primary earpiece: 32 kHz SF bi-directional, 64 kbps with LC3, 2 Mbps, TX = 6 dBm
		1.80		mA	Secondary earpiece: 32 kHz SF RX, 64 kbps with LC3, 2 Mbps, TX = 6 dBm
I_{NFMI}**		1.21		mA	24 kHz SF, bi-directional, low latency, block mode.

* TX ACK are sent in BR mode

** Power consumptions values are based on estimates. Measured values will be available in future datasheet versions.

NOTES:
- Power consumption estimates provided with 48 MHz XTAL with 6 pF of crystal capacitance.
- Recommended VDDO connection: VBAT.
- GPIOs configured with weak pull-up. No activities on GPIOs.
- OD_REG_SUPPLY = VBAT
- Power consumption measurements made with no speaker connected to the Output Stage.

MAINTAINING CONNECTION AND ADVERTISING MODE POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit	Notes
$I_{BTCLASSIC}$, maintaining connection mode*		19		µA	250 ms connection interval, 0 dBm TX
		20		µA	250 ms connection interval, 6 dBm TX
I_{BLE}, maintaining connection mode		33		µA	250 ms connection interval, 0 dBm TX
		37		µA	250 ms connection interval, 6 dBm TX
I_{BLE}, advertising mode		112		µA	211.25 ms advertising interval, 0 dBm TX
		154		µA	211.25 ms advertising interval, 6 dBm TX

* uses BR mode

STANDBY AND SLEEP MODES POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit	Notes
$I_{STANDBY}$		77		μA	RTC and RC 32 kHz on. See Power Modes section.
$I_{SLEEP\ ALL\ RAM\ RET}$		3.0		μA	All RAM in retention, RTC and RC 32 kHz on. See Power Modes section.
$I_{SLEEP\ ALL\ RAM\ OFF}$		0.26		μA	All RAM powered OFF. RTC and RC 32 kHz on. See Power Modes section.

RX POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit	Notes
Current Consumption at 1 Mbps		6.1		mA	BLE/BR in continuous operation (100% duty cycle)
Current Consumption at 2 Mbps		6.8		mA	BLE in continuous operation (100% duty cycle)
		6.4		mA	EDR2 in continuous operation (100% duty cycle)
Current Consumption at 3 Mbps		6.4		mA	EDR3 in continuous operation (100% duty cycle)

NOTE: RX and TX power consumption measurements include the entire chip's power consumption.

TX POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit	Notes
Current consumption at 1 Mbps		11.5		mA	0 dBm TX Power, BLE/BR in continuous operation (100% duty cycle)
		13.7		mA	2 dBm TX Power, BLE/BR in continuous operation (100% duty cycle)
		16.2		mA	4 dBm TX Power, BLE/BR in continuous operation (100% duty cycle)
		19.8		mA	6 dBm TX Power, BLE/BR in continuous operation (100% duty cycle)
Current consumption at 2 Mbps		11.6		mA	0 dBm TX Power, BLE in continuous operation (100% duty cycle)
		13.8		mA	2 dBm TX Power, BLE in continuous operation (100% duty cycle)
		16.3		mA	4 dBm TX Power, BLE in continuous operation (100% duty cycle)
		19.9		mA	6 dBm TX Power, BLE in continuous operation (100% duty cycle)
		12.2		mA	0 dBm TX Power, BT EDR2 in continuous operation (100% duty cycle)
		14.3		mA	2 dBm TX Power, BT EDR2 in continuous operation (100% duty cycle)
		15.4		mA	3 dBm TX Power, BT EDR2 in continuous operation (100% duty cycle)

NOTE: RX and TX power consumption measurements include the entire chip's power consumption.

In case a regulated supply at 1.8 V is available in the system, LDO mode should be used, and no external inductor is needed. VBAT should be connected to VDDA. For information about this configuration, please contact your **onsemi** representative.

Customers using DC-DC mode with a Zn-Air battery can expect to see a power consumption reduction by 5 to 10% on audio streaming use cases, with VBAT at 1.25 V, to the expense of the additional external DC-DC inductor.

In the Zn-Air Supply mode, the following application diagram should be observed:

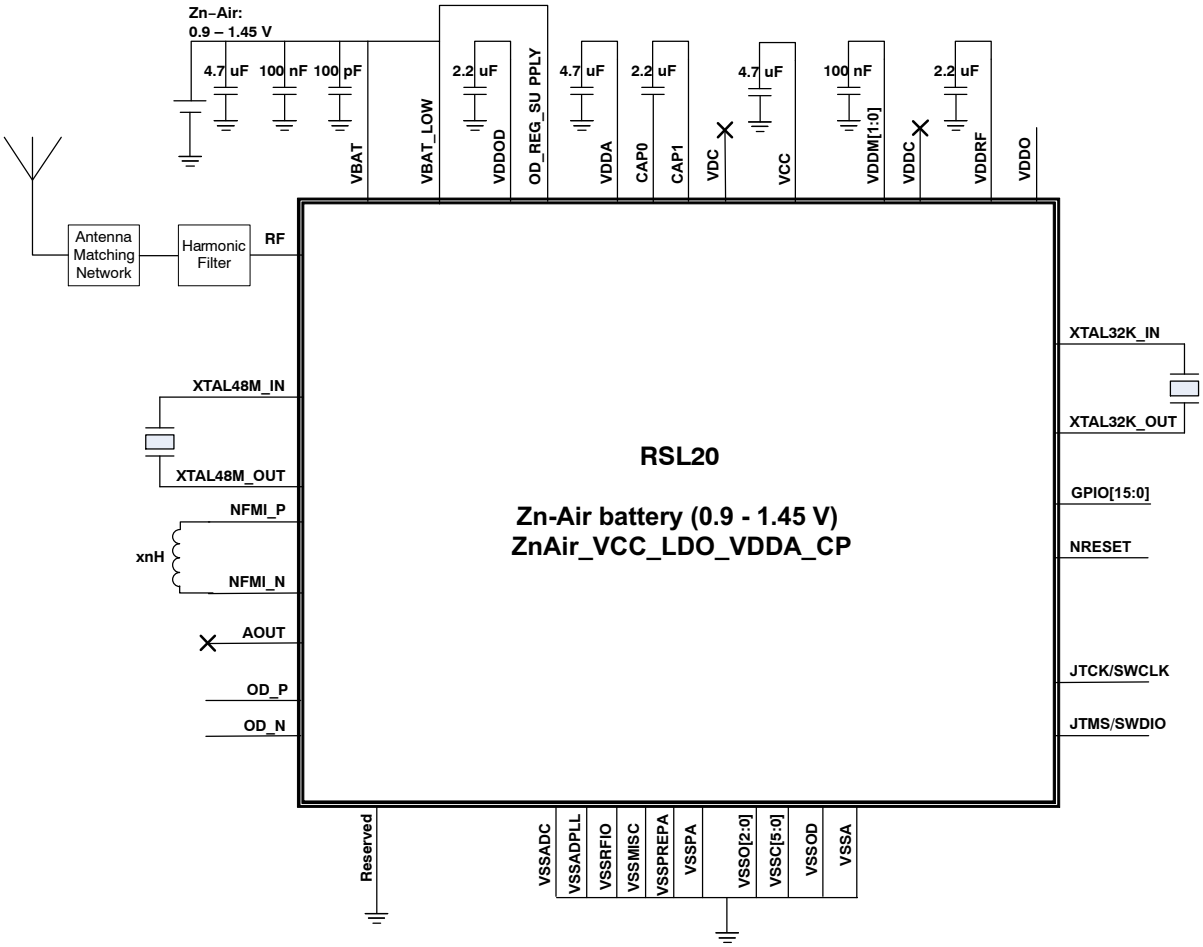


Figure 4. Zn-Air Supply Application Diagram

RSL20 Supplied by a Li-Ion Battery, VDDA in DC-DC Mode from VBAT, VCC in CP Mode (inversed) from VDDA (Li-Ion Supply)

This use case corresponds to an RSL20 system directly supply with a Li-Ion battery (no external regulator). The RSL20 is used in DC-DC mode, and the internal DC-DC (buck converter) is connected to VDDA through an external inductor. Note that the NFMI interface cannot be used in this mode, due to immunity issues with the VDDA inductor.

In this configuration, the following connections will need to be made at the board level:

- VBAT = Li-ion battery.
- VBAT_LOW = VCC, which is the output of the VDDA charge pump, used backwards: VDDA/2
- OD_REG_SUPPLY = VDDA.
  - When the OD is not used, the OD_REG_SUPPLY pin can either be left floating or connected to VDDA. Both the OD and VDDOD must be disabled in the application.

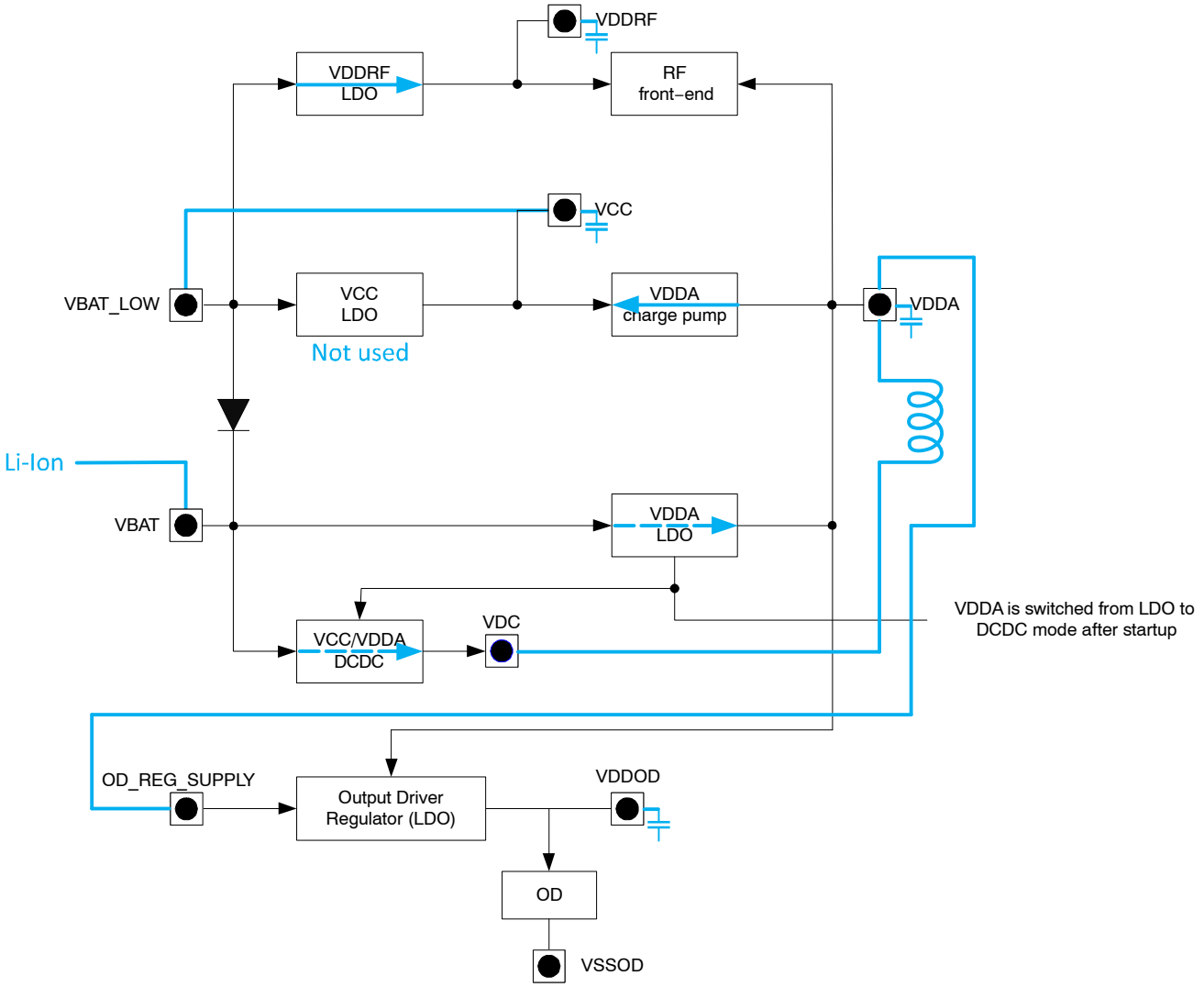


Figure 5. Li-Ion Supply Configuration Diagram

The min Vbat the RSL20 supports in this mode is 2.5 V and is independent from the TX power.

Notes:

- RF front-end low power mode (most of the current is drawn on VDDRF supply) is used up to TX = +2 dBm in BLE/BR mode and up to −1 dBm in EDR2 mode.
- For higher TX Power, RF front-end high power mode is used (most of the current is drawn on VDDA supply).
- When an inductor is connected between the VDC and VDDA pins to support the Li-Ion Supply power supply configuration, DO NOT select the Other_VCC_LDO_VDDA_LDO mode in firmware. To do so causes damage to the chip, rendering RSL20 unusable.

POWER CONSUMPTION FOR VARIOUS AUDIO STREAMING USE CASES (25 °C, VBAT = 3.7 V)

Parameter	Min	Typ	Max	Unit	Notes
$I_{BTCLASSIC}$, audio streaming*		0.81		mA	Primary earpiece: 48 kHz SF, 328 kbps with SBC, EDR2, TX = 0 dBm, no forwarding
		0.81		mA	Primary earpiece: 48 kHz SF, 328 kbps with SBC, EDR2, TX = 4 dBm, no forwarding
		0.83		mA	Primary earpiece: 48 kHz SF, 328 kbps with SBC, EDR2, TX = 6 dBm, no forwarding
		0.84		mA	Primary earpiece: 48 kHz SF, 328 kbps with SBC, EDR2, TX = 10 dBm, no forwarding
$I_{BTCLASSIC}$, phone call		0.96		mA	Primary earpiece: 16 kHz SF bi-directional, 60.8 kbps with mSBC, EDR2, TX = 0 dBm
		1.02		mA	Primary earpiece: 16 kHz SF bi-directional, 60.8 kbps with mSBC, EDR2, TX = 3 dBm
		1.03		mA	Primary earpiece: 16 kHz SF bi-directional, 60.8 kbps with mSBC, EDR2, TX = 6 dBm
		1.19		mA	Primary earpiece: 16 kHz SF bi-directional, 60.8 kbps with mSBC, BR, TX = 6 dBm
		1.27		mA	Primary earpiece: 16 kHz SF bi-directional, 60.8 kbps with mSBC, BR, TX = 10 dBm
I_{BLE}, audio streaming, CIS		0.46		mA	48 kHz SF, 80 kbps with LC3, 2 Mbps, TX = 0 dBm
		0.53		mA	48 kHz SF, 80 kbps with LC3, 2 Mbps, TX = 6 dBm
		0.59		mA	48 kHz SF, 80 kbps with LC3, 2 Mbps, TX = 10 dBm
		0.42		mA	24 kHz SF, 48 kbps with LC3, 2 Mbps, TX = 0 dBm
		0.50		mA	24 kHz SF, 48 kbps with LC3, 2 Mbps, TX = 6 dBm
		0.55		mA	24 kHz SF, 48 kbps with LC3, 2 Mbps, TX = 10 dBm
		0.41		mA	16 kHz SF, 32 kbps with LC3, 2 Mbps, TX = 0 dBm
		0.48		mA	16 kHz SF, 32 kbps with LC3, 2 Mbps, TX = 6 dBm
		0.53		mA	16 kHz SF, 32 kbps with LC3, 2 Mbps, TX = 10 dBm
I_{BLE}, audio streaming, BIS, sink		0.47		mA	48 kHz SF, 80 kbps with LC3, 2 Mbps
		0.40		mA	24 kHz SF, 48 kbps with LC3, 2 Mbps
		0.38		mA	16 kHz SF, 32 kbps with LC3, 2 Mbps
I_{BLE}, phone call		0.75		mA	Primary earpiece: 16 kHz SF bi-directional, 32 kbps with LC3, 2 Mbps, TX = 0 dBm
		0.64		mA	Secondary earpiece: 16 kHz SF RX, 32 kbps with LC3, 2 Mbps, TX = 0 dBm
		0.91		mA	Primary earpiece: 16 kHz SF bi-directional, 32 kbps with LC3, 2 Mbps, TX = 6 dBm
		0.70		mA	Secondary earpiece: 16 kHz SF RX, 32 kbps with LC3, 2 Mbps, TX = 6 dBm
		1.03		mA	Primary earpiece: 16 kHz SF bi-directional, 32 kbps with LC3, 2 Mbps, TX = 10 dBm
		0.72		mA	Secondary earpiece: 16 kHz SF RX, 32 kbps with LC3, 2 Mbps, TX = 10 dBm

POWER CONSUMPTION FOR VARIOUS AUDIO STREAMING USE CASES (25 °C, VBAT = 3.7 V)

Parameter	Min	Typ	Max	Unit	Notes
I_{BLE}, phone call		0.78		mA	Primary earpiece: 32 kHz SF bi-directional, 64 kbps with LC3, 2 Mbps, TX = 0 dBm
		0.62		mA	Secondary earpiece: 32 kHz SF RX, 64 kbps with LC3, 2 Mbps, TX = 0 dBm
		1.09		mA	Primary earpiece: 32kHz SF bi-directional, 64 kbps with LC3, 2 Mbps, TX = 6 dBm
		0.66		mA	Secondary earpiece: 32 kHz SF RX, 64 kbps with LC3, 2 Mbps, TX = 6 dBm
		1.27		mA	Primary earpiece: 32 kHz SF bi-directional, 64 kbps with LC3, 2 Mbps, TX = 10 dBm
		0.69		mA	Secondary earpiece: 32 kHz SF RX, 64 kbps with LC3, 2 Mbps, TX = 10 dBm

* TX ACK are sent in BR mode

NOTES:
- Power consumption estimates provided with 48 Mhz XTAL with 6 pF of crystal capacitance.
- Recommended VDDO connection: VDDA.
- Unused GPIOs configured with weak pull-up.
- OD_REG_SUPPLY = VDDA
- Power consumption measurements made with no speaker connected to the Output Stage.

MAINTAINING CONNECTION AND ADVERTISING MODE POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit	Notes
$I_{BTCLASSIC}$, maintaining connection mode*		5		μA	250 ms connection interval, 0 dBm TX
		7		μA	250 ms connection interval, 6 dBm TX
		7		μA	250 ms connection interval, 10 dBm TX
I_{BLE}, maintaining connection mode		12		μA	250 ms connection interval, 0 dBm TX
		15		μA	250 ms connection interval, 6 dBm TX
		17		μA	250 ms connection interval, 10 dBm TX
I_{BLE}, advertising mode		42		μA	211.25 ms advertising interval, 0 dBm TX
		80		μA	211.25 ms advertising interval, 6 dBm TX
		108		μA	211.25 ms advertising interval, 10 dBm TX

* uses BR mode

STANDBY AND SLEEP MODES POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit	Notes
$I_{STANDBY}$		30		μA	RTC and RC 32 kHz on. See Power Modes section.
$I_{SLEEP\ ALL\ RAM\ RET}$		1.1		μA	All RAM in retention, RTC and RC 32 kHz on. See Power Modes section.
$I_{SLEEP\ ALL\ RAM\ OFF}$		0.16		μA	All RAM powered OFF. RTC and RC 32 kHz on. See Power Modes section.

RX POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit	Notes
Current Consumption at 1 Mbps		2.2		mA	BLE/BR in continuous operation (100% duty cycle)
Current Consumption at 2 Mbps		2.5		mA	BLE in continuous operation (100% duty cycle)
		2.3		mA	EDR2 in continuous operation (100% duty cycle)
Current Consumption at 3 Mbps		2.3		mA	EDR3 in continuous operation (100% duty cycle)

NOTE: RX and TX power consumption measurements include the entire chip's power consumption.

TX POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit	Notes
Current consumption at 1 Mbps		4.2		mA	0 dBm TX Power, BLE/BR in continuous operation (100% duty cycle)
		4.9		mA	2 dBm TX Power, BLE/BR in continuous operation (100% duty cycle)
		9.7		mA	4 dBm TX Power, BLE/BR in continuous operation (100% duty cycle)
		12.1		mA	6 dBm TX Power, BLE/BR in continuous operation (100% duty cycle)
		17.7		mA	10 dBm TX Power, BLE/BR in continuous operation (100% duty cycle)
Current consumption at 2 Mbps		4.3		mA	0 dBm TX Power, BLE in continuous operation (100% duty cycle)
		4.9		mA	2 dBm TX Power, BLE in continuous operation (100% duty cycle)
		9.7		mA	4 dBm TX Power, BLE in continuous operation (100% duty cycle)
		12.2		mA	6 dBm TX Power, BLE in continuous operation (100% duty cycle)
		17.9		mA	10 dBm TX Power, BLE in continuous operation (100% duty cycle)
		6.9		mA	0 dBm TX Power, BT EDR2 in continuous operation (100% duty cycle)
		8.4		mA	2 dBm TX Power, BT EDR2 in continuous operation (100% duty cycle)
		10.1		mA	4 dBm TX Power, BT EDR2 in continuous operation (100% duty cycle)

NOTE: RX and TX power consumption measurements include the entire chip's power consumption.

In this mode, the following application diagram should be observed:

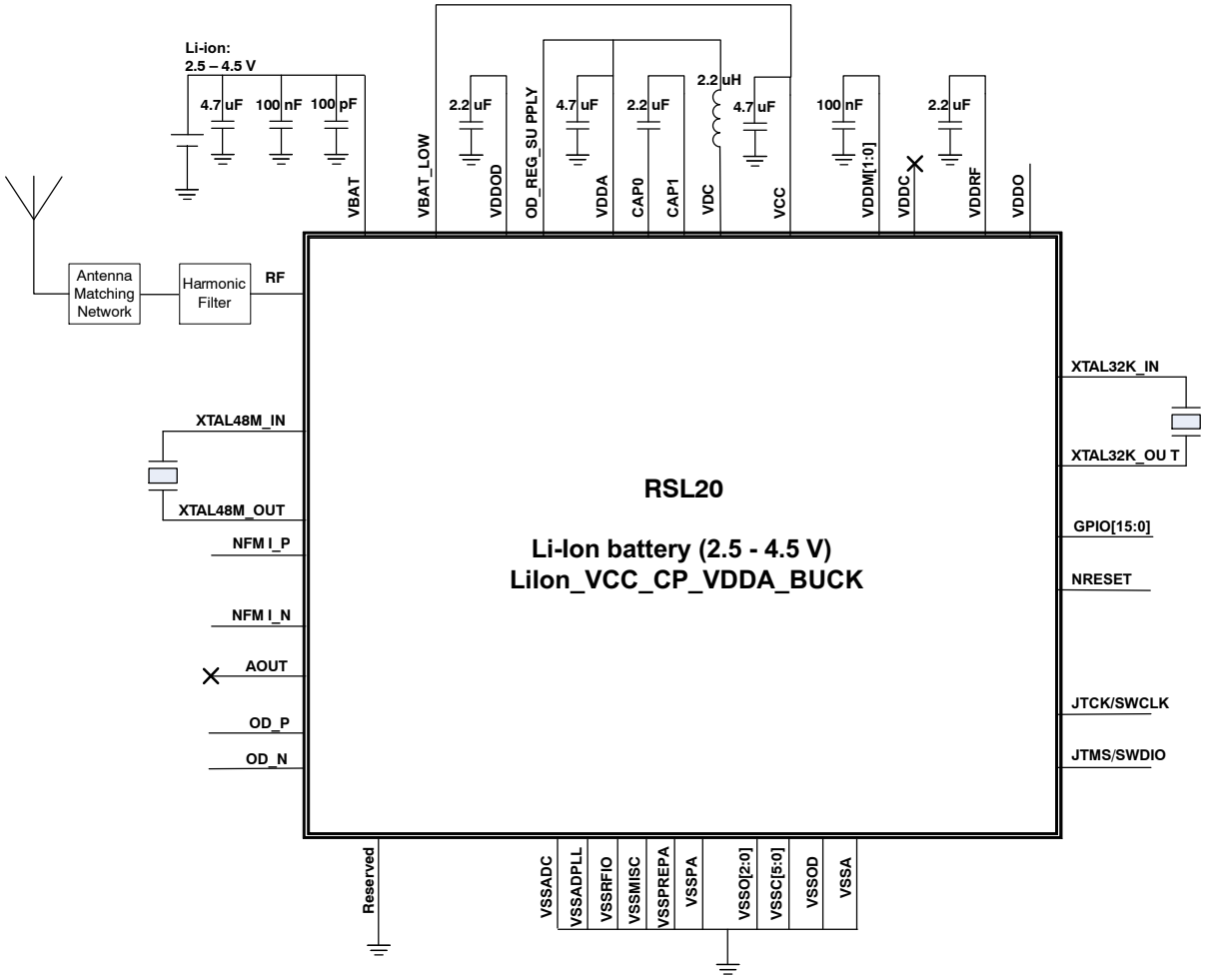


Figure 6. Li-Ion Supply Application Diagram

RSL20 Supplied by a Li-Ion Battery, VDDA in LDO Mode from VBAT, VCC in CP Mode (reversed) from VDDA (Li-Ion LDO Supply)

This use case corresponds to an RSL20 system directly supplied with a Li-Ion battery (no external regulator); in this case, no external inductor is needed: VDDA is generated from VBAT in LDO mode. NFMI can be used in this mode.

In this configuration, the following connections will need to be made at the board level:

- VBAT = Li-ion battery.
- VBAT_LOW = VCC, which is the output of the VDDA charge pump, used backwards: VDDA/2
- OD_REG_SUPPLY = VDDA.
  - When the OD is not used, the OD_REG_SUPPLY pin can either be left floating or connected to VDDA. Both the OD and VDDOD must be disabled in the application.

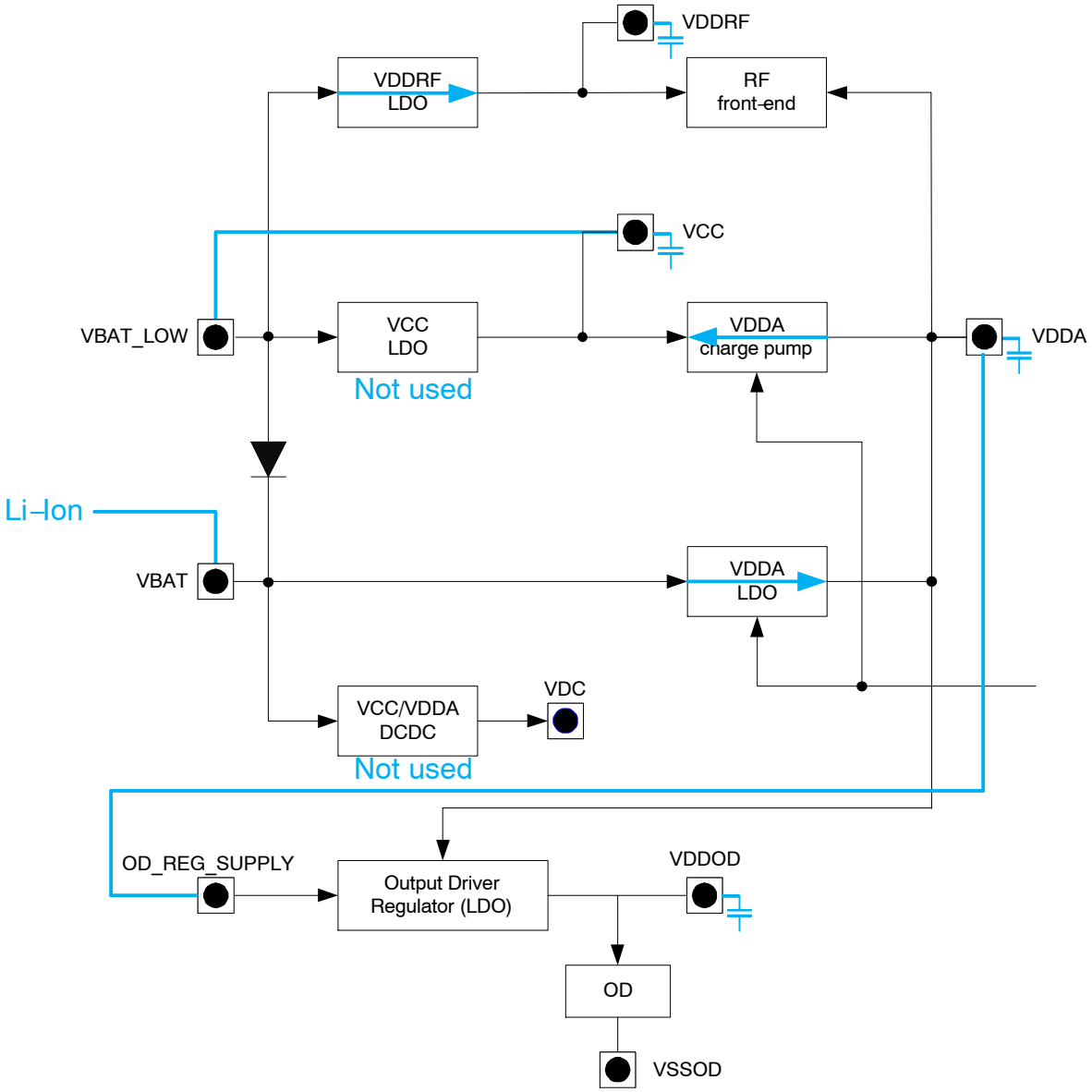


Figure 7. Li-Ion LDO Supply Configuration Diagram

Notes:

- RF front-end low power mode (most of the current is drawn on VDDRF supply) is used up to TX = +2 dBm in BLE/BR mode and up to −1 dBm in EDR2 mode.
- For higher TX Power, RF front-end high power mode is used (most of the current is drawn on VDDA supply).

POWER CONSUMPTION FOR VARIOUS AUDIO STREAMING USE CASES (25 °C, VBAT = 3.7 V)

Parameter	Min	Typ	Max	Unit	Notes
$I_{BTCLASSIC}$, audio streaming*, **		2.89		mA	Primary earpiece: 48 kHz SF, 328 kbps with SBC, EDR2, TX = 0 dBm + NFMI TX
		0.51		mA	Secondary earpiece: NFMI RX
		1.70		mA	Average
		3.16		mA	Primary earpiece: 48 kHz SF, 328 kbps with SBC, EDR2, TX = 4 dBm + NFMI TX
		0.51		mA	Secondary earpiece: NFMI RX
		1.83		mA	Average
		4.30		mA	Primary earpiece: 48 kHz SF, 328 kbps with SBC, EDR2, TX = 6 dBm + NFMI TX
		0.51		mA	Secondary earpiece: NFMI RX
		2.41		mA	Average
		5.55		mA	Primary earpiece: 48 kHz SF, 328 kbps with SBC, EDR2, TX = 10 dBm + NFMI TX
		0.51		mA	Secondary earpiece: NFMI RX
		3.03		mA	Average
$I_{BTCLASSIC}$, audio streaming, no NFMI forwarding*		1.26		mA	48 kHz SF, 328 kbps with SBC, EDR2, TX = 0 dBm
		1.30		mA	48 kHz SF, 328 kbps with SBC, EDR2, TX = 3 dBm
		1.33		mA	48 kHz SF, 328 kbps with SBC, EDR2, TX = 6 dBm
		1.35		mA	48 kHz SF, 328 kbps with SBC, EDR2, TX = 10 dBm
$I_{BTCLASSIC}$, phone call**		1.72		mA	Primary earpiece: 16 kHz SF bi-directional, 60.8 kbps with mSBC, EDR2, TX = 0 dBm + NFMI TX
		0.26		mA	Secondary earpiece: NFMI RX
		0.99		mA	Average
		2.28		mA	Primary earpiece: 16 kHz SF bi-directional, 60.8 kbps with mSBC, EDR2, TX = 3 dBm + NFMI TX
		0.26		mA	Secondary earpiece: NFMI RX
		1.27		mA	Average
		4.46		mA	Primary earpiece: 16 kHz SF bi-directional, 60.8 kbps with mSBC, BR, TX = 6 dBm + NFMI TX
		0.26		mA	Secondary earpiece: NFMI RX
		2.36		mA	Average
		6.40		mA	Primary earpiece: 16 kHz SF bi-directional, 60.8 kbps with mSBC, BR, TX = 10 dBm + NFMI TX
		0.26		mA	Secondary earpiece: NFMI RX
		3.33		mA	Average
$I_{BTCLASSIC}$, phone call, no NFMI forwarding		1.57		mA	16 kHz SF bi-directional, 60.8 kbps with mSBC, EDR2, TX = 0 dBm
		1.61		mA	16 kHz SF bi-directional, 60.8 kbps with mSBC, EDR2, TX = 3 dBm
		1.65		mA	16 kHz SF bi-directional, 60.8 kbps with mSBC, EDR2, TX = 6 dBm
		1.85		mA	16 kHz SF bi-directional, 60.8 kbps with mSBC, BR, TX = 6 dBm
		1.88		mA	16 kHz SF bi-directional, 60.8 kbps with mSBC, BR, TX = 10 dBm

POWER CONSUMPTION FOR VARIOUS AUDIO STREAMING USE CASES (25 °C, VBAT = 3.7 V)

Parameter	Min	Typ	Max	Unit	Notes
I_{BLE}, audio streaming, CIS		0.69		mA	48 kHz SF, 80 kbps with LC3, 2 Mbps, TX = 0 dBm
		0.80		mA	48 kHz SF, 80 kbps with LC3, 2 Mbps, TX = 6 dBm
		0.88		mA	48 kHz SF, 80 kbps with LC3, 2 Mbps, TX = 10 dBm
		0.66		mA	24 kHz SF, 48 kbps with LC3, 2 Mbps, TX = 0 dBm
		0.76		mA	24 kHz SF, 48 kbps with LC3, 2 Mbps, TX = 6 dBm
		0.83		mA	24 kHz SF, 48 kbps with LC3, 2 Mbps, TX = 10 dBm
		0.63		mA	16 kHz SF, 32 kbps with LC3, 2 Mbps, TX = 0 dBm
		0.76		mA	16 kHz SF, 32 kbps with LC3, 2 Mbps, TX = 6 dBm
		0.82		mA	16 kHz SF, 32 kbps with LC3, 2 Mbps, TX = 10 dBm
I_{BLE}, audio streaming, BIS, sink		0.74		mA	48 kHz SF, 80 kbps with LC3, 2 Mbps
		0.63		mA	24 kHz SF, 48 kbps with LC3, 2 Mbps
		0.60		mA	16 kHz SF, 32 kbps with LC3, 2 Mbps
I_{BLE}, phone call		1.08		mA	Primary earpiece: 16 kHz SF bi-directional, 32 kbps with LC3, 2 Mbps, TX = 0 dBm
		0.96		mA	Secondary earpiece: 16 kHz SF RX, 32 kbps with LC3, 2 Mbps, TX = 0 dBm
		1.34		mA	Primary earpiece: 16 kHz SF bi-directional, 32 kbps with LC3, 2 Mbps, TX = 6 dBm
		1.03		mA	Secondary earpiece: 16 kHz SF RX, 32 kbps with LC3, 2 Mbps, TX = 6 dBm
		1.44		mA	Primary earpiece: 16 kHz SF bi-directional, 32 kbps with LC3, 2 Mbps, TX = 10 dBm
		1.06		mA	Secondary earpiece: 16 kHz SF RX, 32 kbps with LC3, 2 Mbps, TX = 10 dBm
		1.19		mA	Primary earpiece: 32 kHz SF bi-directional, 64 kbps with LC3, 2 Mbps, TX = 0 dBm
		0.91		mA	Secondary earpiece: 32 kHz SF RX, 64 kbps with LC3, 2 Mbps, TX = 0 dBm
		1.57		mA	Primary earpiece: 32kHz SF bi-directional, 64 kbps with LC3, 2 Mbps, TX = 6 dBm
		0.99		mA	Secondary earpiece: 32 kHz SF RX, 64 kbps with LC3, 2 Mbps, TX = 6 dBm
		1.74		mA	Primary earpiece: 32 kHz SF bi-directional, 64 kbps with LC3, 2 Mbps, TX = 10 dBm
		1.02		mA	Secondary earpiece: 32 kHz SF RX, 64 kbps with LC3, 2 Mbps, TX = 10 dBm
I_{NFMI}**		0.57		mA	24 kHz SF, bi-directional, low latency, block mode.

* TX ACK are sent in BR mode

** Power consumptions values are based on estimates. Measured values will be available in future datasheet versions.

NOTES:
- Power consumption estimates provided with 48 MHz XTAL with 6 pF of crystal capacitance.
- Recommended VDDO connection: VDDA.
- Unused GPIOs configured with weak pull-up.
- OD_REG_SUPPLY = VDDA
- Power consumption measurements made with no speaker connected to the Output Stage.

MAINTAINING CONNECTION AND ADVERTISING MODE POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit	Notes
$I_{BTCLASSIC}$, maintaining connection mode*		10		µA	250 ms connection interval, 0 dBm TX
		11		µA	250 ms connection interval, 6 dBm TX
		11		µA	250 ms connection interval, 10 dBm TX
I_{BLE}, maintaining connection mode		22		µA	250 ms connection interval, 0 dBm TX
		22		µA	250 ms connection interval, 6 dBm TX
		24		µA	250 ms connection interval, 10 dBm TX
I_{BLE}, advertising mode		60		µA	211.25 ms advertising interval, 0 dBm TX
		124		µA	211.25 ms advertising interval, 6 dBm TX
		179		µA	211.25 ms advertising interval, 10 dBm TX

* uses BR mode

STANDBY AND SLEEP MODES POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit	Notes
$I_{STANDBY}$		43		µA	RTC and RC 32 kHz on. See Power Modes section.
$I_{SLEEP\ ALL\ RAM\ RET}$		1.6		µA	All RAM in retention, RTC and RC 32 kHz on. See Power Modes section.
$I_{SLEEP\ ALL\ RAM\ OFF}$		0.21		µA	All RAM powered OFF. RTC and RC 32 kHz on. See Power Modes section.

RX POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit	Notes
Current Consumption at 1 Mbps		3.2		mA	BLE/BR in continuous operation (100% duty cycle)
Current Consumption at 2 Mbps		3.6		mA	BLE in continuous operation (100% duty cycle)
		3.3		mA	EDR2 in continuous operation (100% duty cycle)
Current Consumption at 3 Mbps		3.3		mA	EDR3 in continuous operation (100% duty cycle)

NOTE: RX and TX power consumption measurements include the entire chip's power consumption.

TX POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit	Notes
Current consumption at 1 Mbps		5.8		mA	0 dBm TX Power, BLE/BR in continuous operation (100% duty cycle)
		7.1		mA	2 dBm TX Power, BLE/BR in continuous operation (100% duty cycle)
		13.8		mA	4 dBm TX Power, BLE/BR in continuous operation (100% duty cycle)
		17.4		mA	6 dBm TX Power, BLE/BR in continuous operation (100% duty cycle)
		26.6		mA	10 dBm TX Power, BLE/BR in continuous operation (100% duty cycle)

TX POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit	Notes
Current consumption at 2 Mbps		6.0		mA	0 dBm TX Power, BLE in continuous operation (100% duty cycle)
		7.2		mA	2 dBm TX Power, BLE in continuous operation (100% duty cycle)
		13.8		mA	4 dBm TX Power, BLE in continuous operation (100% duty cycle)
		17.5		mA	6 dBm TX Power, BLE in continuous operation (100% duty cycle)
		26.7		mA	10 dBm TX Power, BLE in continuous operation (100% duty cycle)
		10.0		mA	0 dBm TX Power, BT EDR2 in continuous operation (100% duty cycle)
		12.1		mA	2 dBm TX Power, BT EDR2 in continuous operation (100% duty cycle)
		14.5		mA	4 dBm TX Power, BT EDR2 in continuous operation (100% duty cycle)

NOTE: RX and TX power consumption measurements include the entire chip's power consumption.

In this mode, the following application diagram should be observed:

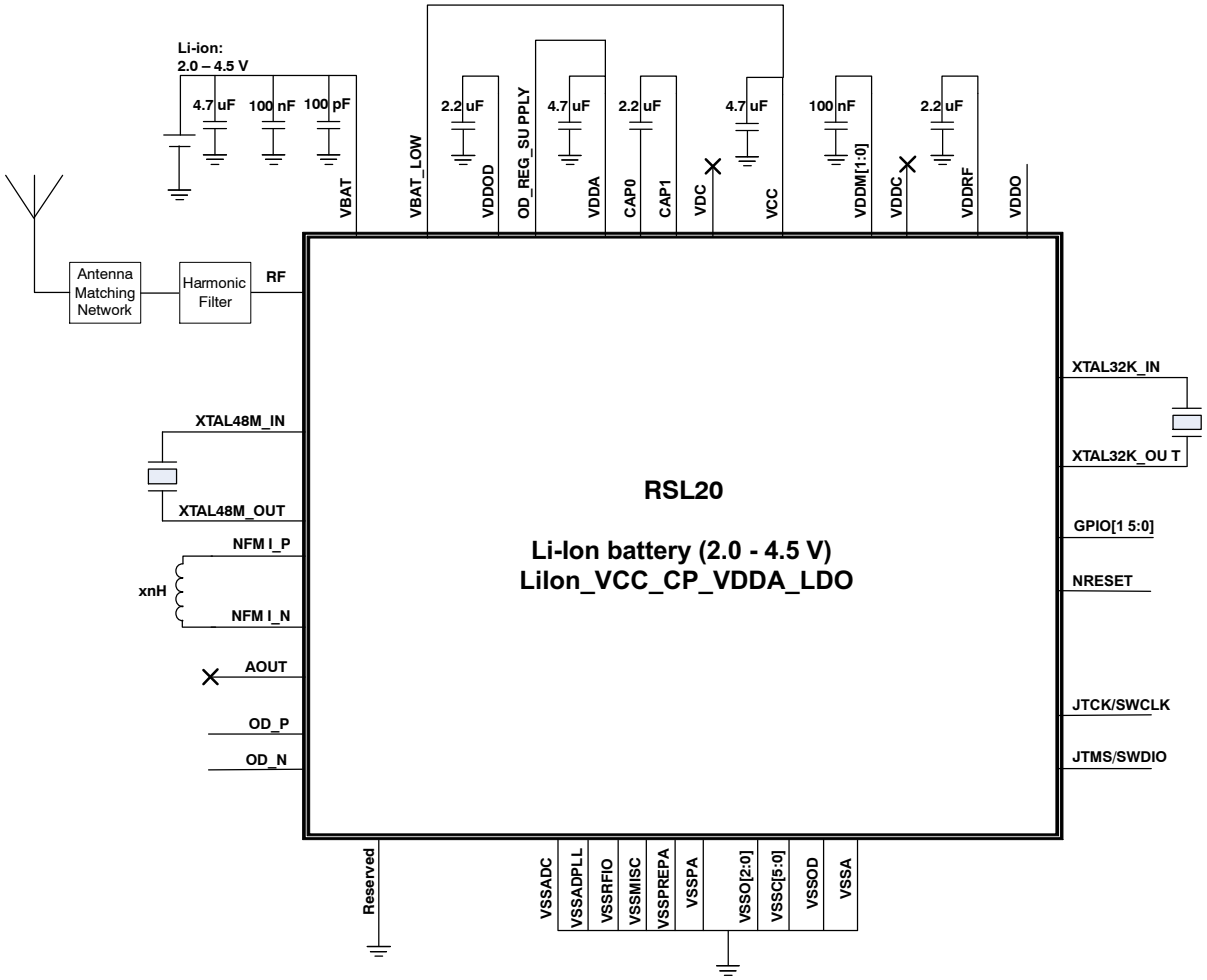
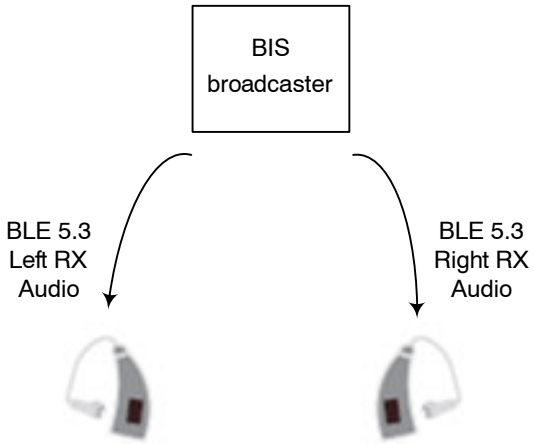


Figure 8. Li-Ion LDO Supply Application Diagram

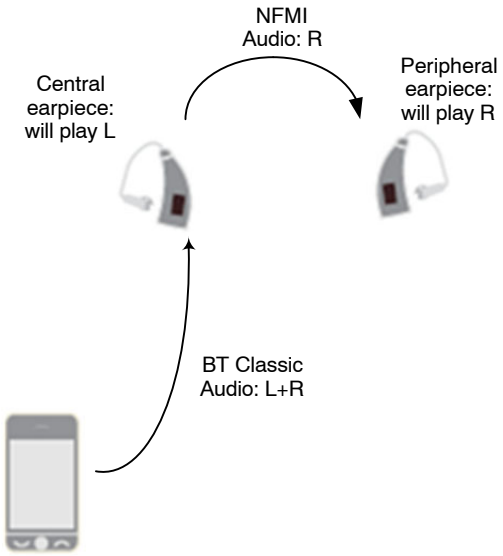
Description of the Main Audio Streaming Use Cases, available through sample codes in the SDK.

Audio Streaming with BLE5.3, CIS (Connected Isochronous Stream): 48, 24 or 16 kHz SF, audio signal at 96, 48 or 32 kbps with LC3, one channel, unidirectional.

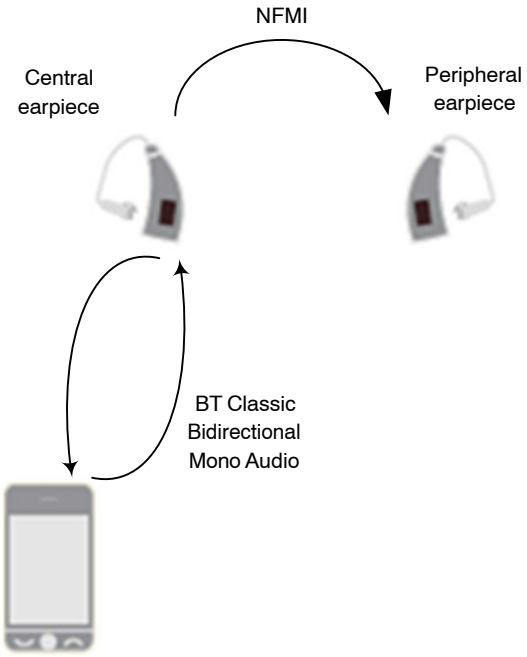
Audio Streaming with BLE5.3, BIS (Broadcast Isochronous Stream): 48, 24 or 16 kHz SF, audio signal at 96, 48 or 32 kbps with LC3, one channel, unidirectional. Sample code available for both the BIS broadcaster and the earpieces.



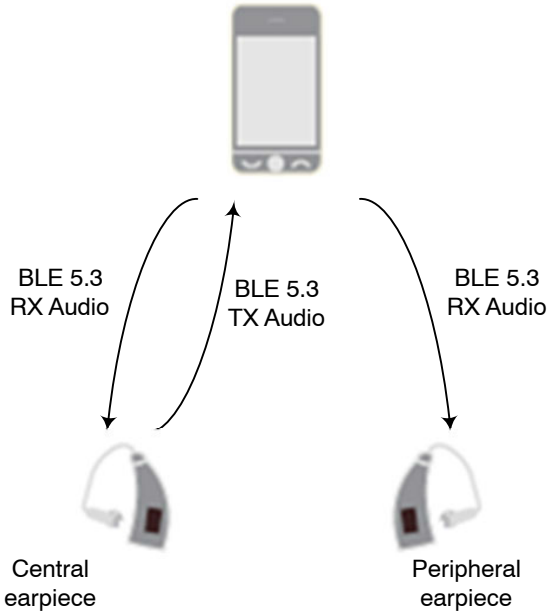
Audio Streaming with Bluetooth Classic: 48 kHz SF, audio signal at 328 kbps with SBC, two channel (for L), unidirectional, TWS with NFMI.



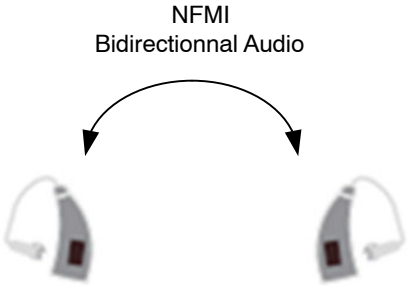
Phone call with Bluetooth Classic: 16 kHz SF, audio signal at 60.8 kbps with mSBC, bidirectional. NFMI forwarding is not available in **onsemi**'s sample code for this use case but can be managed by the customer's application.



Phone call with BLE 5.3: 16 kHz SF, 32 kbps with LC3



NFMI e2e audio, 16, 24 kHz SF



RSL20 Pin Specifications

RSL20 PIN SPECIFICATIONS

Name	Description	Type	Pull	IO Domain	WLCSP
VBAT	Battery input voltage	P		VBAT	M2
VBAT_LOW	Low voltage battery input voltage (typ. 1.2 V)	P			M3
VDDRF	Supply voltage for the low voltage part of RF front-end	P		VDDRF	G2
NFMI_P	Positive NFMI coil pin	A		NFMI_HV	P4
NFMI_N	Negative NFMI coil pin	A			P6
CAP1	Analog charge pump cap	A		VDDA	P1
XTAL32K_IN	XTAL input pin for 32 kHz XTAL	A			P2
XTAL32K_OUT	XTAL output pin for 32 kHz XTAL	A			P3
OD_REG_SUPPLY	VDDOD supply	P			P7
OD_N	Negative output of OD	A			P8
OD_P	Positive output of OD	A			P9
VCC	DC-DC filtered output	P			N1
CAP0	Analog charge pump cap	A			N2
VDDA	Analog charge pump output	P			N3
VSSA	Analog ground	P			N4
VDDOD	Supply for the output driver	P			N8
VSSOD	Ground for the output driver	P			N9
VDC	DC-DC output voltage to external LC filter	P			M1
AOUT	Analog test pin	A			N6
JTMS	CM33 JTAG TMS / Serial Wire DIO	I/O	UD	VDDO	N7
GPIO14	Digital I/O / LSAD / CM33-JTAG Test Data In	I/O	UD		L8
JTCK	CM33 JTAG TCK /Serial Wire CLK	I/O	UD		M8
RESERVED	Reserved. Connect to VSSO.	I	D		K2
NRESET	Reset pin	I	U		L1
GPIO11	Digital I/O / LSAD (Note 9)	I/O	UD		L6
GPIO13	Digital I/O / LSAD	I/O	UD		L7
GPIO15	Digital I/O / LSAD / CM33-JTAG Test Data Out	I/O	UD		M7
VDDC	Core logic voltage supply	P			L2
VSSC	Core logic & memories ground	P			L3,K6,K7, H1, H9, D7
GPIO12	Digital I/O / LSAD	I/O	UD		K9
GPIO1	Digital I/O / LSAD	I/O	UD		J2
GPIO0	Digital I/O / LSAD	I/O	UD		K1
GPIO10	Digital I/O / LSAD	I/O	UD		J7
VDDM	Memories voltage supply	P			J8,B8
GPIO2	Digital I/O / LSAD	I/O	UD		J1
VDDO	Digital I/O voltage supply	P			H3
GPIO9	Digital I/O / LSAD	I/O	UD		H7
VSSO	Digital I/O voltage GROUND	P			G3,G4,G7

RSL20 PIN SPECIFICATIONS (continued)

Name	Description	Type	Pull	IO Domain	WLCSP
GPIO3	Digital I/O / LSAD	I/O	UD	VDDO	G1
GPIO8	Digital I/O / LSAD	I/O	UD		F7
GPIO7	Digital I/O / LSAD	I/O	UD		F9
GPIO5	Digital I/O / LSAD	I/O	UD		D9
GPIO4	Digital I/O / LSAD (Note 9)	I/O	UD		B7
GPIO6	Digital I/O / LSAD	I/O	UD		B9
VSSPA	RF front-end analog ground	P		RF INTERNAL	E3
VSSPREPA	RF front-end analog ground	P			E4
VSSMISC	RF front-end analog ground	P			C5
RF	RF front-end signal input/output (Antenna)	A			C1
VSSRFIO	RF front-end analog ground	P			C2
VSSADPLL	RF front-end analog ground	P			A3
VSSADC	RF front-end analog ground	P			E5
XTAL48M_IN	XTAL input pin for 48 MHz XTAL	A			A4
XTAL48M_OUT	XTAL output pin for 48 MHz XTAL	A			A5
DUM	Dummy ball	–			M9

9. Intense activities on GPIO4 and GPIO11 might affect RF performances. Avoid using GPIO4 and GPIO11 for fast transitioning signals.

NOTES: Legend:

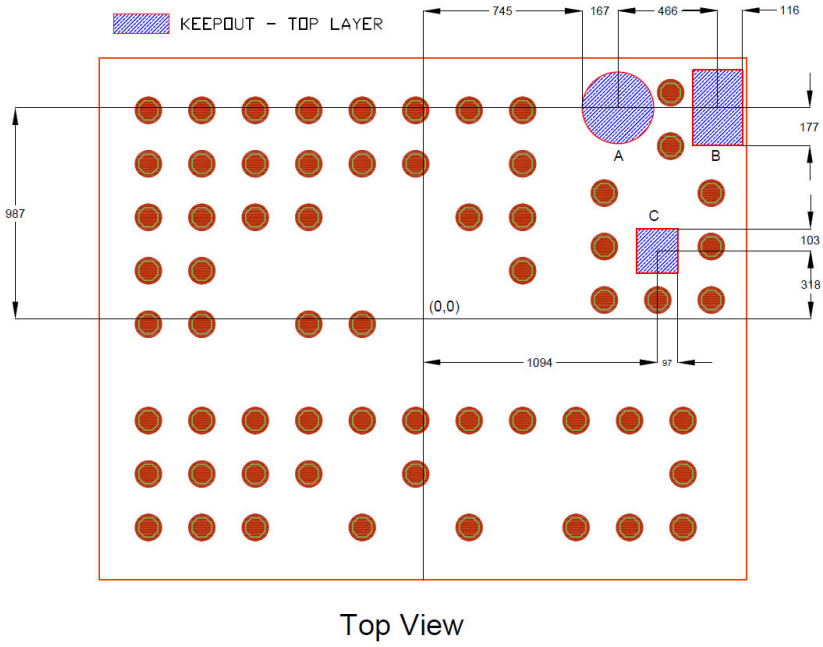
Type: A = analog; D = digital; I = input; O = output; P = power

Pull: U = pull up; D = pull down (Pull-up and pull down values are available in section IOs of the ELECTRICAL SPECIFICATIONS table).

PCB DESIGN GUIDELINES

General Guidelines

- Decoupling capacitors should be placed as close as possible to the related pins.
- Differential output signals should be routed as symmetrically as possible.
- Analog input signals should be shielded as well as possible.
- Put close attention to parasitic coupling capacitance.
- Multi-layer PCB should be used with a keep-out area on the inner layers directly below the antenna matching circuitry in order to reduce the stray capacitances that influence RF performance.
- For the keep-outs around the RF coils, if possible clear ground below them for ~130 µm. See keep-out area figure.
- All the supply voltage should be decoupled as close as possible to their respective pin with high performance RF capacitors. These supplies should be routed separately from each other and should be on different layers of the PCB. Lines between the chip's pin and the supply source should be as short as possible.
- The BUCK inductor must be placed close to the VDC pin, and the VDC node parasitic coupling capacitance must be minimized.



Center Co-ordinates

Keepout Area	X	Y
A	912	987
B	1378	987
C	1094	318

Dimensions

Keepout Area	X	Y	Radius
A			167
B	232	354	
C	194	206	

Units: um

Figure 9. Keep Out Area

Grounds Guidelines

- Connect directly the VSSRFIO to the ground plane. This will avoid noise injection and possible RF sensitivity degradation. VSSRFIO can be used to surround the RFIO on the PCB in a co-axial way. Use VIAs as much as possible to connect VSSRFIO to the ground plane around the RF line.
- Connect VSSADPLL directly to the ground plane to avoid the injection of the harmonics of the PLL to the other grounds through the shared ground line.
- For VSSRFIO and VSSADPLL, place the VIAs that connect these grounds to the ground plane as close as possible to their respective balls and add as much as possible to have a solid ground.
- Connect VSSPA directly to the ground plane.
- Connect VSSPREPA directly to the ground plane.
- Connect VSSADC directly to the ground plane to avoid the noise injection which will impact the sensitivity floor level.
- Connect VSSMISC directly to the ground plane.
- All of the RF grounds (VSSRFIO, VSSADC, VSSADPLL, VSSPA, VSSESD_RF, VSSMISC) should each be connected separately by via to a good ground plane. They should not be daisy chained together on L1 before going to a ground via.
- Keep the RF grounds separate from the VSSC & VSSO grounds, although it is fine for them to be connected at the 'main' ground plane.
- Use the second layer of the PCB as ground plane.

XTAL Guidelines for Both 32 kHz and 48 MHz

- The crystal should be placed as close as possible to the XTAL pins.
- Avoid short spacing between the two crystal's lines for a long distance to avoid a big parasitic shunt capacitance.
- Use a 48 MHz XTAL with low load capacitance to reduce the current consumption (recommended load capacitance = 6 pF).
- Avoid routing any noisy signal near the XTAL pins (e.g.: VDC signal).
- Digital signals should not be routed close to the crystal or the power supply lines.
- For the 48 MHz XTAL, ensure that the grounding is clear below signal pins, signal lines and the XTAL IC pins, on any layers close to the XTAL. Minimize the overall parasitic capacitance, and importantly, the part-to-part variation in parasitic capacitance due to stack up.

RFIO Pin Guidelines

- Keep the connection to the RF pin at 50 Ω
- Have a keep-out area on the inner layers directly below the antenna matching circuitry in order to reduce the stray capacitances that influence RF performance.
- Surround the RF line with VSSRFIO ground and use VIA, connecting VSSRFIO to the ground plan, along the RF line.

NFMI Pins Guidelines

- Routing from the NFMI_N/P pins to the coils should be minimized to reduce the parasitic impedance and inductance and not impact the system quality factor.
- The NFMI_N/P lines should be routed far from any toggling signal to avoid any noise injection.
- There should be no signal lines routed in the NFMI coil area.
- The coils orientation is important to maximize the magnetic field in the communication direction and increase the communication distance
- The coil pins should be orthogonal to the PCB board to minimize the interference.
- The coil should be placed in height with regard to the PCB components to maximize the magnetic field radiation; this recommendation is hard to achieve with an SMD coil.

RSL20 Passive Components

Table 6. EXTERNAL COMPONENTS
The following external components are mandatory:

Comp	Function	Typ. Value	Tol.
Cap (VBAT_LOW−VSSA)	VBAT_LOW decoupling	4.7 μF // 100 nF // 100 pF	±20%
Cap (VBAT−VSSA)	VBAT decoupling	4.7 μF // 100 nF // 100 pF	±20%
Cap (OD_REG_SUPPLY−VSSOD)	OD_REG_SUPPLY decoupling	4.7 μF	±20%
Cap (VDDOD−VSSOD)	VDDOD decoupling	2.2 μF	±20%
Cap (VDDO−VSSO)	VDDO decoupling	2.2 μF	±20%
Cap (VCC−VSSA)	VCC decoupling	4.7 μF	±20%
Cap (VDDA−VSSA)	VDDA decoupling	4.7 μF	±20%
Cap (CAP0−CAP1)	Pump capacitor for VDDA	2.2 μF	±20%
Cap (VDDM−VSSC)	VDDM decoupling	0.1 μF	±20%
Cap (VDDRF−VSSA)	VDDRF decoupling	2.2 μF	±20%
Inductor (DC-DC)	For Buck converter	2.2 μH Low ESR (<0.5 Ω), high Isat (min 200 mA), (i.e: CKP2012N_2R2, Taiyo Yuden)	±20%
XTAL_32kHz	XTAL for 32 kHz oscillator	Epsontoyocom MC − 306 Micro crystal CM8V-T1A	
XTAL_48MHz	XTAL for 48 MHz oscillator	Abracon ABM12W-48.0000MHZ-6-B1U-T3	
Antenna	Rx/Tx communication	Custom Antenna / SMD antenna	
NFMI Coil	Rx/Tx communication	Depends on the carrier frequency (3.9 μH for a carrier frequency of 10.56 MHz)	

NOTES:

- The VBAT_LOW caps depend on the Power Management configurations, see Supply Application Diagrams for more details.
- Please refer to the Supply Application Diagrams of section POWER MANAGEMENT CONFIGURATIONS for additional connection details.
- The NFMI performances depend on the Q factor of the coil. The RSL20 EVB uses a NFMI coil with a Q factor of 80 at 10.6 MHz.
- Recommendations for all external capacitors are:
  - Nominal voltage of 6.3 V, to reduce capacitor drop due to DC biasing effect.
  - Low ESR: < 0.2 Ω on frequency range of 100 kHz − 10 MHz.
  - Cap Type X5R: ±15% variation over temperature => ±35% total cap accuracy.
  - Recommendation of multilayer ceramic caps (i.e. Taiyo Yuden® AMK105BJ225 or Murata™ GRM155C80J225KE95 for 2.2 μF)

RSL20 Block Diagram

The Block Diagram of the RSL20 is shown in Figure 10.

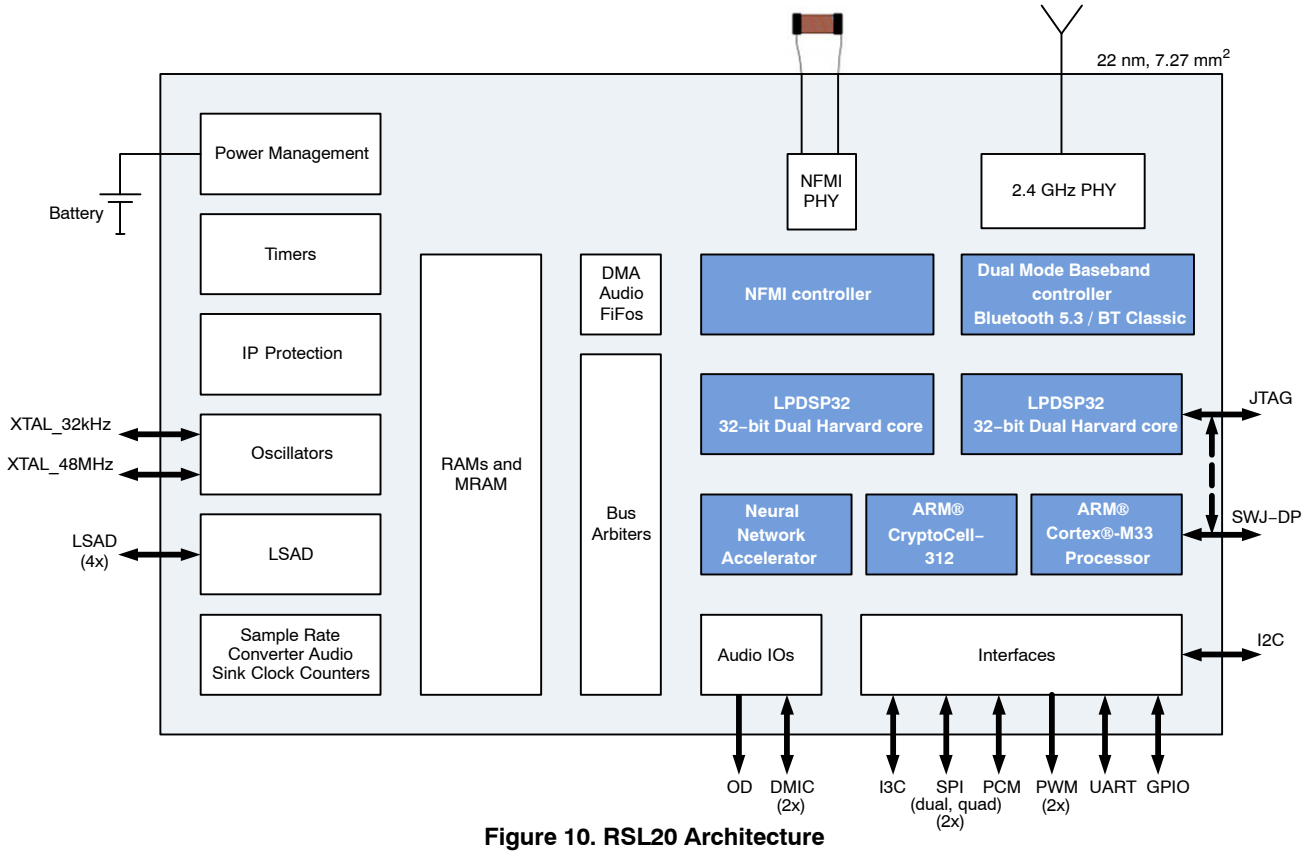


Figure 10. RSL20 Architecture

RSL20 Power Modes

RSL20 supports three power modes:

1. RUN mode: all cores are active with all necessary components under software control.

2. STANDBY mode: optimal for short inactive times.

In this mode:

- The digital core is not clocked and its supply voltage VDDC is reduced to lower the leakage. The whole 587 kB of RAM are in retention state and the MRAM is power off.
- The wake-up can come from an external event on the GPIO pin (GPIO[3:0]) or from an internal counter. At wake-up, the application continues at the point it stopped before the chip was put in standby mode (no full re-boot). The system is able to enter and leave standby mode with minimal delay.

3. SLEEP mode: optimal for the lowest power consumption.

In this mode:

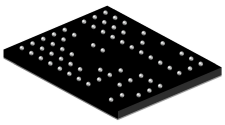
- The digital core, the ROM, the MRAM and the peripheral of the RAMs are powered off. In this mode, the wake-up can come from an external event on the GPIO pin (GPIO[3:0]) or from an internal counter. Also, the whole 587 kB of RAM can be put in retention state (with a granularity of 3 groups of memory) or powered off:
  - When all memories are in retention state, the transition time between SLEEP mode and RUN mode is lower than 200 µs. This mode can be used when the RSL20 is in advertising mode or when RSL20 is in connected to a central device like a phone.
  - When all memories are OFF, the transition time between SLEEP mode and RUN mode is 200 µs (needs further analysis from our side).

Programing the RSL20

It is recommended to use the SWD interface to program the RSL20 in customers' manufacturing line.

REVISION HISTORY

Revision	Description of Changes	Date
0	Production document release.	2/12/2026



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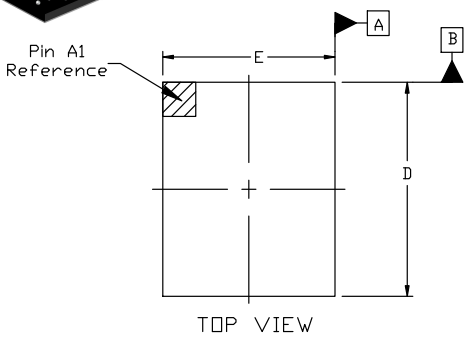
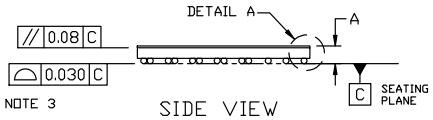
CASE 567XF
ISSUE A

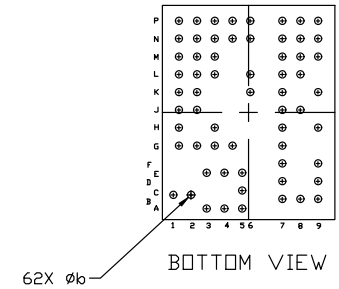
DATE 03 MAR 2023



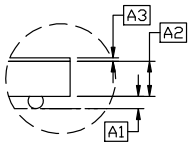
TOP VIEW



SIDE VIEW



BOTTOM VIEW



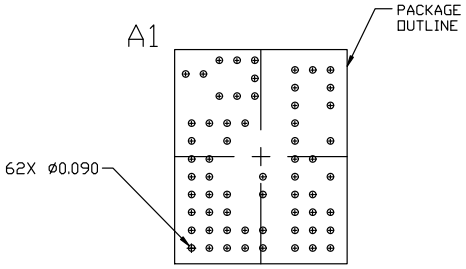
DETAIL A
SCALE 1:3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

BALL POSITION TABLE (MM)					
CENTER OF DIE TO CENTER OF BALL/PAD					
BALL	X	Y	BALL	X	Y
A3	-0.588	-1.348	K6	0.025	0.284
A4	-0.338	-1.348	K7	0.475	0.284
A5	-0.088	-1.348	K9	0.975	0.284
B7	0.475	-1.216	L1	-0.975	0.534
B8	0.725	-1.216	L2	-0.725	0.534
B9	0.975	-1.216	L3	-0.475	0.534
C1	-1.058	-1.158	L6	0.025	0.534
C2	-0.808	-1.158	L7	0.475	0.534
C5	-0.088	-1.098	L8	0.725	0.534
D7	0.475	-0.966	M1	-0.975	0.784
D9	0.975	-0.966	M2	-0.725	0.784
E3	-0.588	-0.848	M3	-0.475	0.784
E4	-0.338	-0.848	M7	0.475	0.784
E5	-0.088	-0.848	M8	0.725	0.784
F7	0.475	-0.716	M9	0.975	0.784
F9	0.975	-0.716	N1	-0.975	1.034
G1	-0.975	-0.466	N2	-0.725	1.034
G2	-0.725	-0.466	N3	-0.475	1.034
G3	-0.475	-0.466	N4	-0.225	1.034
G4	-0.225	-0.466	N6	0.025	1.034
G7	0.475	-0.466	N7	0.475	1.034
H1	-0.975	-0.216	N8	0.725	1.034
H3	-0.475	-0.216	N9	0.975	1.034
H7	0.475	-0.216	P1	-0.975	1.284
H9	0.975	-0.216	P2	-0.725	1.284
J1	-0.975	0.034	P3	-0.475	1.284
J2	-0.725	0.034	P4	-0.225	1.284
J7	0.475	0.034	P6	0.025	1.284
J8	0.725	0.034	P7	0.475	1.284
K1	-0.975	0.284	P8	0.725	1.284
K2	-0.725	0.284	P9	0.975	1.284

MOUNTING PAD POSITION TABLE (MM)					
CENTER OF DIE TO CENTER OF BALL/PAD					
BALL	X	Y	BALL	X	Y
A3	-0.588	1.348	K6	0.025	-0.284
A4	-0.338	1.348	K7	0.475	-0.284
A5	-0.088	1.348	K9	0.975	-0.284
B7	0.475	1.216	L1	-0.975	-0.534
B8	0.725	1.216	L2	-0.725	-0.534
B9	0.975	1.216	L3	-0.475	-0.534
C1	-1.058	1.158	L6	0.025	-0.534
C2	-0.808	1.158	L7	0.475	-0.534
C5	-0.088	1.098	L8	0.725	-0.534
D7	0.475	0.966	M1	-0.975	-0.784
D9	0.975	0.966	M2	-0.725	-0.784
E3	-0.588	0.848	M3	-0.475	-0.784
E4	-0.338	0.848	M7	0.475	-0.784
E5	-0.088	0.848	M8	0.725	-0.784
F7	0.475	0.716	M9	0.975	-0.784
F9	0.975	0.716	N1	-0.975	-1.034
G1	-0.975	0.466	N2	-0.725	-1.034
G2	-0.725	0.466	N3	-0.475	-1.034
G3	-0.475	0.466	N4	-0.225	-1.034
G4	-0.225	0.466	N6	0.025	-1.034
G7	0.475	0.466	N7	0.475	-1.034
H1	-0.975	0.216	N8	0.725	-1.034
H3	-0.475	0.216	N9	0.975	-1.034
H7	0.475	0.216	P1	-0.975	-1.284
H9	0.975	0.216	P2	-0.725	-1.284
J1	-0.975	-0.034	P3	-0.475	-1.284
J2	-0.725	-0.034	P4	-0.225	-1.284
J7	0.475	-0.034	P6	0.025	-1.284
J8	0.725	-0.034	P7	0.475	-1.284
K1	-0.975	-0.284	P8	0.725	-1.284
K2	-0.725	-0.284	P9	0.975	-1.284



RECOMMENDED
MOUNTING FOOTPRINT

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.225	0.250	0.275
A1	0.060	0.075	0.090
A2	0.137	0.150	0.163
A3	0.022	0.025	0.028
b	0.087	0.102	0.117
D	2.979	3.004	3.029
E	2.394	2.419	2.444

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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