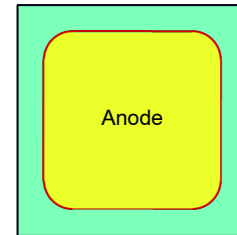


# Silicon Carbide (SiC) Schottky Diode – EliteSiC, 20 A, 650 V, D1, Die

## PCFFS2065AF



### Description

Silicon Carbide (SiC) Schottky Diodes use a completely new technology that provides superior switching performance and higher reliability compared to Silicon. No reverse recovery current, temperature dependent switching characteristics, and excellent thermal performance sets Silicon Carbide as the next generation of power semiconductor. System benefits include highest efficiency, faster operation frequency, increased power density, reduced EMI, and reduced system size and cost.

### Features

- Max Junction Temperature 175°C
- Avalanche Rated 95 mJ
- High Surge Current Capacity
- Positive Temperature Coefficient
- Ease of Paralleling
- No Reverse Recovery/No Forward Recovery

### Applications

- General Purpose
- SMPS, Solar Inverter, UPS
- Power Switching Circuits

### For Additional Product Information and Electrical Characteristics on Package

Refer to [FFSP2065A](#) product datasheet.

### Die Information

- Wafer Diameter: 6 inch
- Die Size: 2,240 × 2,240 μm (include Scribe Lane)
- Metallization:
  - ◆ Top: Ti/TiN/AICu 4 μm
  - ◆ Back: Ti/NiV/Ag
- Die Thickness: Typ. 200 μm
- Bonding Pad Size:
  - ◆ Anode: 1,880 × 1,880 μm
- Recommended Wire Bond\*
  - ◆ Anode: 15mil × 2

\*Based on TO-220 package of onsemi

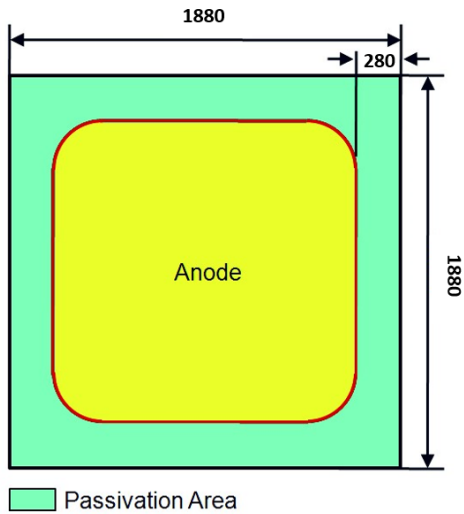
### ELECTRICAL CHARACTERISTICS ON WAFER ( $T_C = 25^\circ\text{C}$ unless otherwise noted) (Note 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_R$	Reverse Blocking Voltage	$I_R = 200 \mu\text{A}$ , $T_C = 25^\circ\text{C}$	650	–	–	V
$V_F$	Forward Voltage	$I_F = 20 \text{ A}$ , $T_C = 25^\circ\text{C}$	1.20	–	1.75	V
$I_R$	Reverse Current	$V_R = 650 \text{ V}$ , $T_C = 25^\circ\text{C}$	–	–	200	$\mu\text{A}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Tested 100% on wafer

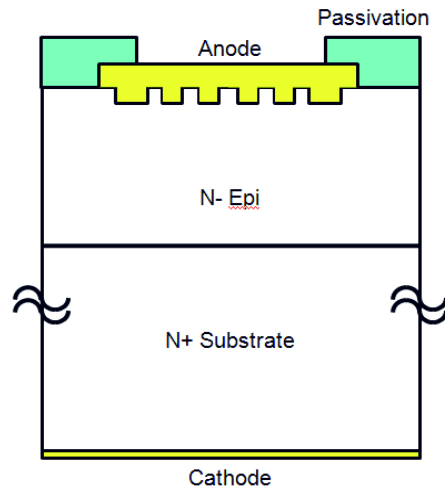
**Die Layout**  
(Dimension:  $\mu\text{m}$ , except Scribe Lane)



**Passivation Information**

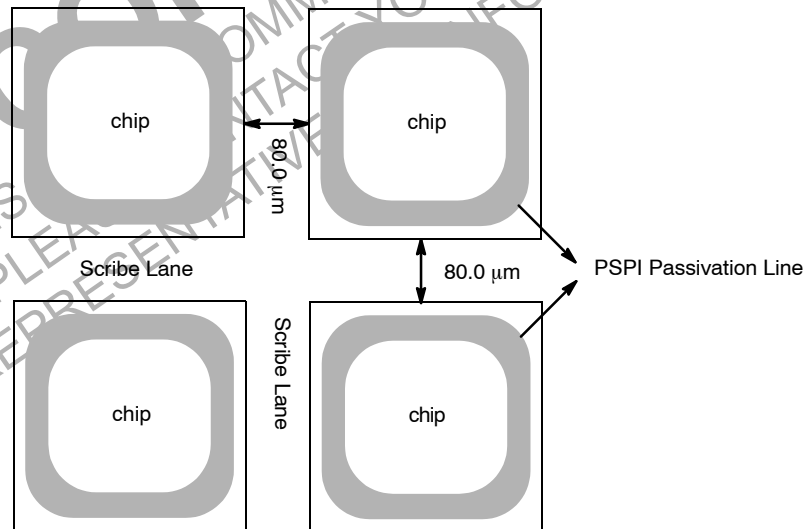
- Passivation Material: Polyimide (PSPI)
- Passivation Type: Local Passivation
- Passivation Thickness: 90KA

**Cross Section**



**The Configuration of Chips**

(Based on 6 inch Wafer)



Sawn-on-film frame packing based on tested wafer

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