NXH160T120L2Q1PG, NXH160T120L2Q1SG

Q1PACK Module

This high−density, integrated power module combines high−performance IGBTs with rugged anti−parallel diodes.

Features

- Extremely Efficient Trench with Fieldstop Technology
- Low Switching Loss Reduces System Power Dissipation
- Module Design Offers High Power Density
- Low Inductive Layout
- Q1PACK Package with Press−Fit and Solder Pins

Typical Applications

- Solar Inverters
- Uninterruptable Power Supplies

ON Semiconductor®

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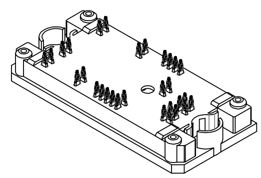
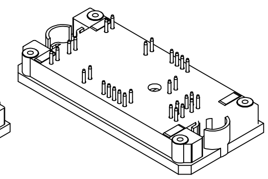
PACKAGE PICTURE

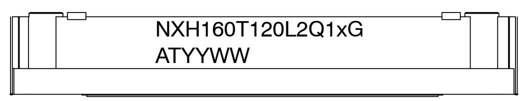


Q1PACK
CASE 180AD
PRESS FIT



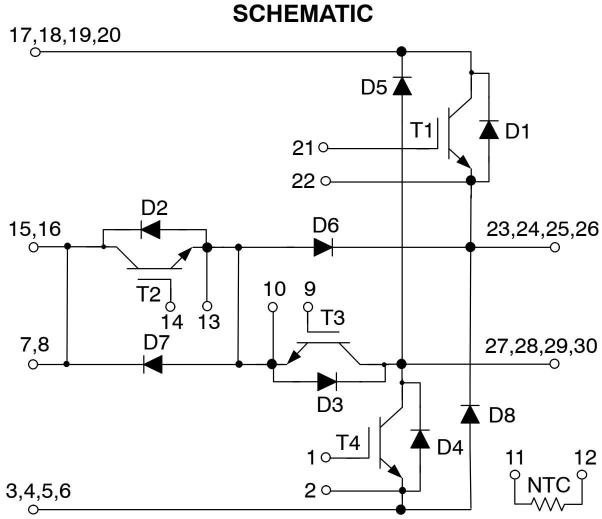
Q1PACK
CASE 180AQ
SOLDER PINS

DEVICE MARKING

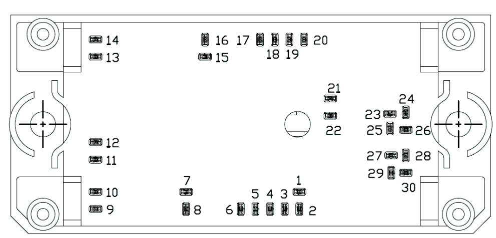


x = P or S
G = Pb−Free Package
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

SCHEMATIC



PIN ASSIGNMENTS



ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

Table 1. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
HALFBRIDGE IGBT INVERSE DIODE (D1, D4)			
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Forward Current, DC @ T_h = 80°C	I_F	20	A
Repetitive Peak Forward Current T_{pulse} limited by T_{jmax}	I_{FRM}	80	A
Power Dissipation per Diode $T_j = T_{jmax}$ T_h = 80°C	P_{tot}	51	W
Maximum Junction Temperature	T_J	150	°C
HALFBRIDGE IGBT (T1, T4)			
Collector−emitter voltage	V_{CES}	1200	V
Collector current @ T_h = 80°C	I_C	140	A
Pulsed Collector Current, T_{pulse} Limited by T_{jmax}	I_{CM}	480	A
Power Dissipation per IGBT $T_j = T_{jmax}$ T_h = 80°C	P_{tot}	280	W
Gate−emitter voltage	V_{GE}	±20	V
Short Circuit Withstand Time V_{GE} = 15 V, V_{CE} = 600 V, $T_J \le$ 150°C	T_{SC}	10	µs
Maximum Junction Temperature	T_J	150	°C
NP DIODE (D6, D7)			
Peak Repetitive Reverse Voltage	V_{RRM}	650	V
Forward Current, DC @ T_h = 80°C	I_F	58	A
Repetitive Peak Forward Current, T_{pulse} limited by T_{Jmax}	I_{FRM}	200	A
Power Dissipation Per Diode $T_j = T_{jmax}$ T_h = 80°C	P_{tot}	89	W
Maximum Junction Temperature	T_J	150	°C
NP IGBT (T2, T3)			
Collector−emitter voltage	V_{CES}	650	V
Collector current @ T_h = 80°C	I_C	83	A
Pulsed collector current, T_{pulse} limited by T_{Jmax}	I_{CM}	235	A
Power Dissipation Per IGBT $T_j = T_{jmax}$ T_h = 80°C	P_{tot}	117	W
Gate−emitter voltage	V_{GE}	±20	V
Short Circuit Withstand Time V_{GE} = 15 V, V_{CE} = 400 V, $T_J \le$ 150°C	T_{sc}	5	µs
Maximum Junction Temperature	T_J	150	°C
NP INVERSE DIODE (D2, D3)			
Peak Repetitive Reverse Voltage	V_{RRM}	650	V
Forward Current, DC @ T_h = 80°C	I_F	17	A
Repetitive Peak Forward Current, T_{pulse} limited by T_{Jmax}	I_{FRM}	68	A
Power Dissipation Per Diode $T_j = T_{jmax}$ T_h = 80°C	P_{tot}	28	W
Maximum Junction Temperature	T_J	150	°C
HALFBRIDGE DIODE (D5, D8)			
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Forward Current, DC @ T_h = 80°C (per diode)	I_F	45	A
Repetitive Peak Forward Current, T_{pulse} limited by T_{Jmax}	I_{FRM}	180	A
Power Dissipation Per Diode $T_j = T_{jmax}$ T_h = 80°C	P_{tot}	78	W

Table 1. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
HALFBRIDGE DIODE (D5, D8)			
Junction Temperature	T_J	150	°C
THERMAL PROPERTIES			
Operating Temperature under switching condition	$T_{VJ\ OP}$	−40 to (T_{jmax}−25)	°C
Storage Temperature range	T_{stg}	−40 to 125	°C
INSULATION PROPERTIES			
Isolation test voltage, t = 1 sec, 60 Hz/50 Hz	V_{is}	3000	V_{RMS}
Creepage distance		12.7	mm
Clearance		8.06	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
HALFBRIDGE IGBT INVERSE DIODE (D1, D4) CHARACTERISTICS						
Forward voltage	I_F = 7 A, T_j = 25°C I_F = 7 A, T_j = 125°C	V_F	– –	1.46 1.49	2.7 –	V
Thermal Resistance − chip−to−heatsink	Thermal grease, Thickness = 2 Mil ± 2%, λ = 1 W/mK	R_{thJH}		1.864		°C/W
HALFBRIDGE IGBT (T1, T4) CHARACTERISTICS						
Collector−emitter saturation voltage	V_{GE} = 15 V, I_C = 160 A, T_j = 25°C V_{GE} = 15 V, I_C = 160 A, T_j = 125°C	$V_{CE(sat)}$	– –	2.06 2.10	2.50 –	V
Gate−emitter threshold voltage	V_{GE} = V_{CE}, I_C = 6 mA	$V_{GE(TH)}$	5.0	5.80	6.50	V
Collector−emitter cutoff current	V_{GE} = 0 V, V_{CE} = 1200 V	I_{CES}	–	–	800	μA
Gate leakage current	V_{GE} = 20 V, V_{CE} = 0 V	I_{GES}	–	–	800	nA
Turn−on delay time	T_j = 125°C V_{CE} = 350 V, I_C = 100 A V_{GE} = ±15 V, R_G = 4 Ω	$t_{d(on)}$	–	55	–	ns
Rise time		t_r	–	50	–	
Turn−off delay time		$t_{d(off)}$	–	430	–	
Fall time		t_f	–	105	–	
Turn on switching loss		E_{on}	–	2.73	–	mJ
Turn off switching loss		E_{off}	–	3.58	–	
Input capacitance	V_{CE} =25 V. V_{GE} = 0 V. f = 10 kHz	C_{ies}	–	38164	–	pF
Output capacitance		C_{oes}	–	644	–	
Reverse transfer capacitance		C_{res}	–	784	–	
Gate charge total	V_{CE} = 600 V, I_C = 160 A, V_{GE} = 15 V	Q_g	–	1664	–	nC
Thermal Resistance − chip−to−heatsink	Thermal grease, Thickness = 2 Mil ± 2%, λ = 1 W/mK	R_{thJH}		0.337		°C/W
NP DIODE (D6, D7) CHARACTERISTICS						
Forward voltage	V_{GE} = 0 V, I_F = 150 A, T_j = 25°C V_{GE} = 0 V, I_F = 150 A, T_j = 125°C	V_F	– –	2.15 2.36	2.60 –	V
Reverse leakage current	V_{CE} = 650 V, V_{GE} = 0 V	Ir	–	–	200	μA
Reverse recovery time	T_j = 125°C V_{CE} = 350 V, I_C = 100 A V_{GE} = ±15 V, R_G = 4 Ω	trr	–	225	–	ns
Reverse recovery charge		Qrr	–	6.15	–	μC
Peak reverse recovery current		Irrm	–	85	–	A
Peak rate of fall of recovery current		di/dtmax	–	1315	–	A/μs
Reverse recovery energy		Err	–	1.336	–	mJ
Thermal Resistance − chip−to−heatsink	Thermal grease, Thickness = 2 Mil ± 2%, λ = 1 W/mK	RthJH	–	1.07	–	°C/W

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
NP IGBT (T2, T3)						
Collector−emitter saturation voltage	V_{CE} = 15 V, I_C = 150 A, T_j = 25°C V_{CE} = 15 V, I_C = 150 A, T_j = 125°C	$V_{CE(sat)}$	– –	1.65 1.84	2.0 –	V
Gate−emitter threshold voltage	V_{GE} = V_{CE}, I_C = 8 mA	$V_{GE(TH)}$	5.0	6.10	6.90	V
Collector−emitter cutoff current	V_{GE} = 0 V, V_{CE} = 650 V	I_{CES}	–	–	400	μA
Gate leakage current	V_{GE} = 20 V, V_{CE} = 0 V	I_{GES}	–	–	800	nA
Turn−on delay time	T_j = 125°C V_{CE} = 350 V, I_C = 100 A V_{GE} = ±15 V, R_G = 4 Ω	$t_{d(on)}$	–	46	–	ns
Rise time		t_r	–	48	–	
Turn−off delay time		$t_{d(off)}$	–	250	–	
Fall time		t_f	–	105	–	
Turn on switching loss		E_{on}	–	1.245	–	mJ
Turn off switching loss		E_{off}	–	2.525	–	
Input capacitance	V_{CE} = 25 V, V_{GE} = 0 V, f = 10 kHz	C_{ies}	–	19380	–	pF
Output capacitance		C_{oes}	–	570	–	
Reverse transfer capacitance		C_{res}	–	496	–	
Gate charge total	V_{CE} = 480 V, I_C = 150 A, V_{GE} = 15 V	Q_g	–	790	–	nC
Thermal Resistance − chip−to−heatsink	Thermal grease, Thickness = 2 Mil ± 2%, λ = 1 W/mK	R_{thJH}	–	0.81	–	°C/W
NP INVERSE DIODE (D2, D3)						
Forward voltage	V_{GE} = 0 V, I_F = 15 A, T_j = 25°C V_{GE} = 0 V, I_F = 15 A, T_j = 125°C	V_F	– –	1.60 1.59	2.20 –	V
Thermal Resistance − chip−to−heatsink	Thermal grease, Thickness = 2 Mil ± 2%, λ = 1 W/mK	R_{thJH}		3.43		°C/W
HALFBRIDGE DIODE (D5, D8)						
Forward voltage	V_{GE} = 0 V, I_F = 150 A, T_j = 25°C V_{GE} = 0 V, I_F = 150 A, T_j = 125°C	V_F	– –	2.50 2.80	3.50 –	V
Reverse leakage current	V_{CE} = 1200 V, V_{GE} = 0 V	Ir	–	–	200	μA
Reverse recovery time	T_j = 125°C V_{CE} = 350 V, I_C = 100 A V_{GE} = ±15 V, R_G = 4 Ω	trr	–	405	–	ns
Reverse recovery charge		Qrr	–	15.5	–	μC
Peak reverse recovery current		Irrm	–	220	–	A
Peak rate of fall of recovery current		di/dtmax	–	5440	–	A/μs
Reverse recovery energy		Err	–	5.225	–	mJ
Thermal Resistance − chip−to−heatsink	Thermal grease, Thickness = 2 Mil ± 2%, λ = 1 W/mK	RthJH	–	1.213	–	°C/W
THERMISTOR CHARACTERISTICS						
Nominal resistance		R_{25}	–	22	–	kΩ
Nominal resistance	T = 100°C	R_{100}	–	1486	–	Ω
Deviation of R25		DR/R	−5	–	5	%
Power dissipation		P_D	–	200	–	mW
Power dissipation constant			–	2	–	mW/K
B−value	B(25/50), tol ±3%		–	3950	–	K
B−value	B(25/100), tol ±3%		–	3998	–	K

TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT AND NEUTRAL POINT FORWARD DIODE

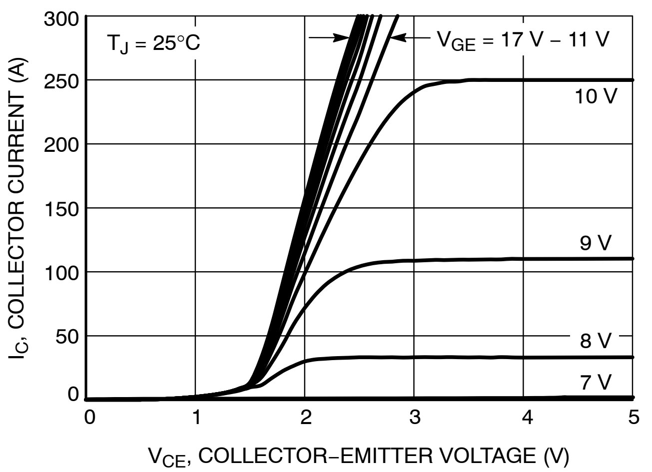


Figure 1. Typical Output Characteristics

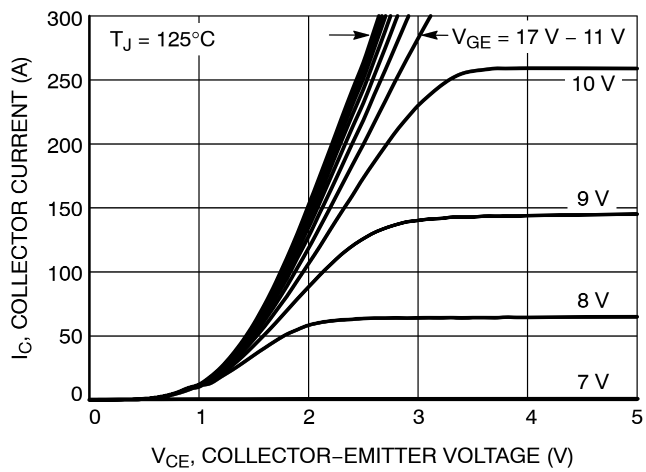


Figure 2. Typical Output Characteristics

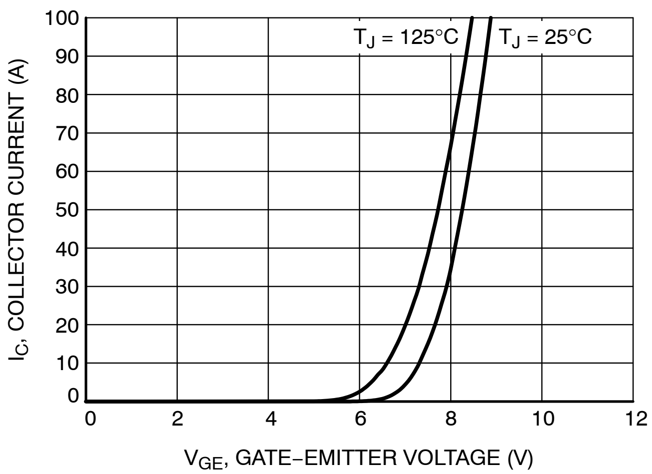


Figure 3. Typical Transfer Characteristics

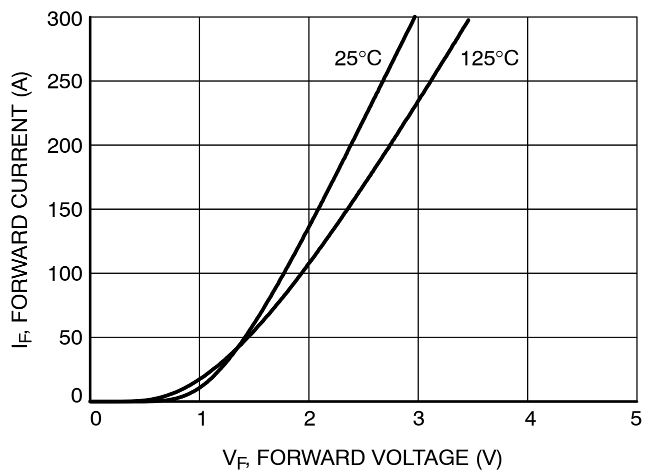


Figure 4. Diode Forward Characteristics

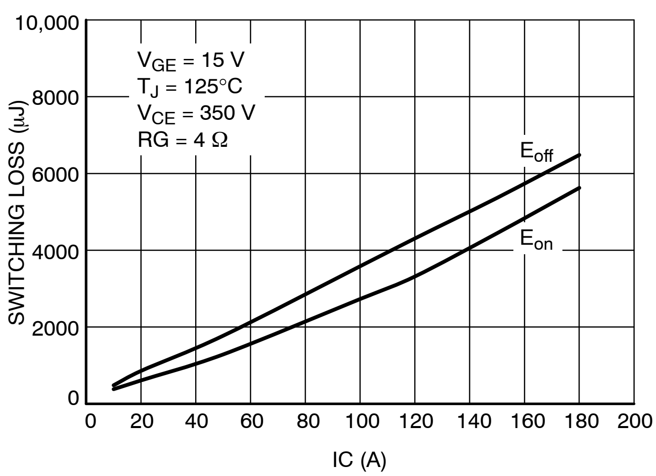


Figure 5. Typical Switching Loss vs. IC

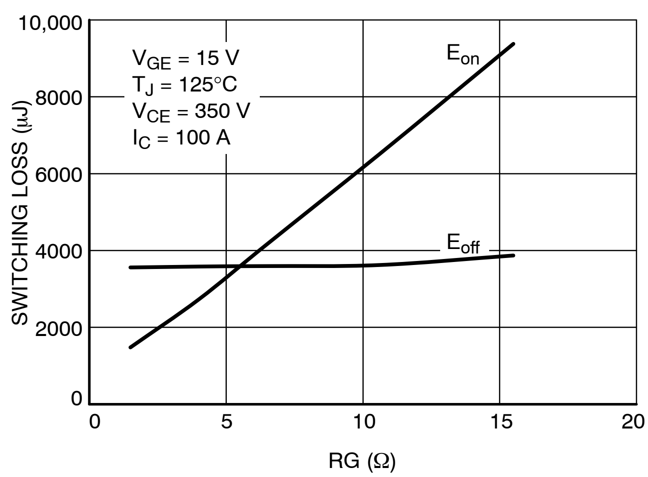


Figure 6. Typical Switching Loss vs. RG

TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT AND NEUTRAL POINT FORWARD DIODE

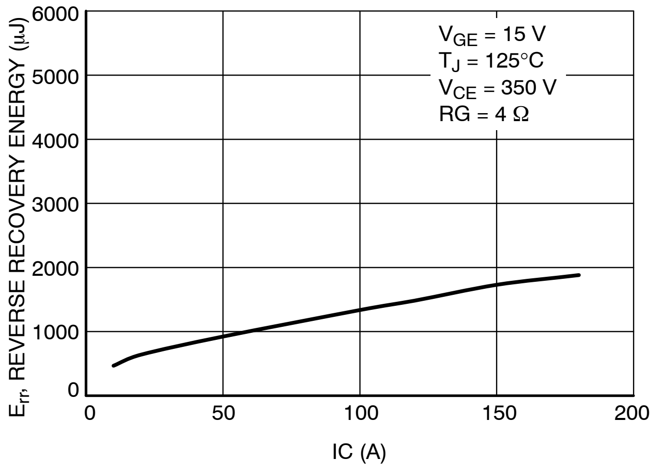


Figure 7. Typical Reverse Recovery Energy Loss vs. IC

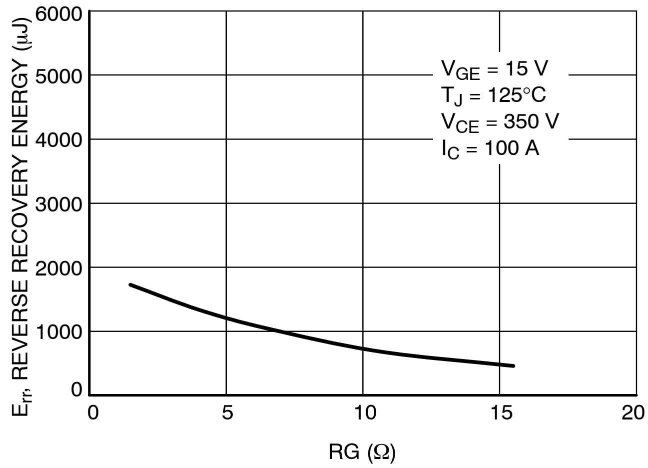


Figure 8. Typical Reverse Recovery Energy Loss vs. RG

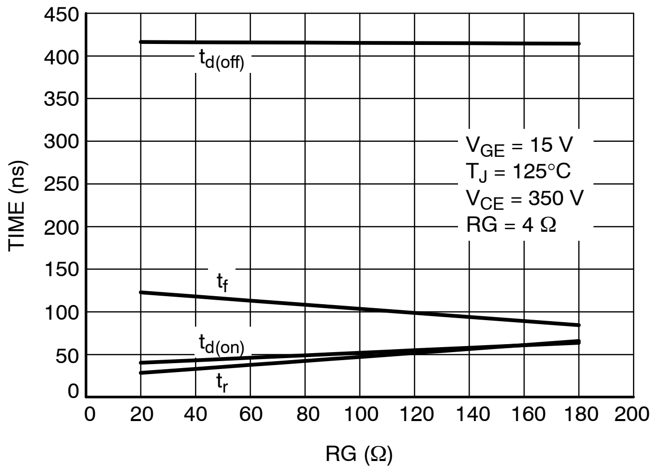


Figure 9. Typical Switching Time vs. IC

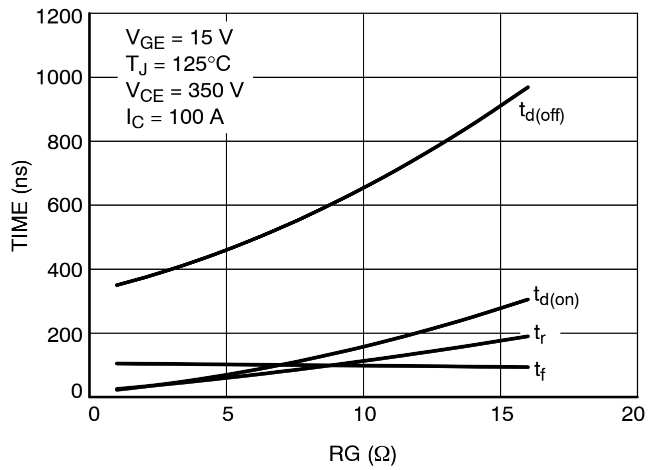


Figure 10. Typical Switching Time vs. RG

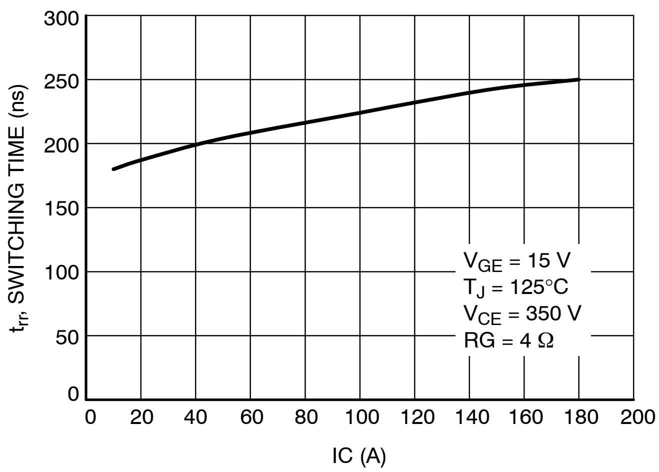


Figure 11. Typical Reverse Recovery Time vs. IC

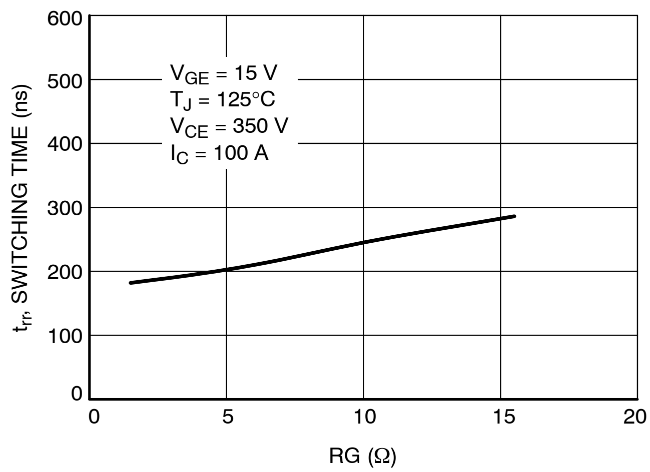


Figure 12. Typical Reverse Recovery Time vs. RG

TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT AND NEUTRAL POINT FORWARD DIODE

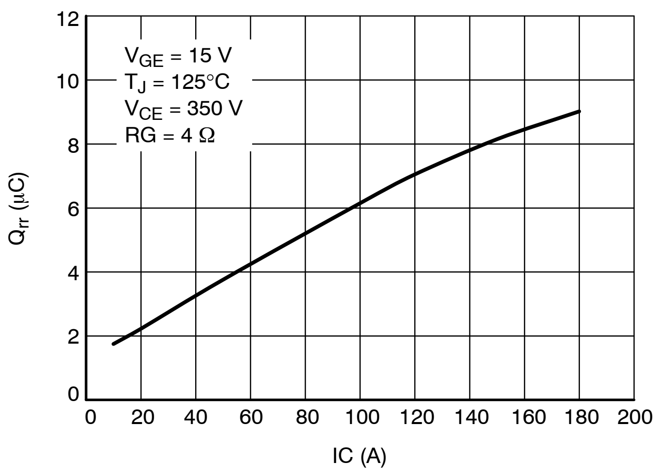


Figure 13. Typical Reverse Recovery Charge vs. IC

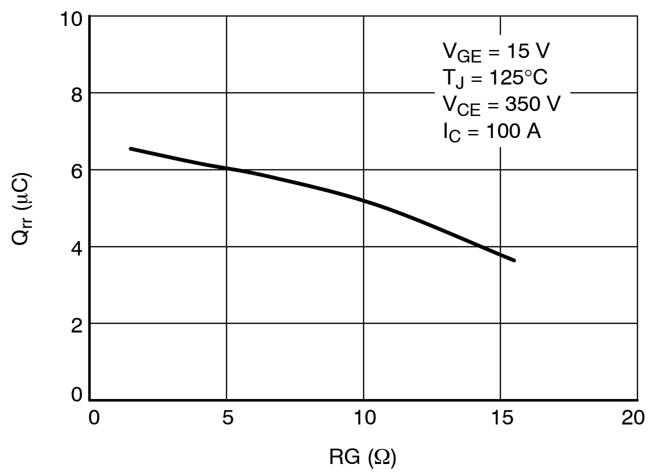


Figure 14. Typical Reverse Recovery Charge vs. RG

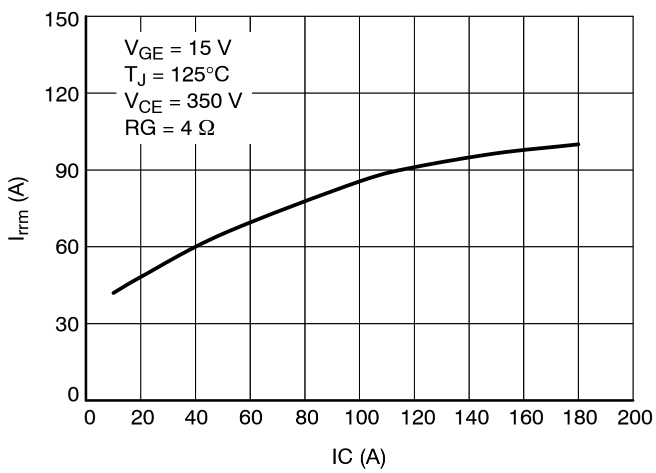


Figure 15. Typical Reverse Recovery Current vs. IC

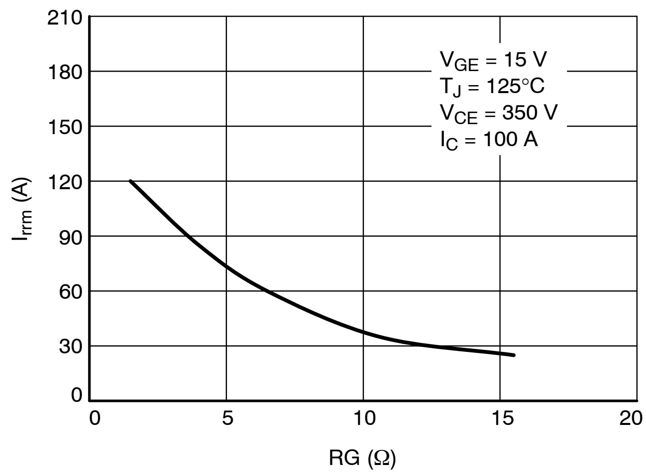


Figure 16. Typical Reverse Recovery Current vs. RG

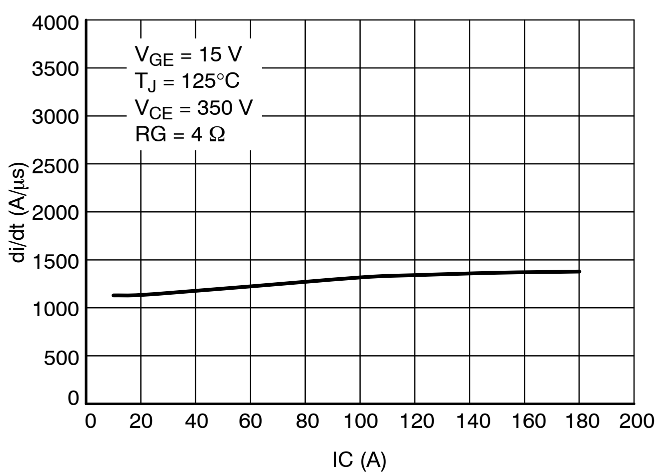


Figure 17. Typical di/dt vs. IC

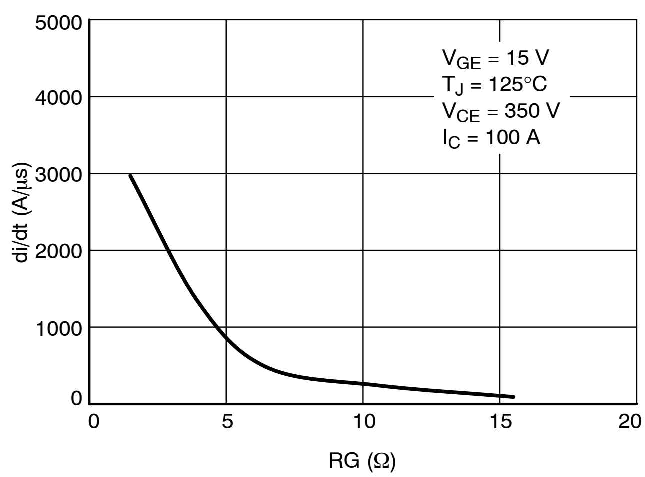


Figure 18. Typical di/dt vs. RG

TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT AND NEUTRAL POINT FORWARD DIODE

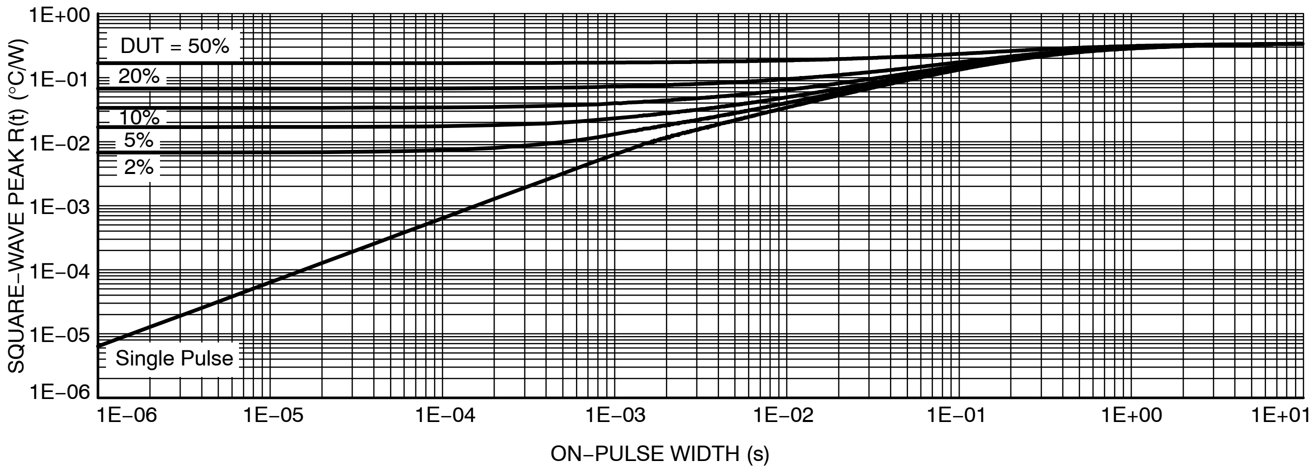


Figure 19. Transient Thermal Impedance (Half Bridge IGBT)

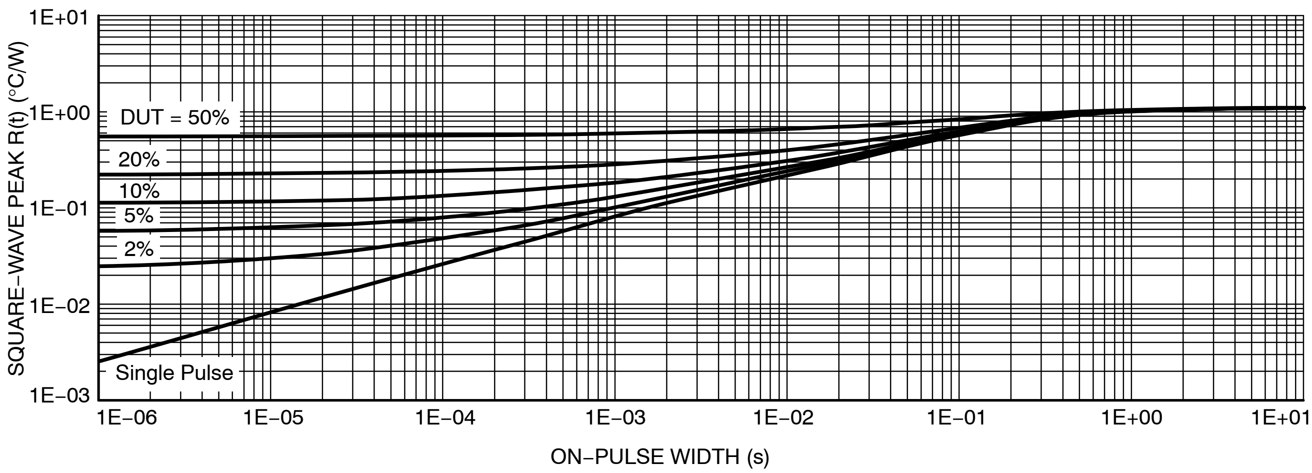


Figure 20. Transient Thermal Impedance (Neutral Point Forward Diode)

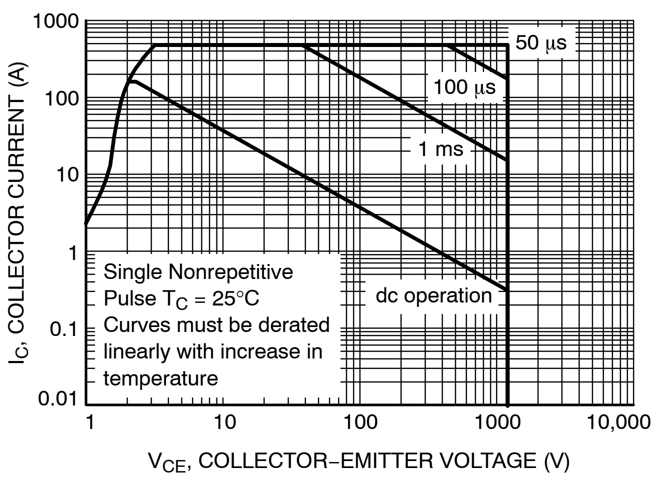


Figure 21. Safe Operating Area

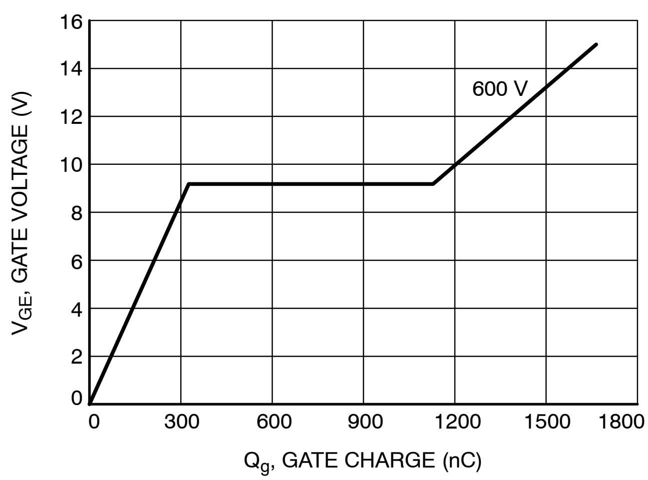


Figure 22. Gate Voltage vs. Gate Charge

TYPICAL CHARACTERISTICS – NEUTRAL POINT IGBT AND HALF BRIDGE FORWARD DIODE

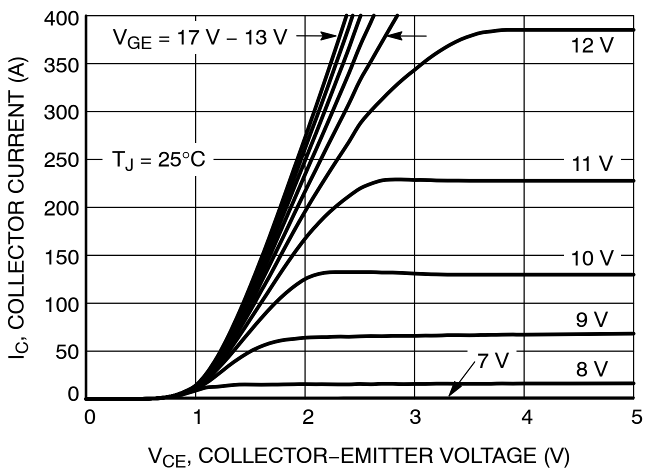


Figure 23. Typical Output Characteristics

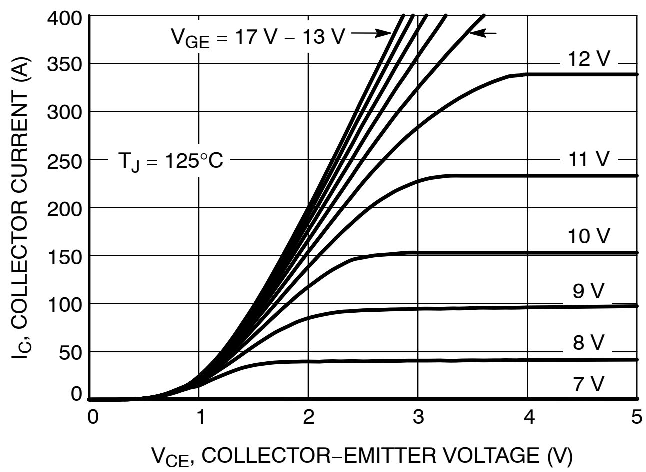


Figure 24. Typical Output Characteristics

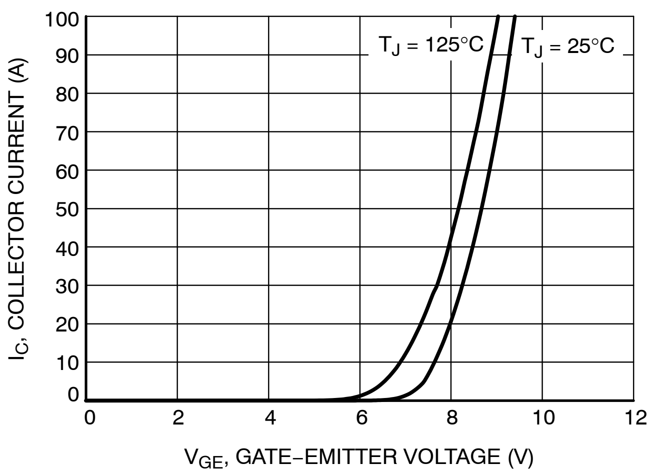


Figure 25. Typical Transfer Characteristics

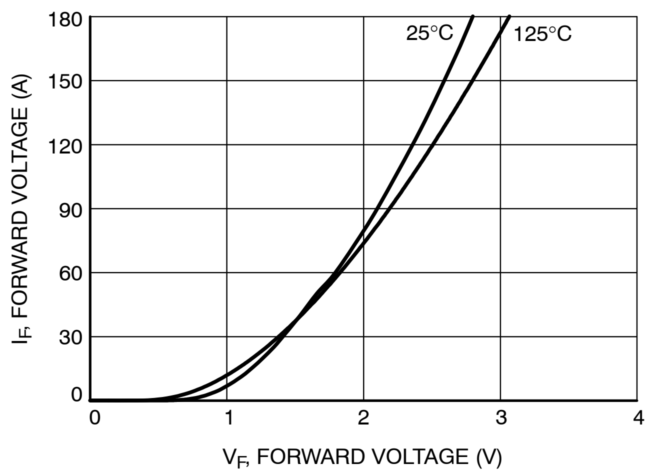


Figure 26. Diode Forward Characteristics

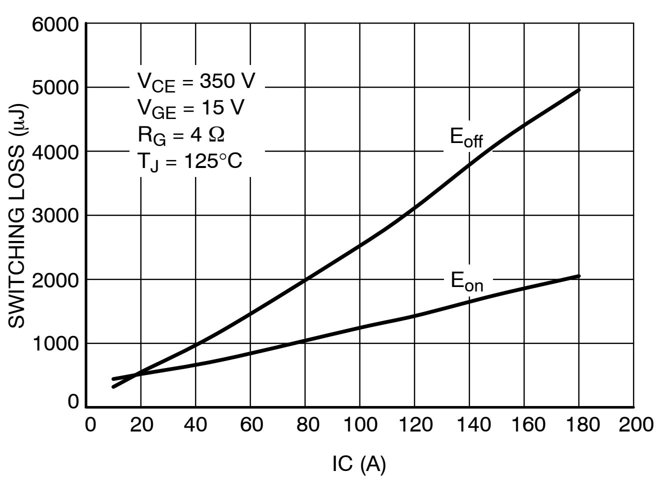


Figure 27. Typical Switching Loss vs. IC

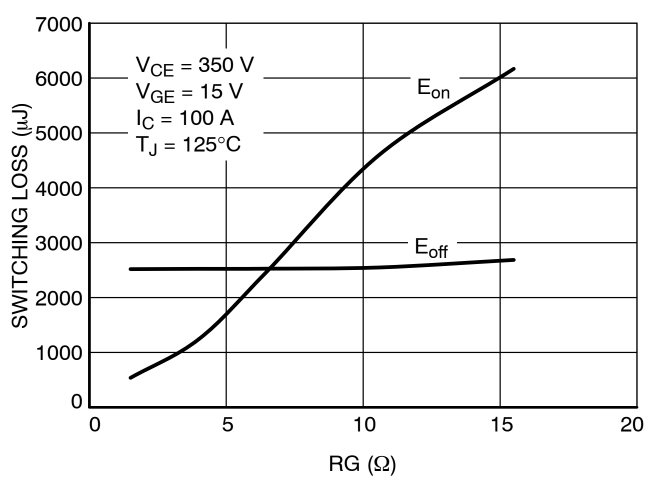


Figure 28. Typical Switching Loss vs. RG

TYPICAL CHARACTERISTICS – NEUTRAL POINT IGBT AND HALF BRIDGE FORWARD DIODE

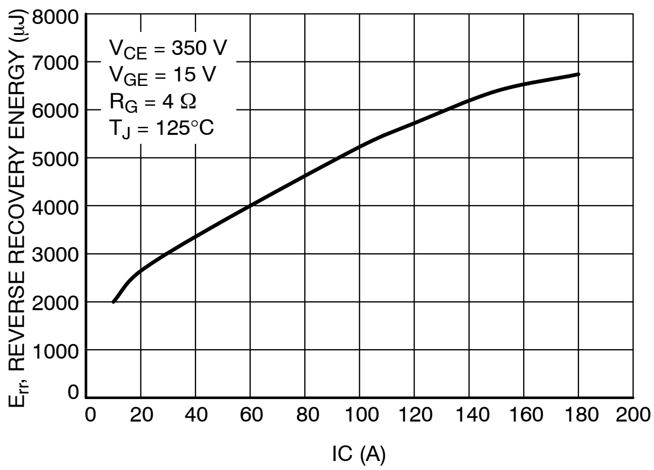


Figure 29. Typical Reverse Recovery Energy Loss vs. IC

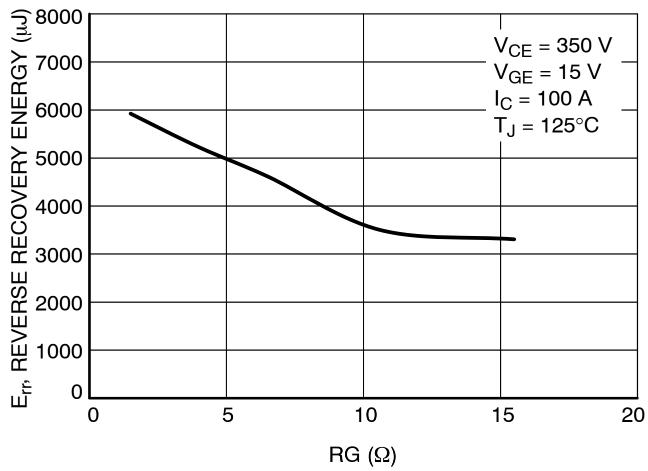


Figure 30. Typical Reverse Recovery Energy Loss vs. RG

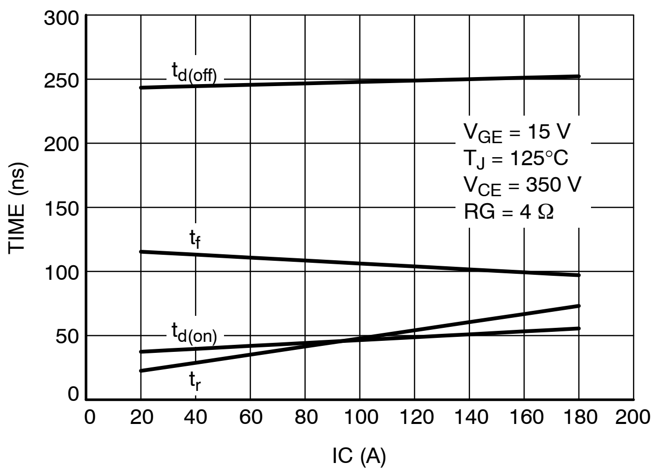


Figure 31. Typical Switching Time vs. IC

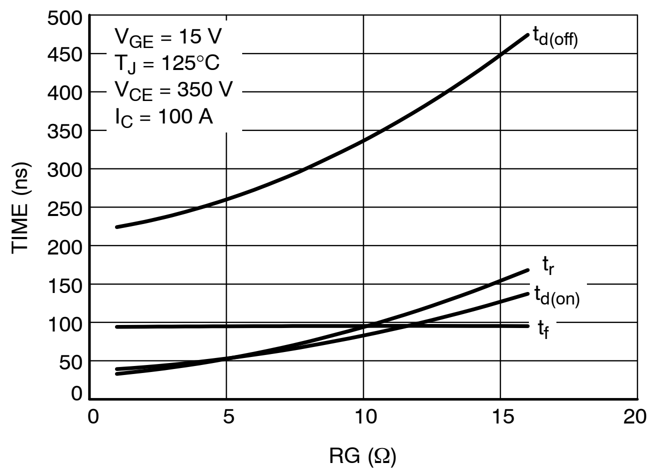


Figure 32. Typical Switching Time vs. RG

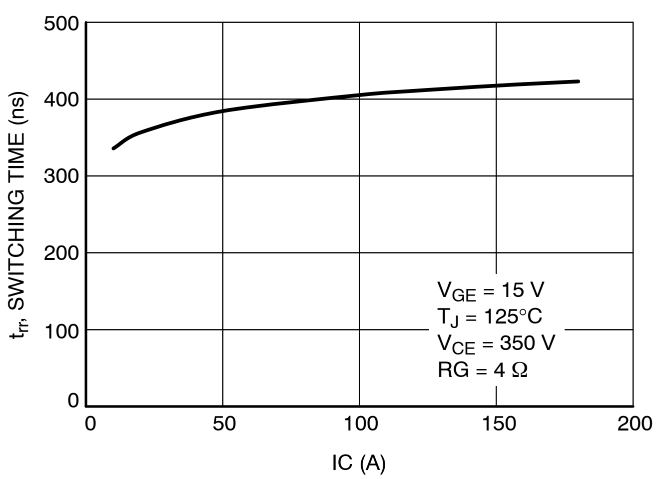


Figure 33. Half Bridge Forward Diode Typical Reverse Recovery Time vs. IC

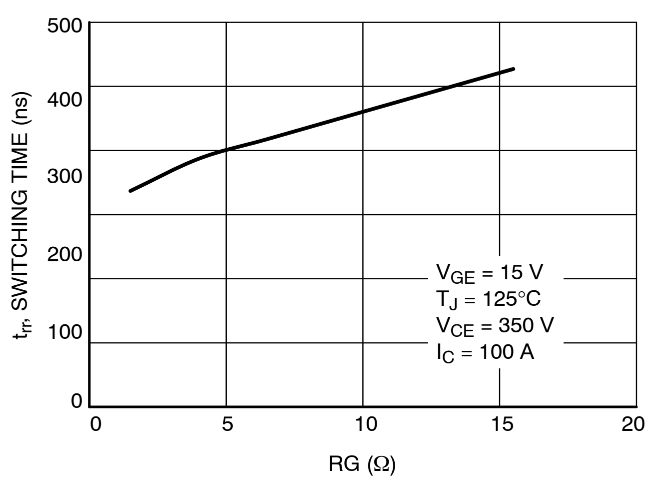


Figure 34. Half Bridge Forward Diode Typical Reverse Recovery Time vs. RG

TYPICAL CHARACTERISTICS – NEUTRAL POINT IGBT AND HALF BRIDGE FORWARD DIODE

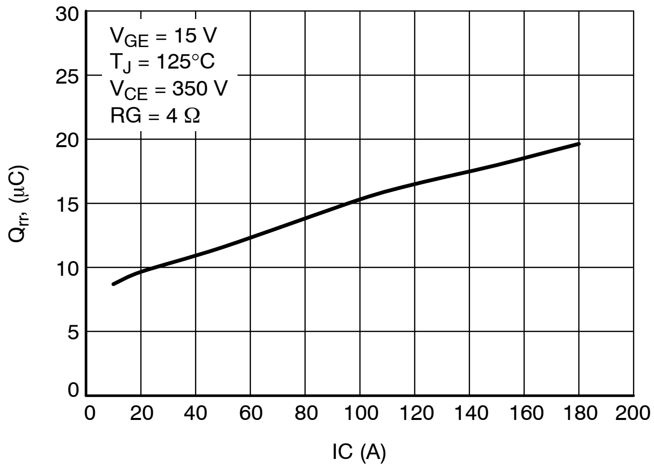


Figure 35. Half Bridge Forward Diode Typical Reverse Recovery Charge vs. IC

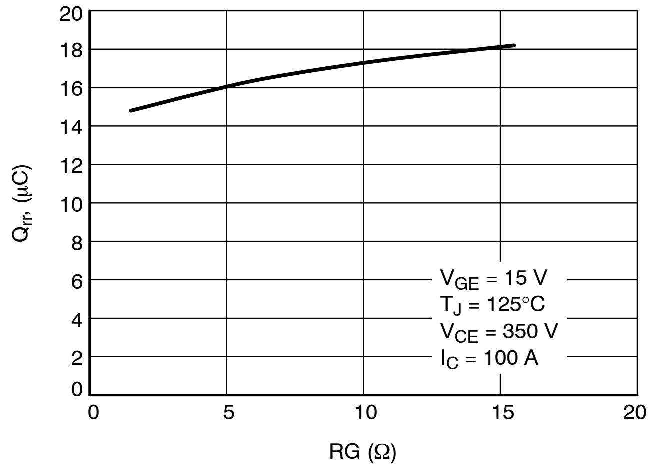


Figure 36. Half Bridge Forward Diode Typical Reverse Recovery Charge vs. RG

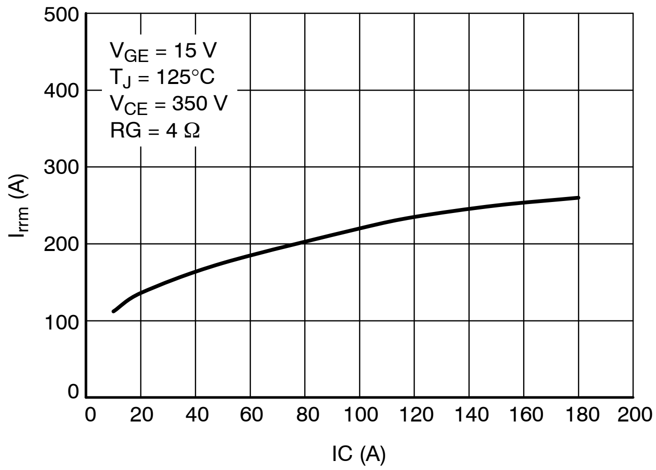


Figure 37. Typical Reverse Recovery Current vs. IC

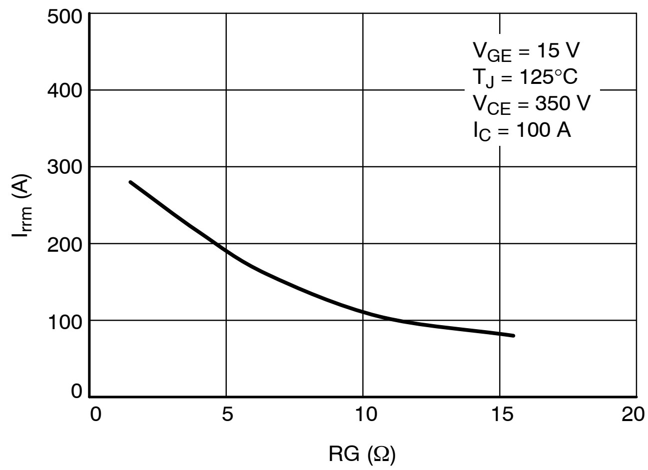


Figure 38. Typical Reverse Recovery Current vs. RG

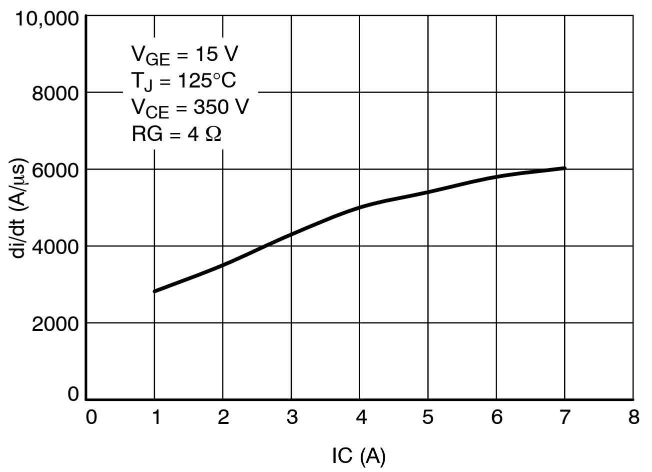


Figure 39. Typical di/dt vs. IC

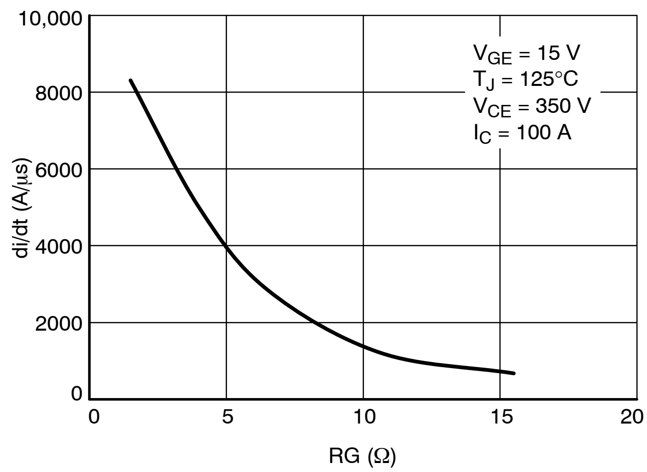


Figure 40. Typical di/dt vs. RG

TYPICAL CHARACTERISTICS – NEUTRAL POINT IGBT AND HALF BRIDGE FORWARD DIODE

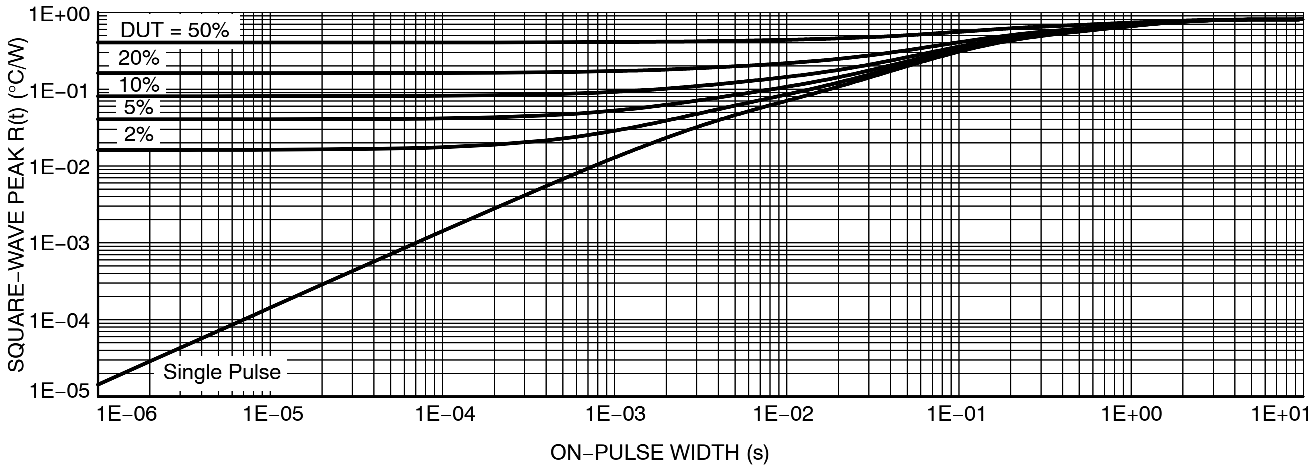


Figure 41. Transient Thermal Impedance (Neutral Point IGBT)

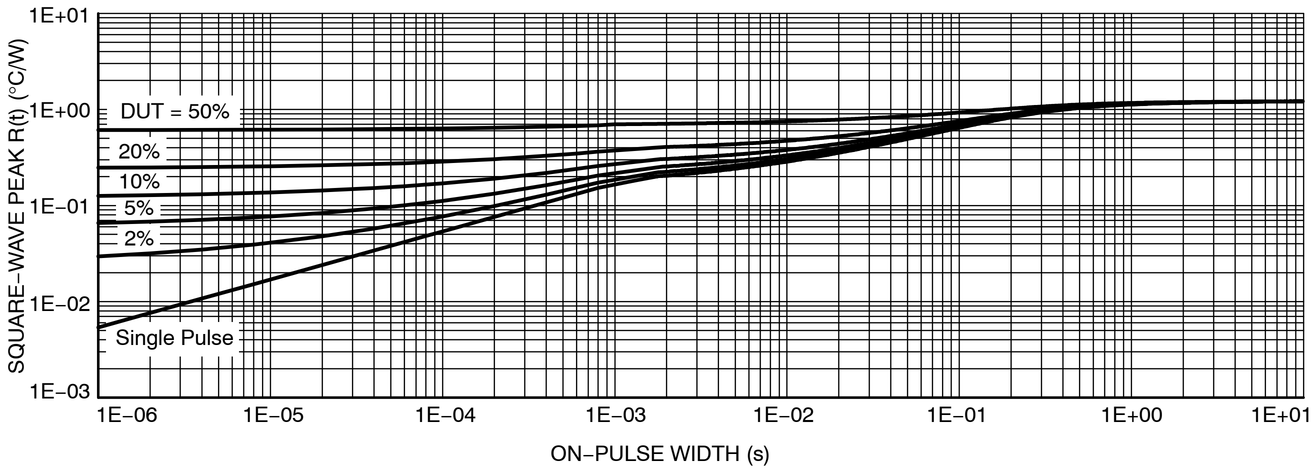


Figure 42. Transient Thermal Impedance (Half Bridge Forward Diode)

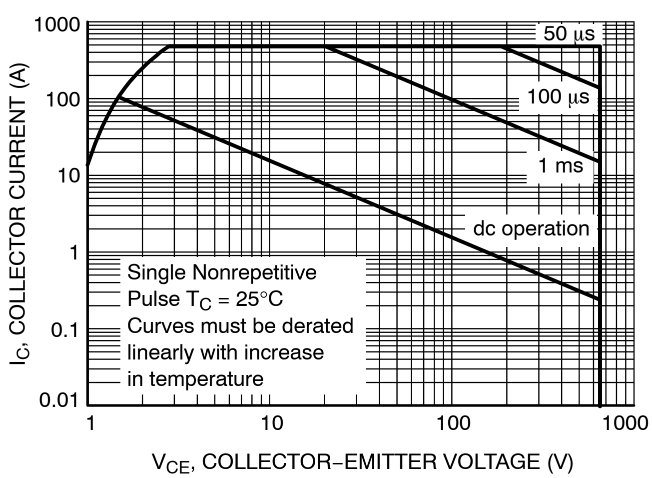


Figure 43. Safe Operating Area

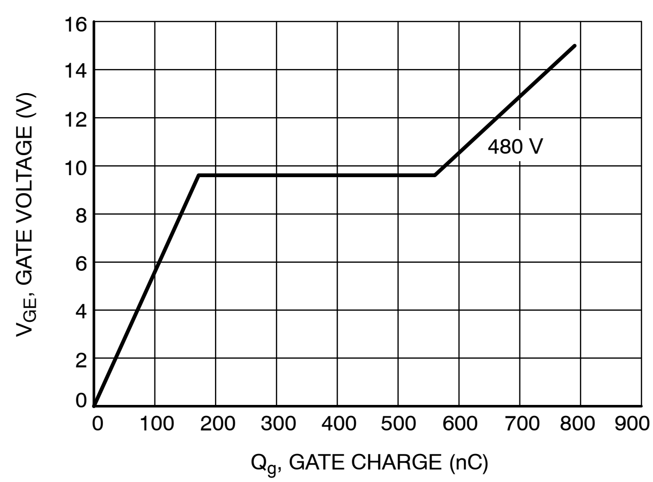


Figure 44. Gate Voltage vs. Gate Charge

TYPICAL CHARACTERISTICS – HALF BRIDGE INVERSE DIODE

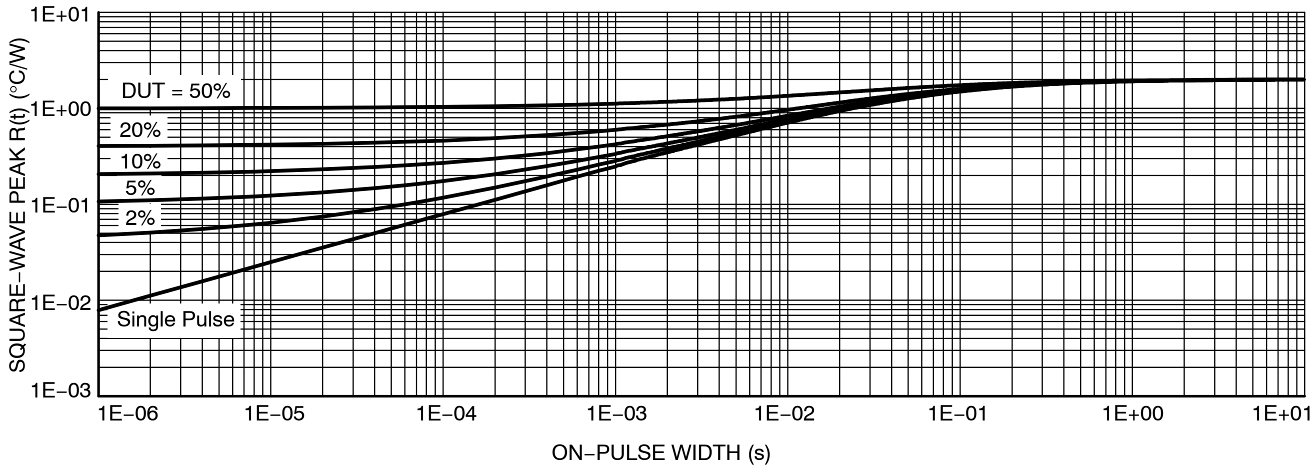


Figure 45. Transient Thermal Impedance

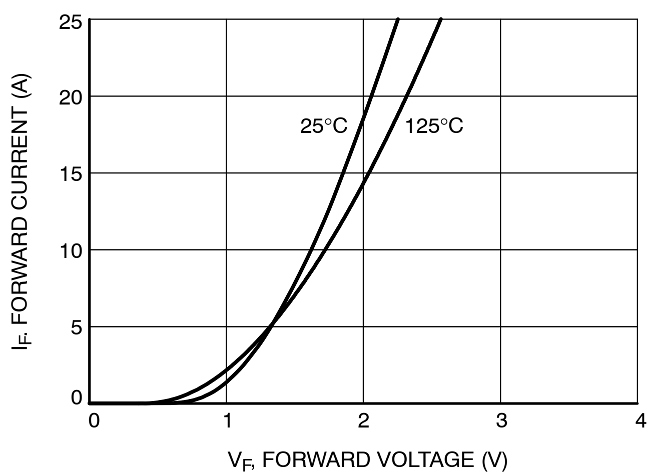


Figure 46. Diode Forward Characteristics

TYPICAL CHARACTERISTICS – NEUTRAL POINT INVERSE DIODE

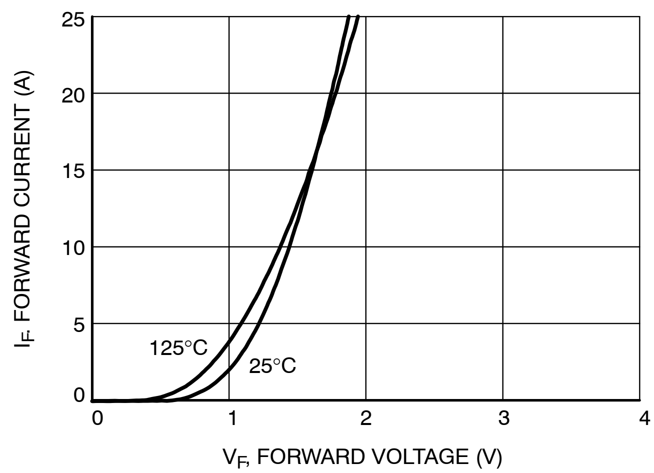


Figure 47. Diode Forward Characteristics

TYPICAL CHARACTERISTICS – THERMISTOR

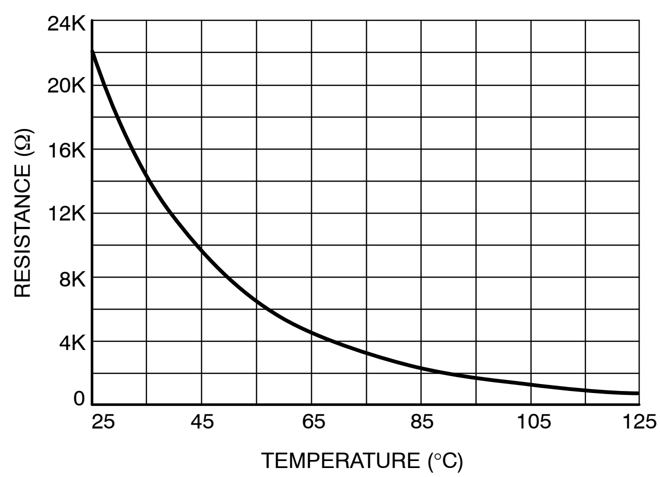


Figure 48. Thermistor Characteristics

ORDERING INFORMATION

Orderable Part Number	Package	Shipping
NXH160T120L2Q1PG (Press Fit)	Q1PACK – Case 180AD (Pb−Free and Halide−Free)	21 Units / Blister Tray
NXH160T120L2Q1SG (Solder Pin)	Q1PACK – Case 180AQ (Pb−Free and Halide−Free)	21 Units / Blister Tray

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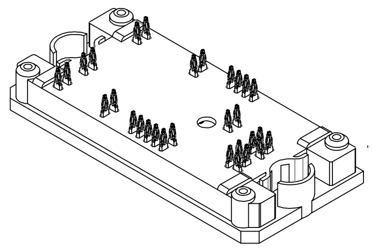
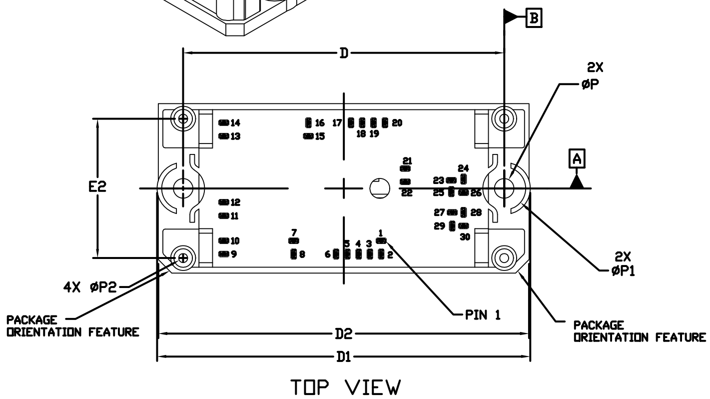
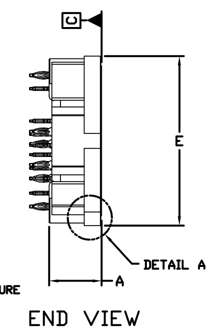
PIM30, 71x37.4
CASE 180AD
ISSUE E

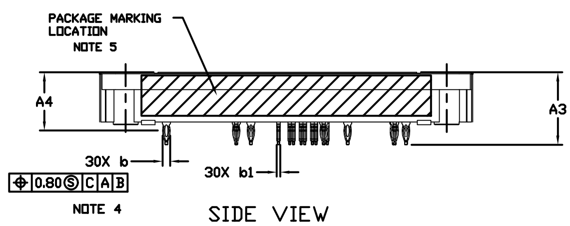
DATE 28 NOV 2017

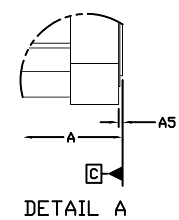






MOUNTING HOLE POSITION			MOUNTING HOLE POSITION		
PIN	X	Y	PIN	X	
1	8.30	11.55	16	−7.800	−14.50
2	8.30	14.50	17	1.60	−14.50
3	5.80	14.50	18	4.10	−14.50
4	3.30	14.50	19	6.60	−14.50
5	0.80	14.50	20	9.10	−14.50
6	−1.70	14.50	21	13.60	−4.40
7	−11.05	11.55	22	13.60	−1.45
8	−11.05	14.50	23	23.80	−1.80
9	−26.50	14.50	24	26.50	−2.05
10	−26.50	11.55	25	23.80	0.70
11	−26.50	6.05	26	26.50	0.95
12	−26.50	3.05	27	24.00	5.30
13	−26.50	−11.55	28	26.50	5.30
14	−26.50	−14.50	29	24.00	8.30
15	−7.80	−11.55	30	26.50	8.30

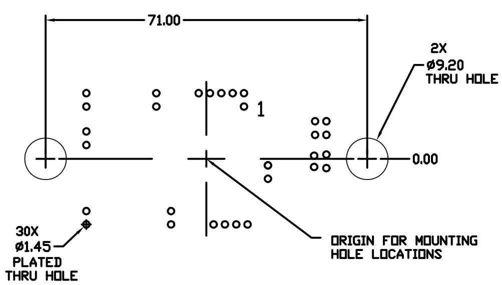




DIM	MILLIMETERS MIN.	NOM.
A	11.10	12.10
A3	15.50	16.50
A4	12.88 BSC	
A5	0.00	0.45
b	1.61	1.71
b1	0.75	0.85
D	70.50	71.50
D1	82.00	83.00
D2	81.50	82.50
E	36.90	37.90
E2	30.30	31.30
P	4.30	4.50
P1	9.30	9.70
P2	1.90	2.10

NOTE 4

PIN	PIN POSITION X	Y	PIN	PIN POSITION X	Y
1	8.30	−11.55	16	−7.800	14.50
2	8.30	−14.50	17	1.60	14.50
3	5.80	−14.50	18	4.10	14.50
4	3.30	−14.50	19	6.60	14.50
5	0.80	−14.50	20	9.10	14.50
6	−1.70	−14.50	21	13.60	4.40
7	−11.05	−11.55	22	13.60	1.45
8	−11.05	−14.50	23	23.80	1.80
9	−26.50	−14.50	24	26.50	2.05
10	−26.50	−11.55	25	23.80	−0.70
11	−26.50	−6.05	26	26.50	−0.95
12	−26.50	−3.05	27	24.00	−5.30
13	−26.50	11.55	28	26.50	−5.30
14	−26.50	14.50	29	24.00	−8.30
15	−7.80	11.55	30	26.50	−8.30

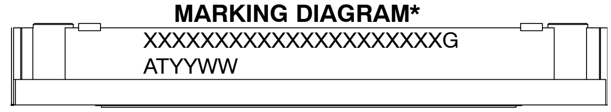


RECOMMENDED
MOUNTING PATTERN
(VIEW FROM MOUNTING SIDE)

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b AND b1 APPLY TO THE PLATED TERMINALS AND ARE MEASURED AT DIMENSION A4.
4. POSITION OF THE CENTER OF THE TERMINALS IS DETERMINED FROM DATUM B THE CENTER OF DIMENSION D, X DIRECTION, AND FROM DATUM A, Y DIRECTION. POSITIONAL TOLERANCE, AS NOTED IN DRAWING, APPLIES TO EACH TERMINAL IN BOTH DIRECTIONS.
5. PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
G = Pb−Free Package
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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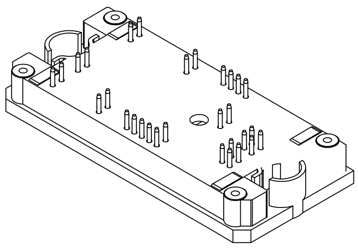
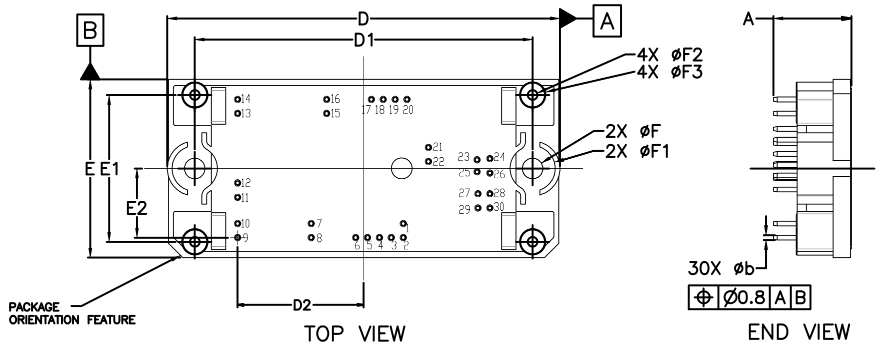
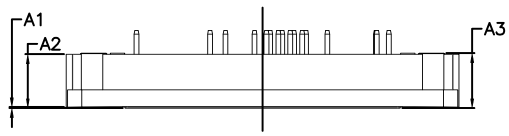


PIM30, 71x37.4
CASE 180AQ
ISSUE A

DATE 25 JUN 2018



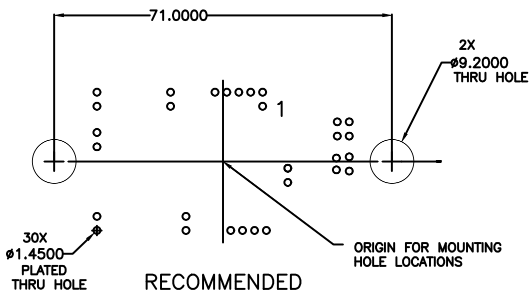
MOUNTING HOLE POSITION			MOUNTING HOLE POSITION		
PIN	X	Y	PIN	X	Y
1	8.30	11.55	16	−7.800	−14.50
2	8.30	14.50	17	1.60	−14.50
3	5.80	14.50	18	4.10	−14.50
4	3.30	14.50	19	6.60	−14.50
5	0.80	14.50	20	9.10	−14.50
6	−1.70	14.50	21	13.60	−4.40
7	−11.05	11.55	22	13.60	−1.45
8	−11.05	14.50	23	23.80	−1.80
9	−26.50	14.50	24	26.50	−2.05
10	−26.50	11.55	25	23.80	0.70
11	−26.50	6.05	26	26.50	0.95
12	−26.50	3.05	27	24.00	5.30
13	−26.50	−11.55	28	26.50	5.30
14	−26.50	−14.50	29	24.00	8.30
15	−7.80	−11.55	30	26.50	8.30



SIDE VIEW

NOTE 4

PIN	PIN POSITION X	PIN POSITION Y	PIN	PIN POSITION X	PIN POSITION Y
1	8.30	−11.55	16	−7.800	14.50
2	8.30	−14.50	17	1.60	14.50
3	5.80	−14.50	18	4.10	14.50
4	3.30	−14.50	19	6.60	14.50
5	0.80	−14.50	20	9.10	14.50
6	−1.70	−14.50	21	13.60	4.40
7	−11.05	−11.55	22	13.60	1.45
8	−11.05	−14.50	23	23.80	1.80
9	−26.50	−14.50	24	26.50	2.05
10	−26.50	−11.55	25	23.80	−0.70
11	−26.50	−6.05	26	26.50	−0.95
12	−26.50	−3.05	27	24.00	−5.30
13	−26.50	11.55	28	26.50	−5.30
14	−26.50	14.50	29	24.00	−8.30
15	−7.80	11.55	30	26.50	−8.30



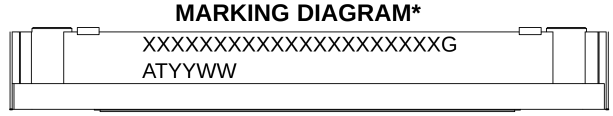
RECOMMENDED MOUNTING PATTERN

DIM	MILLIMETERS MIN.	MILLIMETERS NOM.	MILLIMETERS MAX.
A	15.90	16.40	16.90
A1	---	0.30	0.60
A2	10.90	11.40	11.90
A3	11.10	11.60	12.10
b	0.90	1.00	1.10
D	82.00	82.50	83.00
D1	70.50	71.00	71.50
D2		26.50 REF	
E	36.90	37.40	37.90
E1	30.30	30.80	31.30
E2		14.50 REF	
F	4.30	4.30	4.50
F1		9.5 REF	
F2		2.0 REF	
F3		5.5 REF	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b AND b1 APPLY TO THE PLATED TERMINALS AND ARE MEASURED AT DIMENSION A4.
4. POSITION OF THE CENTER OF THE TERMINALS IS DETERMINED FROM DATUM B THE CENTER OF DIMENSION D, X DIRECTION, AND FROM DATUM A, Y DIRECTION. POSITIONAL TOLERANCE, AS NOTED IN DRAWING, APPLIES TO EACH TERMINAL IN BOTH DIRECTIONS.
5. PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
G = Pb−Free Package
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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