Silicon Carbide (SiC) Module – 22 mohm, 1200 V, SiC M3S MOSFET, 6-PACK, F1 Package

Product Preview

NXH022S120M3F1PTG

The NXH022S120M3F1PTG is a power module containing 22 mΩ / 1200 V SiC MOSFET 6−PACK and a thermistor with Al2O3 DBC in an F1 package.

Features

- 22 mΩ / 1200 V M3S SiC MOSFET 6−PACK
- Al2O3 DBC
- Thermistor
- Options with Pre−Applied Thermal Interface Material (TIM) and without Pre−Applied TIM
- Press−Fit Pins
- These Devices are Pb−Free, Halide Free and are RoHS Compliant

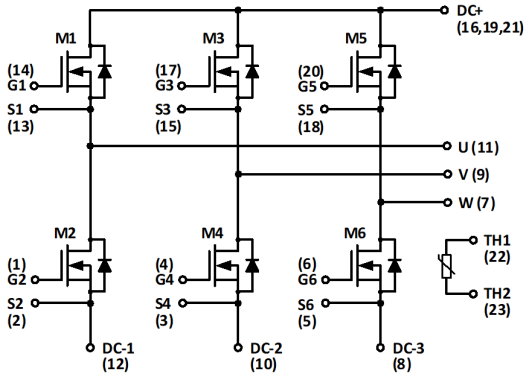
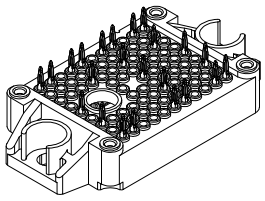


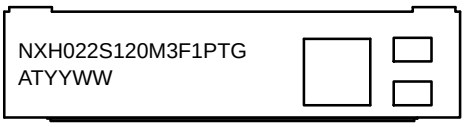
Figure 1. NXH022S120M3F1PTG Schematic Diagram

PACKAGE PICTURE



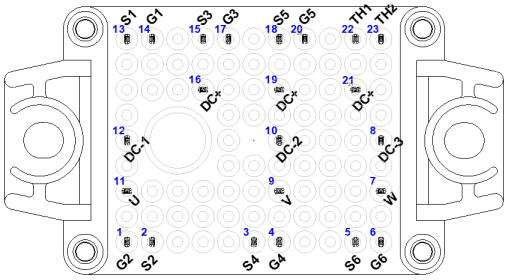
PIM23 33.80x42.50x12.00
CASE 180DA

MARKING DIAGRAM



NXH022S120M3F1PTG = Specific Device Code
AT = Assembly & Test Site Code
YWW = Year and Work Week Code

PIN CONNECTIONS



See Pin Function Description for pin names

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	G2	M2 Gate (Low side switch)
2	S2	M2 Kelvin Source (Low side switch)
3	S4	M4 Kelvin Source (Low side switch)
4	G4	M4 Gate (Low side switch)
5	S6	M6 Kelvin Source (Low side switch)
6	G6	M6 Gate (Low side switch)
7	W	W Terminal
8	DC−3	DC Negative Bus Connection
9	V	V Terminal
10	DC−2	DC Negative Bus Connection
11	U	U Terminal
12	DC−1	DC Negative Bus Connection
13	S1	M1 Kelvin Source (High side switch)
14	G1	M1 Gate (High side switch)
15	S3	M3 Kelvin Source (High side switch)
16	DC+	DC Positive Bus Connection
17	G3	M3 Gate (High side switch)
18	S5	M5 Kelvin Source (High side switch)
19	DC+	DC Positive Bus Connection
20	G5	M5 Gate (High side switch)
21	DC+	DC Positive Bus Connection
22	TH1	Thermistor Connection 1
23	TH2	Thermistor Connection 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
SiC MOSFET			
Drain−Source Voltage	V_{DSS}	1200	V
Gate−Source Voltage	V_{GS}	+22/−10	V
Continuous Drain Current @ T_c = 80°C (T_J = 175°C)	I_D	48	A
Pulsed Drain Current (T_J = 150°C)	I_{Dpulse}	144	A
Maximum Power Dissipation (T_J = 175°C)	P_{tot}	116	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	175	°C
THERMAL PROPERTIES			
Storage Temperature Range	T_{stg}	−40 to 150	°C
INSULATION PROPERTIES			
Isolation Test Voltage, t = 1 s, 60 Hz	V_{is}	4800	V_{RMS}
Creepage Distance		12.7	mm
CTI		600	
Substrate Ceramic Material		Al_2O_3	
Substrate Ceramic Material Thickness		0.32	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 1200 V, T_J = 25°C	I_{DSS}	−	−	100	μA
Drain−Source On Resistance (Note 1)	V_{GS} = 18 V, I_D = 50 A, T_J = 25°C	$R_{DS(ON)}$	−	22.6	30	mΩ
	V_{GS} = 18 V, I_D = 50 A, T_J = 125°C		−	38.6	−	
	V_{GS} = 18 V, I_D = 50 A, T_J = 150°C		−	43.8	−	
	V_{GS} = 18 V, I_D = 50 A, T_J = 175°C		−	50.6	−	
Gate−Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 20 mA	$V_{GS(TH)}$	2.04	2.72	4.4	V
Recommended Gate Voltage		V_{GOP}	−3	−	+18	V
Gate−to−Source Leakage Current	V_{GS} = +22/−10 V, V_{DS} = 0 V	I_{GSS}	−	−	±1	μA
Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 800 V	C_{ISS}	–	3246	–	pF
Reverse Transfer Capacitance		C_{RSS}	–	14	–	
Output Capacitance		C_{OSS}	–	157	–	
Total Gate Charge	V_{GS} = −3/18 V, V_{DS} = 800 V, I_D = 50 A	$Q_{G(TOTAL)}$	–	138	–	nC
Gate−Source Charge		Q_{GS}	–	29	–	nC
Gate−Drain Charge		Q_{GD}	–	33	–	nC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Turn−on Delay Time	T_J = 25°C V_{DS}= 800 V, I_D = 50 A V_{GS} = −3/18 V, R_G = 10 Ω	$t_{d(on)}$	–	25.75	–	ns
Rise Time		t_r	–	10.4	–	
Turn−off Delay Time		$t_{d(off)}$	–	105.98	–	
Fall Time		t_f	–	5.31	–	
Turn−on Switching Loss per Pulse		E_{ON}	–	0.66	–	mJ
Turn−off Switching Loss per Pulse		E_{OFF}	–	0.47	–	
Turn−on Delay Time	T_J = 150°C V_{DS}= 800 V, I_D = 50 A V_{GS} = −3/18 V, R_G = 10 Ω	$t_{d(on)}$	–	25.61	–	ns
Rise Time		t_r	–	8.73	–	
Turn−off Delay Time		$t_{d(off)}$	–	117.56	–	
Fall Time		t_f	–	5.17	–	
Turn−on Switching Loss per Pulse		E_{ON}	–	0.83	–	mJ
Turn−off Switching Loss per Pulse		E_{OFF}	–	0.56	–	
Diode Forward Voltage	I_{SD} = 50 A, V_{GS} = −3 V, T_J = 25°C,	V_{SD}	–	5.21	6.2	V
	I_{SD} = 50 A, V_{GS} = −3 V, T_J = 125°C		–	5.11	–	
	I_{SD} = 50 A, V_{GS} = −3 V, T_J = 150°C		–	5.02	–	
Thermal Resistance − Chip−to−Case	M1, M2, M3, M4, M5, M6	R_{thJC}	–	0.816	–	°C/W
Thermal Resistance − Chip−to−Heatsink	Thermal grease, Thickness = 2 Mil ±2%, A = 2.8 W/mK	R_{thJH}	–	1.263	–	°C/W
THERMISTOR CHARACTERISTICS						
Nominal Resistance	T = 25°C	R_{25}	–	5	–	kΩ
	T = 100°C	R_{100}	–	457	–	Ω
	T = 150°C	R_{150}	–	159.5	–	Ω
Deviation of R_{100}	T = 100°C	ΔR/R	−5	–	5	%
Power Dissipation − Recommended Limit	0.15 mA, Non−self−heating Effect	P_D	–	0.1	–	mW
Power Dissipation − Absolute Maximum	5 mA	P_D	–	34.2	–	mW
Power Dissipation Constant			–	1.4	–	mW/K
B−value	B(25/50), tolerance ±2%		–	3375	–	K
B−value	B(25/100), tolerance ±2%		–	3436	–	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH022S120M3F1PTG	NXH022S120M3F1PTG	F1: Case 180DA Press−fit Pins with pre−applied thermal interface material (TIM) (Pb−Free / Halide Free)	28 Units / Blister Tray

TYPICAL CHARACTERISTIC

(M1~M6 SiC MOSFET CHARACTERISTIC)

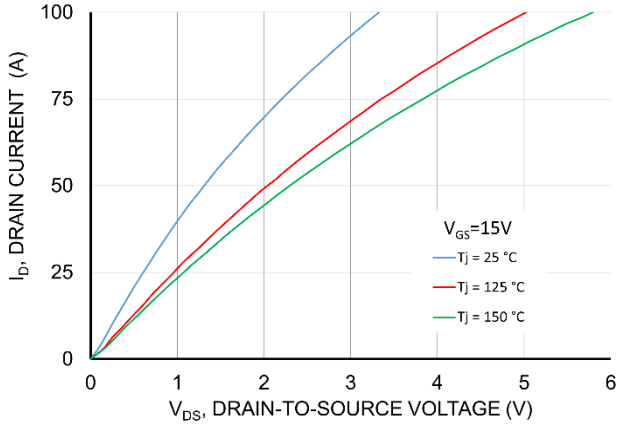


Figure 2. MOSFET Typical Output Characteristic V_{GS} = 15 V

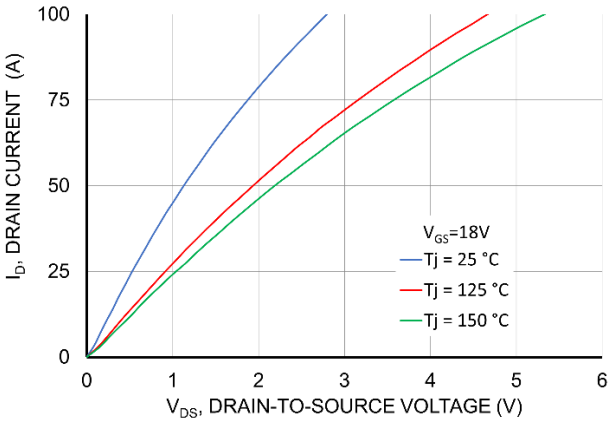


Figure 3. MOSFET Typical Output Characteristic V_{GS} = 15 V

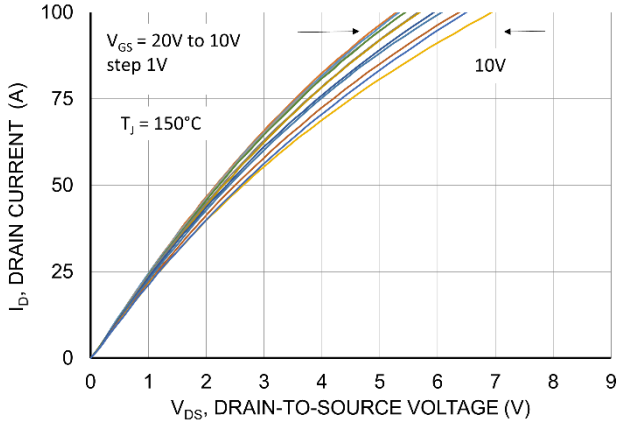


Figure 4. MOSFET Typical Transfer Characteristic V_{GS} = var.

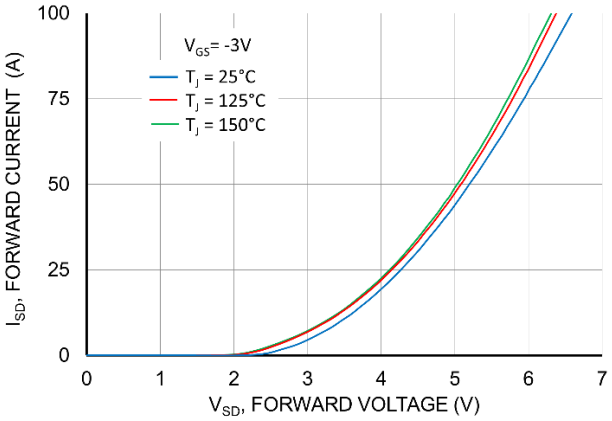


Figure 5. Body Diode Forward Characteristic

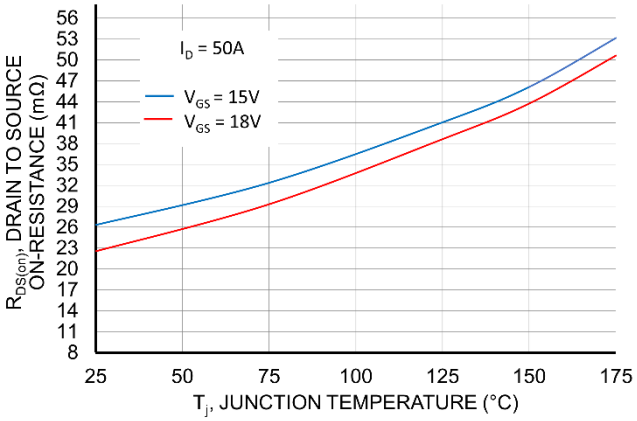


Figure 6. $R_{DS(ON)}$ Drain to Source On Resistance vs. Junction Temperature

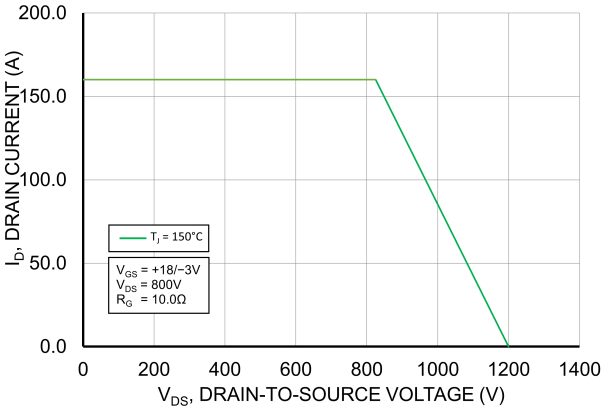


Figure 7. Reverse Bias Safe Operating Area (RBSOA)

TYPICAL CHARACTERISTIC

(M1~M6 SiC MOSFET CHARACTERISTIC) (CONTINUED)

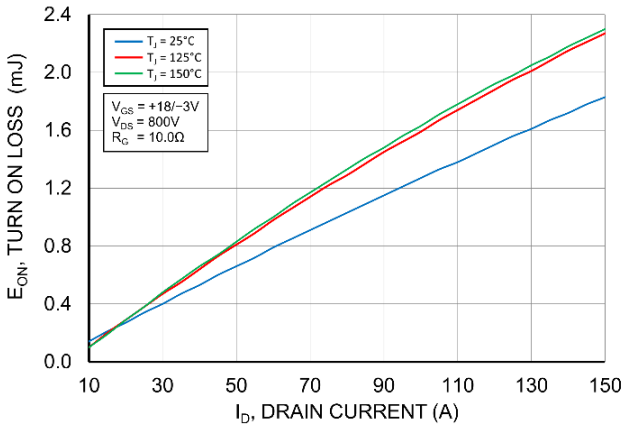


Figure 8. Switching On Loss vs. Drain Current V_{DS} = 800 V

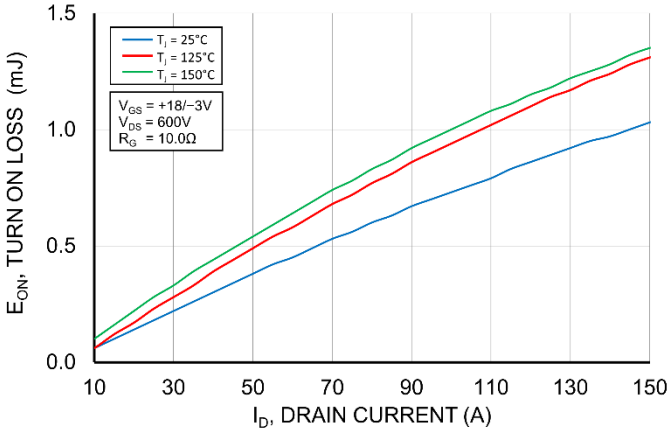


Figure 9. Switching On Loss vs. Drain Current V_{DS} = 600 V

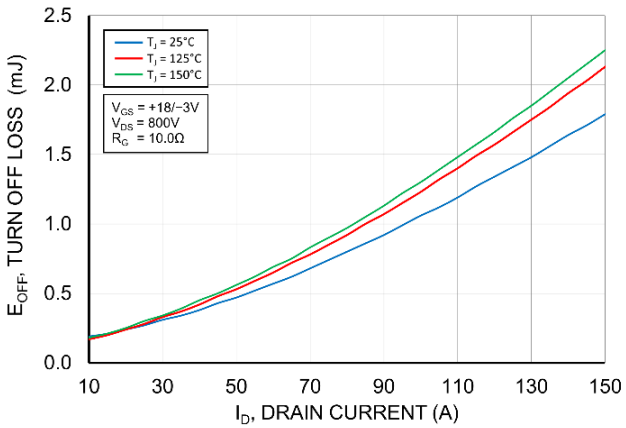


Figure 10. Switching Off Loss vs. Drain Current V_{DS} = 800 V

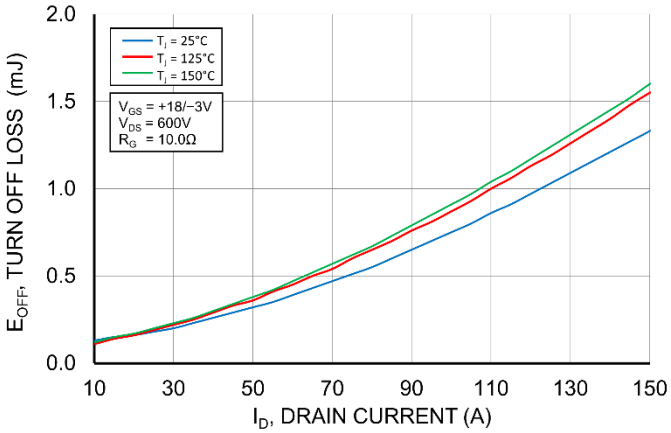


Figure 11. Switching Off Loss vs. Drain Current V_{DS} = 600 V

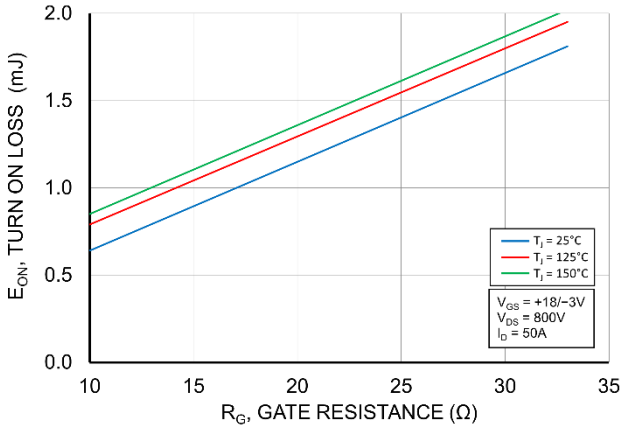


Figure 12. Switching On Loss vs. Gate Resistance V_{DS} = 800 V

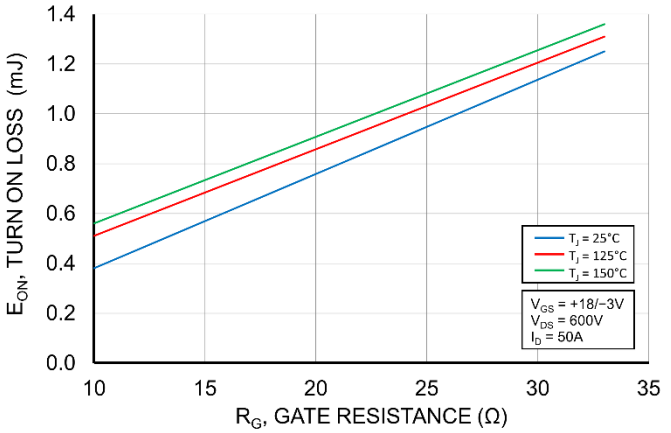


Figure 13. Switching On Loss vs. Gate Resistance V_{DS} = 600 V

TYPICAL CHARACTERISTIC

(M1/M2 SiC MOSFET CHARACTERISTIC) (CONTINUED)

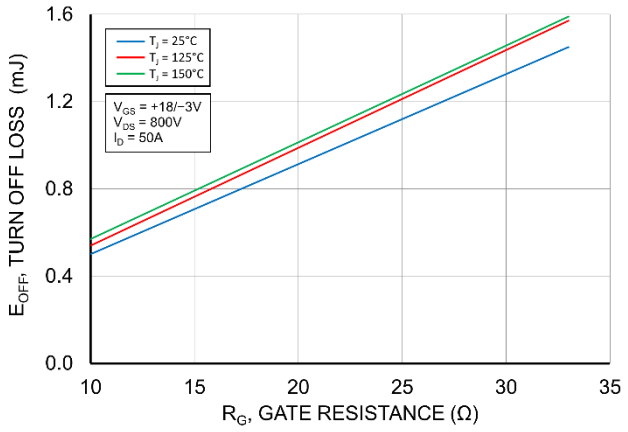


Figure 14. Switching Off Loss vs. Gate Resistance V_{DS} = 800 V

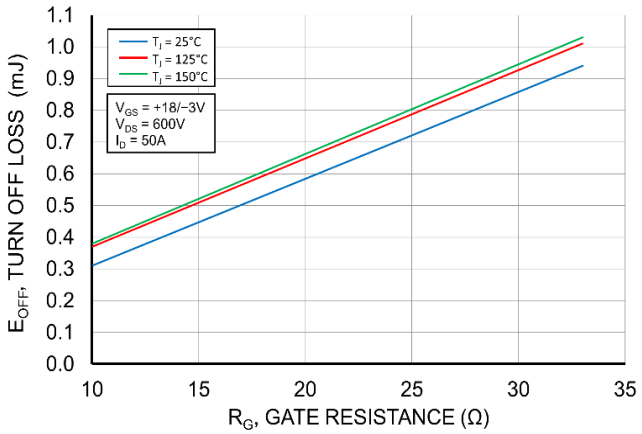


Figure 15. Switching Off Loss vs. Gate Resistance V_{DS} = 600 V

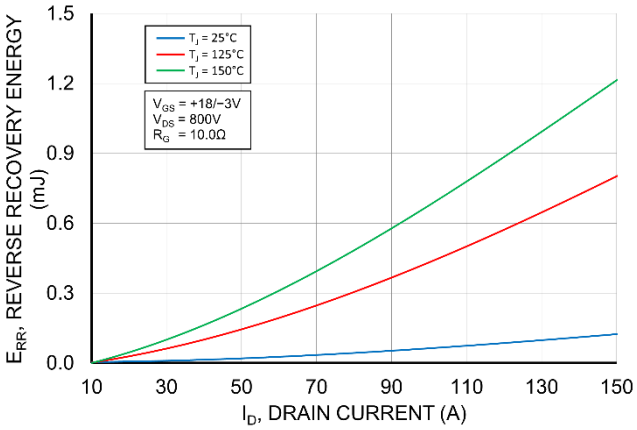


Figure 16. Reverse Recovery Loss vs. Gate Resistance

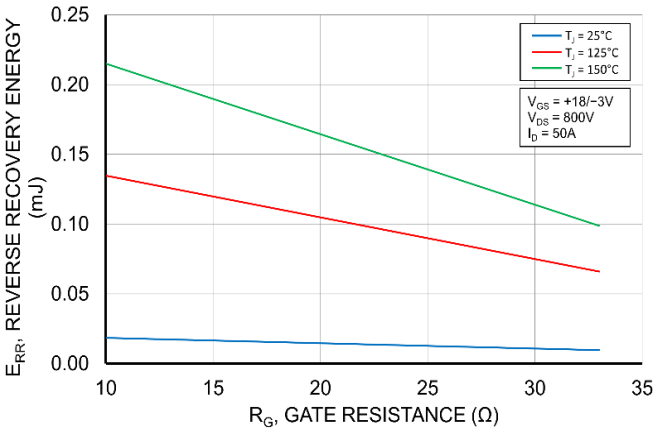


Figure 17. Reverse Recovery Loss vs. Gate Resistance

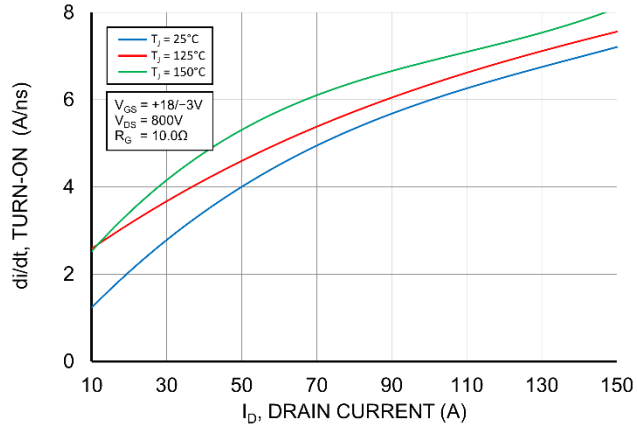


Figure 18. di/dt Turn On vs. Drain Current

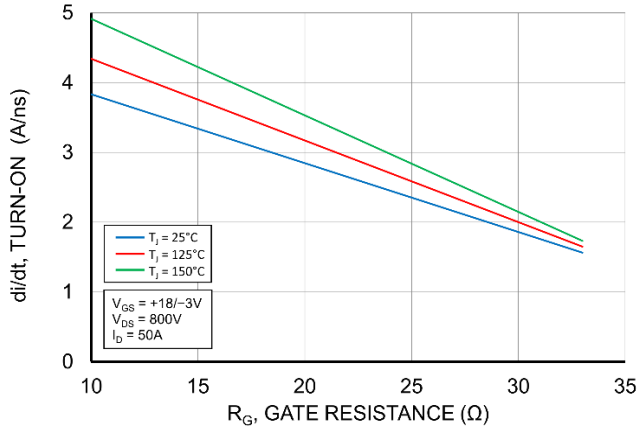


Figure 19. di/dt Turn On vs. Gate Resistance

TYPICAL CHARACTERISTIC

(M1/M2 SiC MOSFET CHARACTERISTIC) (CONTINUED)

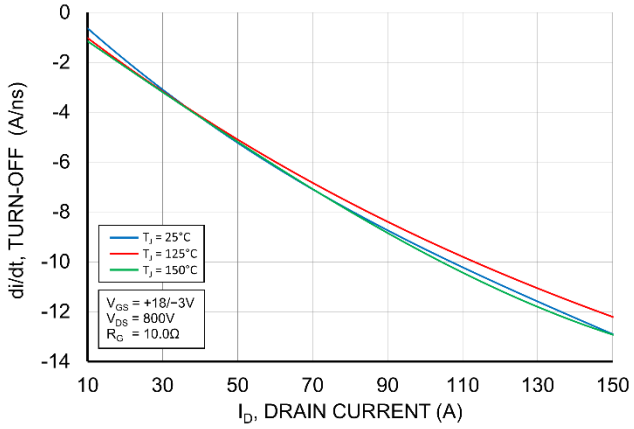


Figure 20. di/dt Turn Off vs. Drain Current

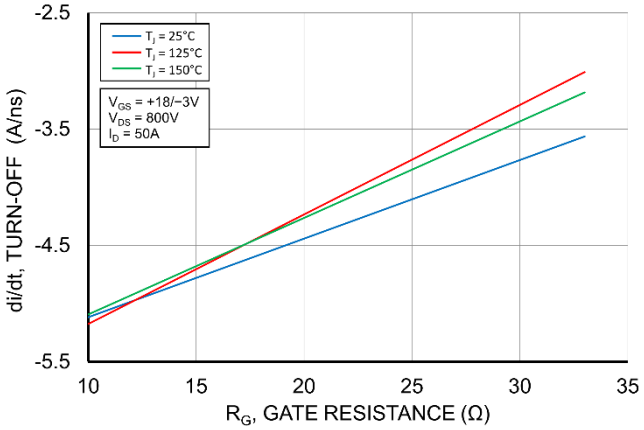


Figure 21. di/dt Turn Off vs. Gate Resistance

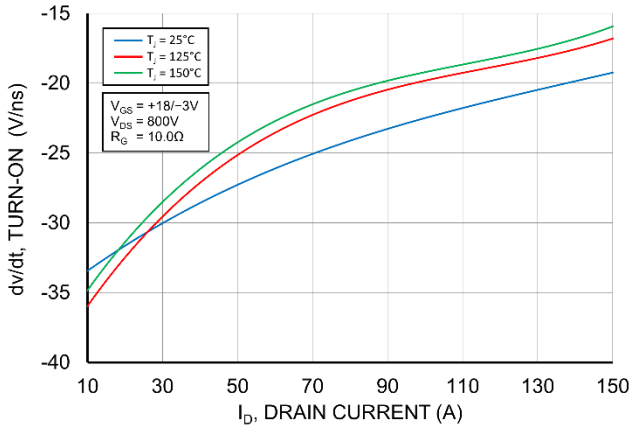


Figure 22. dv/dt Turn On vs. Drain Current

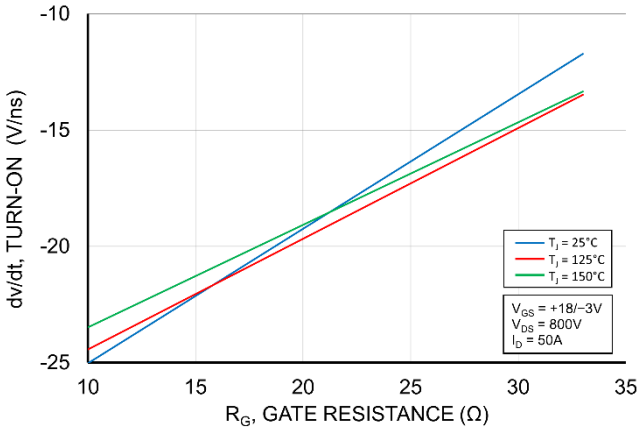


Figure 23. dv/dt Turn On vs. Gate Resistance

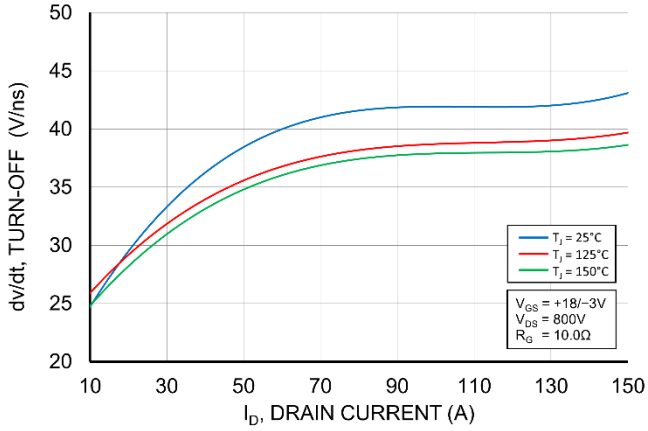


Figure 24. dv/dt Turn Off vs. Drain Current

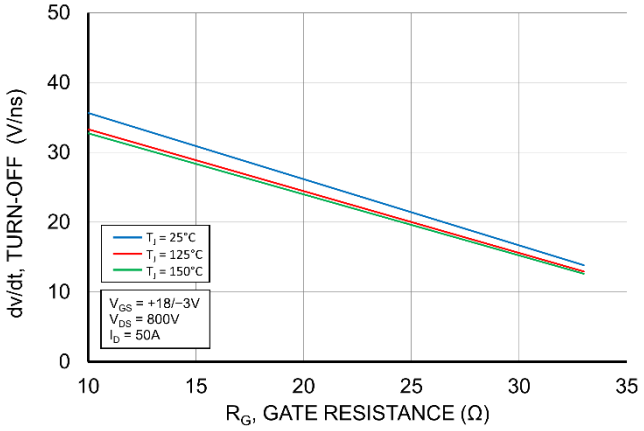


Figure 25. dv/dt Turn Off vs. Gate Resistance

TYPICAL CHARACTERISTIC

(M1/M2 SiC MOSFET CHARACTERISTIC) (CONTINUED)

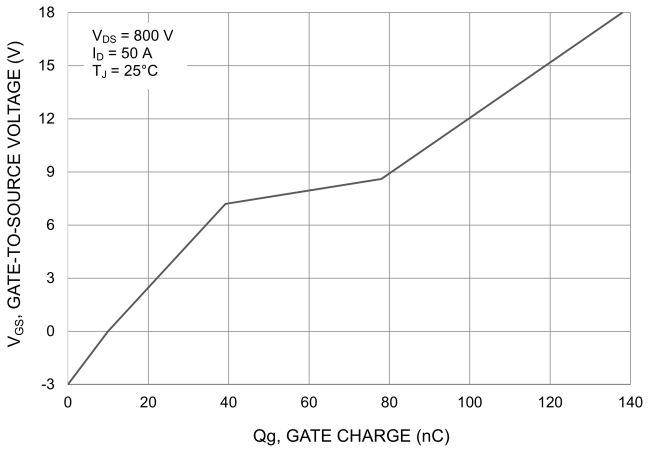


Figure 26. Gate−to− Source Voltage vs. Total Charge

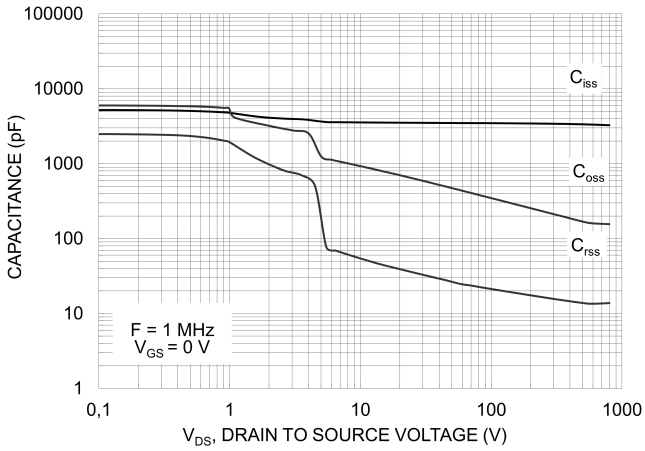


Figure 27. Capacitance vs. Drain−to−Source Voltage

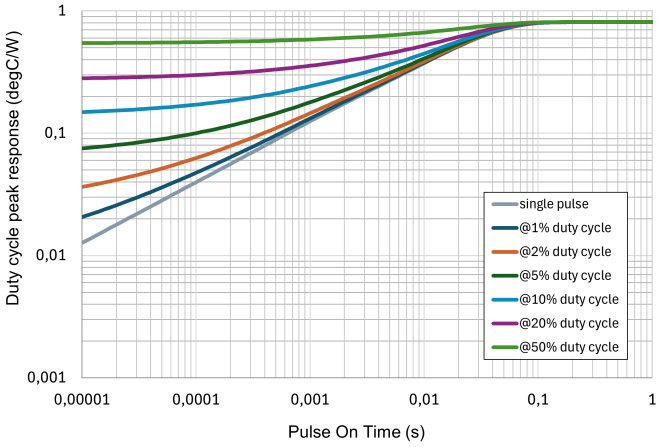
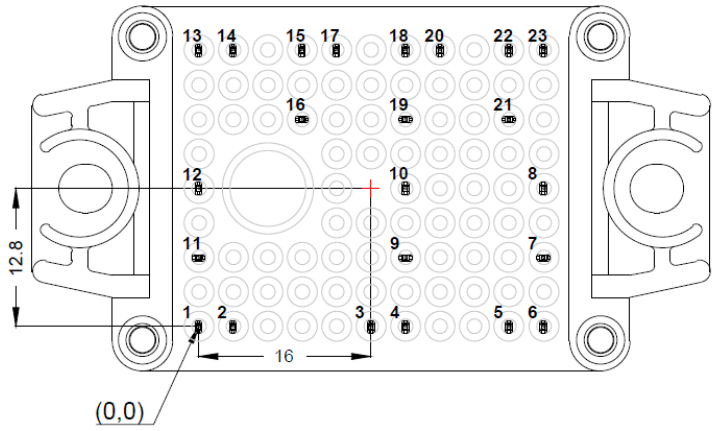


Figure 28. Duty Cycle Response vs. Pulse On Time

Table 1. CAUER NETWORKS

Cauer Element #	Rth (K/W)	Cth (Ws/K)
1	0.0004	0.0006
2	0.0112	0.0003
3	0.0064	0.0006
4	0.105	0.0013
5	0.1388	0.0071
6	0.2554	0.0215
7	0.1847	0.0576



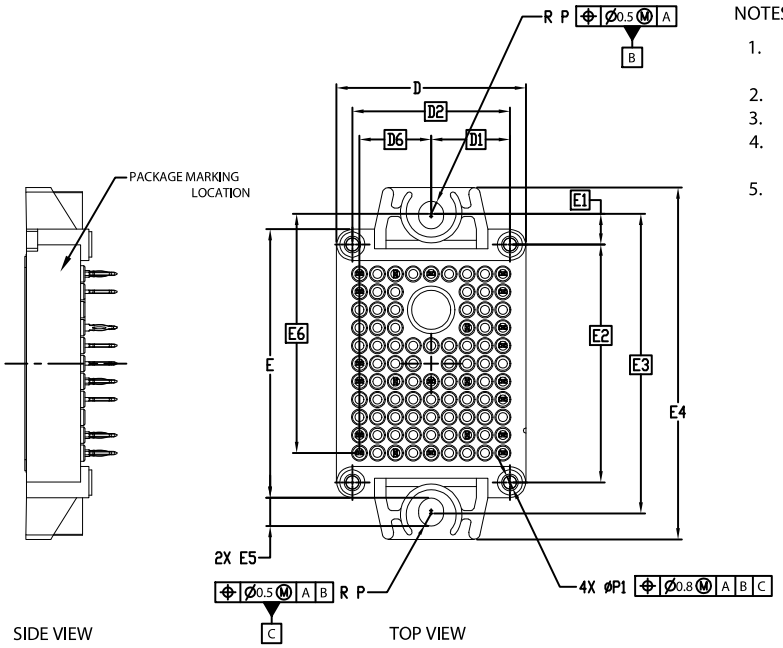
* Pin position

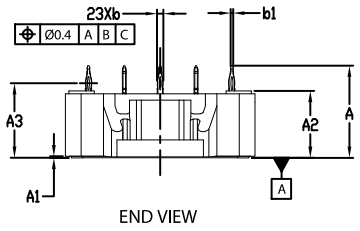
Pin #	X	Y	Function	Pin #	X	Y	Function
1	0	0	G2	13	0	25.6	S1
2	3.2	0	S2	14	3.2	25.6	G1
3	16	0	S4	15	9.6	25.6	S3
4	19.2	0	G4	16	9.6	19.2	DC+
5	28.8	0	S6	17	12.8	25.6	G3
6	32	0	G6	18	19.2	25.6	S5
7	32	6.4	W	19	19.2	19.2	DC+
8	32	12.8	DC-3	20	22.4	25.6	G5
9	19.2	6.4	V	21	28.8	19.2	DC+
10	19.2	12.8	DC-2	22	28.8	25.6	TH1
11	0	6.4	U	23	32	25.6	TH2
12	0	12.8	DC-1				

Figure 29.

PACKAGE DIMENSIONS

PIM23 33.80x42.50x12.00
CASE 180DA
ISSUE O





NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5 - 2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. PIN-GRID IS 3.2mm.
4. PACKAGE MARKING ARE LOCATED ON BOTH SIDES OF THE PACKAGE.
5. THE PINS ARE TIN PLATED.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	16.00	16.50	17.00
A1	0.00	0.35	0.60
A2	11.65	12.00	12.35
b	0.95	1.20	1.25
D	33.50	33.80	34.10
D1	14.05 BSC		
D2	28.10 BSC		
D6	12.80 BSC		
E	47.70	48.00	48.30
E1	5.50 BSC		
E2	42.50 BSC		
E3	53.00 BSC		
E4	62.30	62.80	63.30
E5	4.90	5.00	5.10
E6	42.75BSC		
P	2.20	2.25	2.30
P1	2.20	2.30	2.40

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