

# Silicon Carbide (SiC) Module - EliteSiC, 6 mΩ, 1200 V, SiC M3 MOSFET, 2-PACK Half Bridge Topology, F1 Package

## NXH006P120M3F1PG

The NXH006P120M3F1PG is a power module containing 6 mΩ / 1200 V SiC MOSFET half-bridge and a thermistor with Al<sub>2</sub>O<sub>3</sub> DBC in an F1 package.

### Features

- 6 mΩ / 1200 V M3S SiC MOSFET Half-Bridge
- Al<sub>2</sub>O<sub>3</sub> DBC
- Thermistor
- Press-Fit Pins
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

### Typical Applications

- Solar Inverter
- Uninterruptible Power Supplies
- Electric Vehicle Charging Stations
- Industrial Power

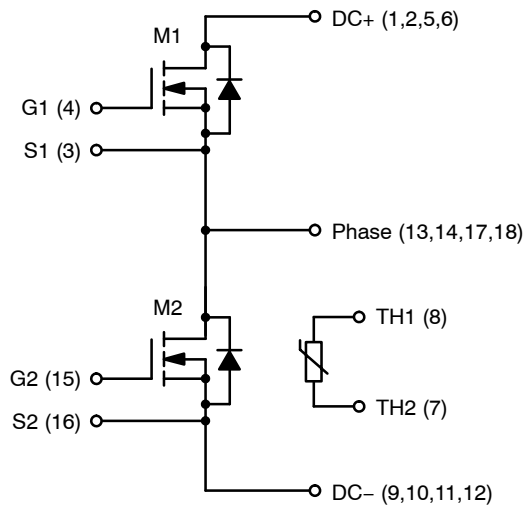
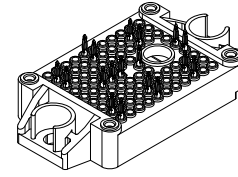
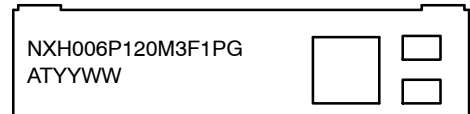


Figure 1. Schematic Diagram



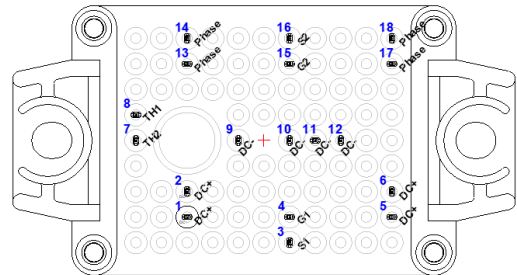
PIM18 33.8x42.5 (PRESS FIT)  
CASE 180BW

### MARKING DIAGRAM



NXH006P120M3F1PG = Specific Device Code  
AT = Assembly & Test Site Code  
YYWW = Year and Work Week Code

### PIN CONNECTIONS



See Pin Function Description for pin names

### ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

# NXH006P120M3F1PG

## PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	DC+	DC Positive Bus connection
2	DC+	DC Positive Bus connection
3	S1	M1 Kelvin Emitter (High side switch)
4	G1	M1 Gate (High side switch)
5	DC+	DC Positive Bus connection
6	DC+	DC Positive Bus connection
7	TH2	Thermistor Connection 2
8	TH1	Thermistor Connection 1
9	DC-	DC Negative Bus connection
10	DC-	DC Negative Bus connection
11	DC-	DC Negative Bus connection
12	DC-	DC Negative Bus connection
13	PHASE	Center point of half bridge
14	PHASE	Center point of half bridge
15	G2	M2 Gate (Low side switch)
16	S2	M2 Kelvin Emitter (Low side switch)
17	PHASE	Center point of half bridge
18	PHASE	Center point of half bridge

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## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
<b>SiC MOSFET</b>			
Drain-to-Source Voltage	$V_{DSS}$	1200	V
Gate-to-Source Voltage	$V_{GS}$	+22/-10	V
Continuous Drain Current @ $T_C = 80\text{ }^\circ\text{C}$ (Note 2)	$I_D$	200	A
Pulsed Drain Current ( $T_J = 175\text{ }^\circ\text{C}$ , $t_p = 100\text{ }\mu\text{s}$ )	$I_{DM}$	600	A
Maximum Power Dissipation @ $T_C = 80\text{ }^\circ\text{C}$ (Note 2)	$P_{tot}$	333	W
Minimum Operating Junction Temperature	$T_{JMIN}$	-40	$^\circ\text{C}$
Maximum Operating Junction Temperature	$T_{JMAX}$	175	$^\circ\text{C}$

## THERMAL PROPERTIES

Storage Temperature Range	$T_{stg}$	-40 to 150	$^\circ\text{C}$
TIM Layer Thickness	$T_{TIM}$	160 $\pm$ 20	$\mu\text{m}$

## INSULATION PROPERTIES

Isolation Test Voltage, $t = 1\text{ s}$ , 60 Hz	$V_{is}$	4800	$V_{RMS}$
Creepage Distance		12.7	mm
CTI		600	
Substrate Ceramic Material		$\text{Al}_2\text{O}_3$	
Substrate Ceramic Material Thickness		0.32	mm
Substrate Warpage (Note 3)	W	Max 0.18	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters
2. Maximum continuous current and power, without switching losses, to reach  $T_J = 175\text{ }^\circ\text{C}$  defined by design based on MOSFET  $R_{DS(ON)}$  and  $R_{\theta JC}$  and not subject to production test
3. Height difference between horizontal plane and substrate copper bottom

## RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	$T_J$	-40	150	$^\circ\text{C}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>SiC MOSFET CHARACTERISTICS</b>						
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 1200\text{ V}$			300	$\mu\text{A}$
Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 18\text{ V}$ , $I_D = 120\text{ A}$ , $T_J = 25\text{ }^\circ\text{C}$		6.0	9	$\text{m}\Omega$
		$V_{GS} = 18\text{ V}$ , $I_D = 120\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		7.5		
		$V_{GS} = 18\text{ V}$ , $I_D = 120\text{ A}$ , $T_J = 150\text{ }^\circ\text{C}$		8.5		
Gate-to-Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 80\text{ mA}$	1.8	2.8	4.4	V
Gate Leakage Current	$I_{GSS}$	$V_{GS} = -10\text{ V} / 22\text{ V}$ , $V_{DS} = 0\text{ V}$	-400		400	nA
Input Capacitance	$C_{ISS}$	$V_{DS} = 800\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 100\text{ kHz}$		13715		pF
Reverse Transfer Capacitance	$C_{RSS}$			52		
Output Capacitance	$C_{OSS}$			598		

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## ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>SiC MOSFET CHARACTERISTICS</b>						
Total Gate Charge	$Q_{G(TOTAL)}$	$V_{DS} = 800\text{ V}, V_{GS} = -5/20\text{ V}, I_D = 100\text{ A}$		622		nC
Gate-to-Source Charge	$Q_{GS}$			91		nC
Gate-to-Drain Charge	$Q_{GD}$			120		nC
Turn-on Delay Time	$t_{d(on)}$	$T_J = 25\text{ }^\circ\text{C}$ $V_{DS} = 800\text{ V}, I_D = 120\text{ A}$ $V_{GS} = -5\text{ V} / 18\text{ V}, R_G = 1.8\text{ }\Omega$		43		ns
Rise Time	$t_r$			14		
Turn-off Delay Time	$t_{d(off)}$			149		
Fall Time	$t_f$			13		
Turn-on Switching Loss per Pulse	$E_{ON}$			3.04		mJ
Turn-off Switching Loss per Pulse	$E_{OFF}$			0.24		
Turn-on Delay Time	$t_{d(on)}$		$T_J = 150\text{ }^\circ\text{C}$ $V_{DS} = 800\text{ V}, I_D = 120\text{ A}$ $V_{GS} = -5\text{ V} / 18\text{ V}, R_G = 1.8\text{ }\Omega$		40	
Rise Time	$t_r$			13		
Turn-off Delay Time	$t_{d(off)}$			160		
Fall Time	$t_f$			13.5		
Turn-on Switching Loss per Pulse	$E_{ON}$			3.71		mJ
Turn-off Switching Loss per Pulse	$E_{OFF}$			0.3		
Diode Forward Voltage	$V_{SD}$	$I_D = 120\text{ A}, T_J = 25\text{ }^\circ\text{C}$		5.3	7.5	V
		$I_D = 120\text{ A}, T_J = 125\text{ }^\circ\text{C}$		4.91		
		$I_D = 120\text{ A}, T_J = 150\text{ }^\circ\text{C}$		4.82		
Thermal Resistance – Chip-to-Case	$R_{thJC}$	M1, M2 (Note 4)		0.21	0.28	$^\circ\text{C}/\text{W}$
Thermal Resistance – Chip-to-Heatsink	$R_{thJH}$	Thermal grease, Thickness = 2 Mil +2%, A = 2.8 W/mK (Note 5)		0.43		$^\circ\text{C}/\text{W}$

## Thermistor Characteristics

Nominal Resistance	$R_{25}$	$T_{NTC} = 25\text{ }^\circ\text{C}$		5		k $\Omega$
Nominal Resistance	$R_{100}$	$T_{NTC} = 100\text{ }^\circ\text{C}$		493		$\Omega$
Nominal Resistance	$R_{150}$	$T_{NTC} = 150\text{ }^\circ\text{C}$		159.5		$\Omega$
Deviation of $R_{100}$	$\Delta R/R$	$T_{NTC} = 100\text{ }^\circ\text{C}$	-5		5	%
Power Dissipation – Recommended Limit	$P_D$	0.15 mA, non-self-heating effect		0.1		mW
Power Dissipation – Absolute Maximum	$P_D$	5 mA		34.2		mW
Power Dissipation Constant				1.4		mW/K
B-value		B(25/50), tolerance $\pm 2\%$		3375		K
B-value		B(25/100), tolerance $\pm 2\%$		3436		K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

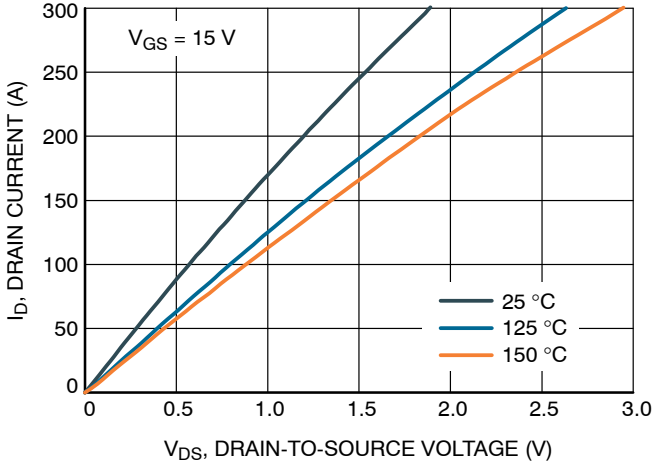
4. Test method compliant with MIL STD 883-1012.1, Cosmetic oxidation and discoloration on the DBC surface allowed
5. Defined by thermal simulation

## ORDERING INFORMATION

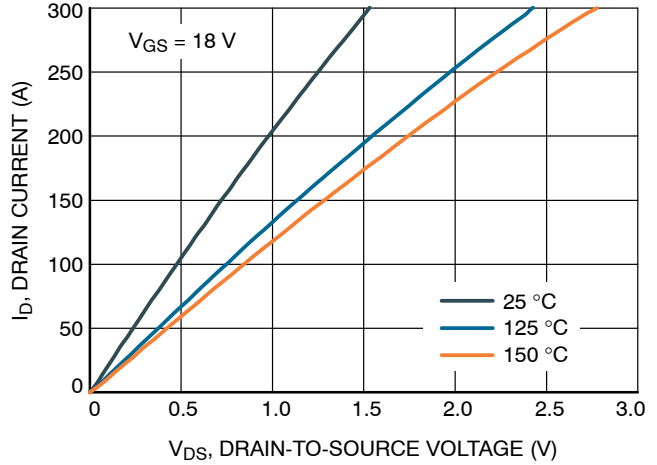
Orderable Part Number	Marking	Package	Shipping
NXH006P120M3F1PG	NXH006P120M3F1PG	F2HALFBR: Case 180BY Press-fit Pins with pre-applied thermal interface material (TIM) (Pb-Free / Halide Free)	20 Units / Blister Tray

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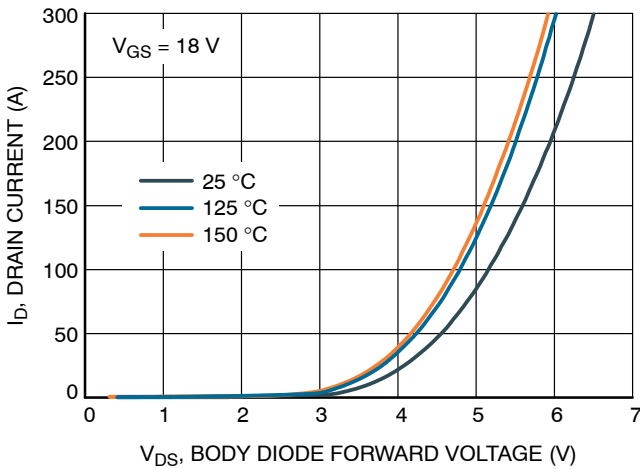
## TYPICAL CHARACTERISTICS



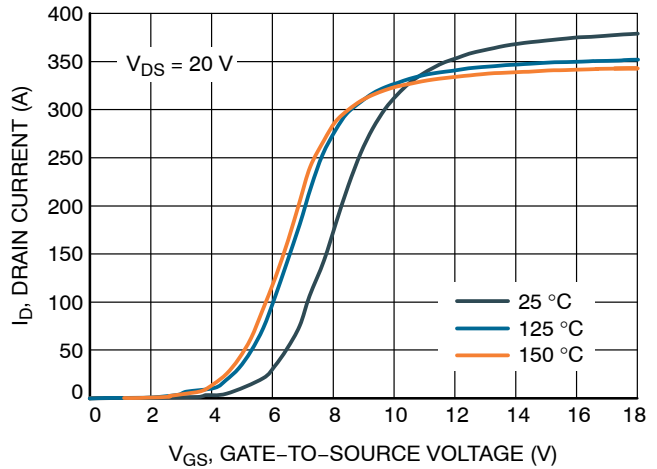
**Figure 2. MOSFET Typical Output Characteristic**



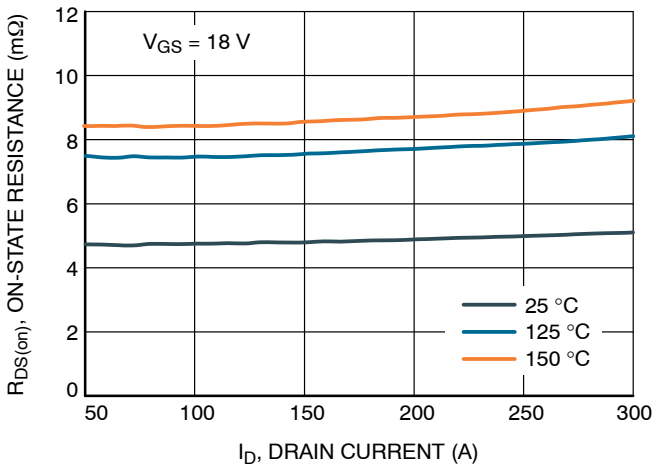
**Figure 3. MOSFET Typical Output Characteristic**



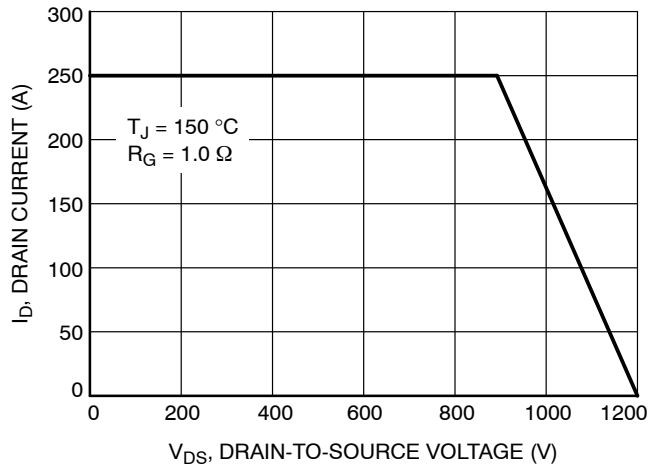
**Figure 4. Body Diode Forward Characteristic**



**Figure 5. Transfer Characteristics**



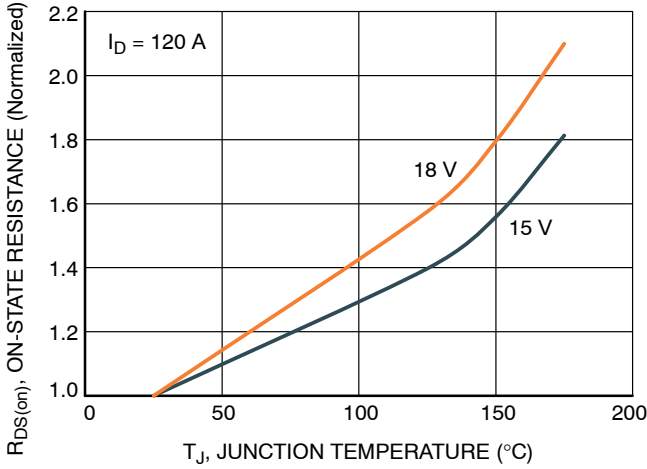
**Figure 6. On-Resistance vs. Drain Current**



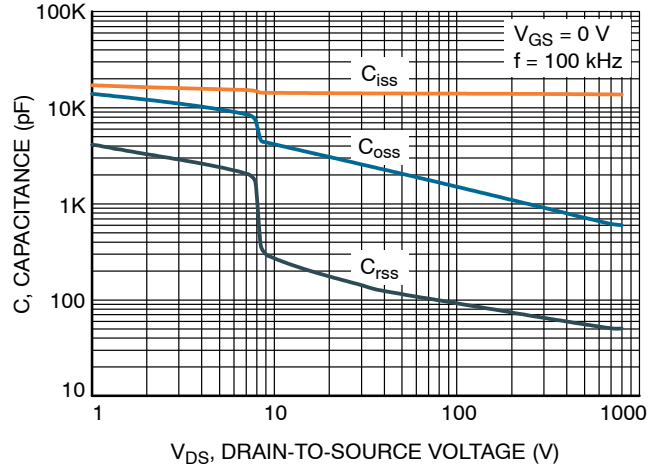
**Figure 7. RBSOA**

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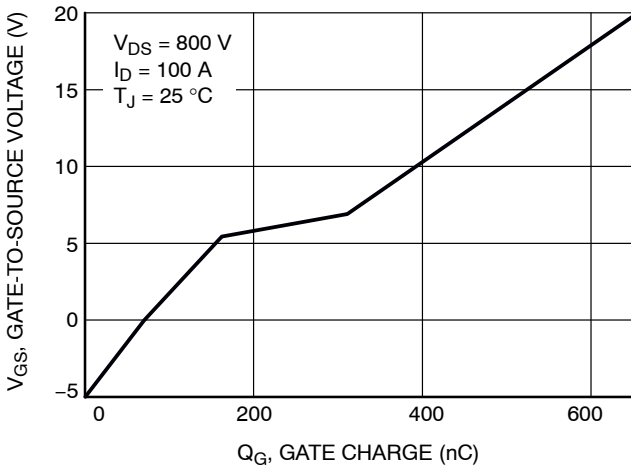
## TYPICAL CHARACTERISTICS



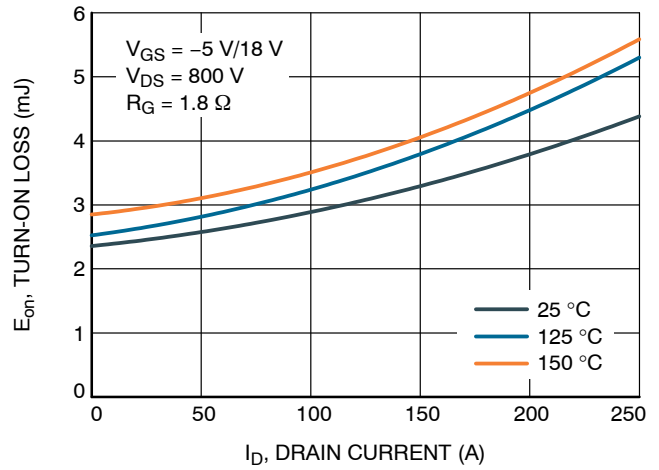
**Figure 8. On-Resistance vs. Junction Temperature (Normalized)**



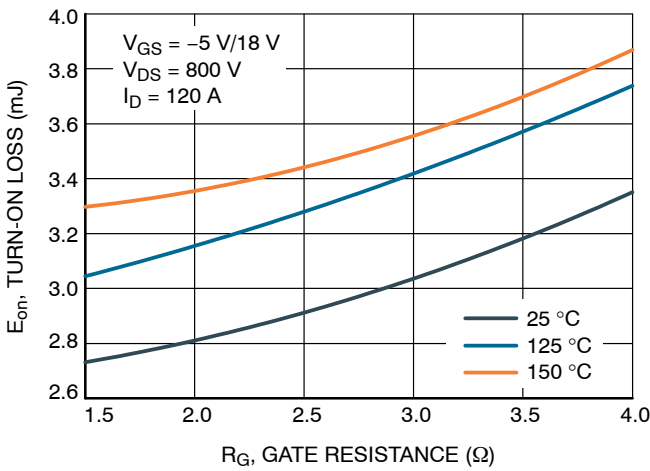
**Figure 9. Capacitance Characteristics**



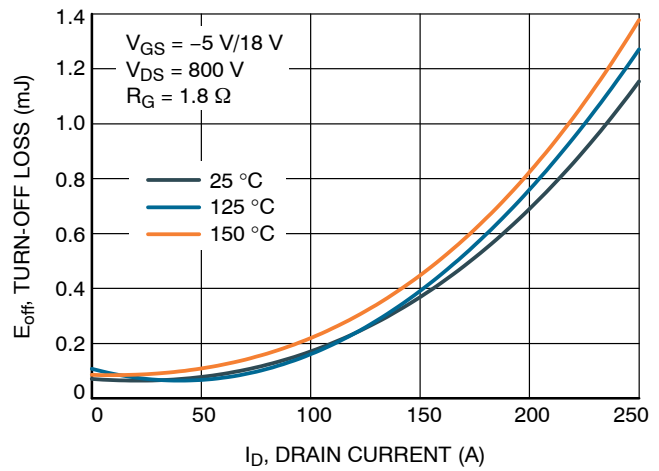
**Figure 10. Gate Charge Characteristics**



**Figure 11. Typical Switching Loss E<sub>on</sub> vs. Drain Current**



**Figure 12. Typical Switching Loss E<sub>on</sub> vs. R<sub>g</sub>**



**Figure 13. Typical Switching Loss E<sub>off</sub> vs. Drain Current**

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## TYPICAL CHARACTERISTICS

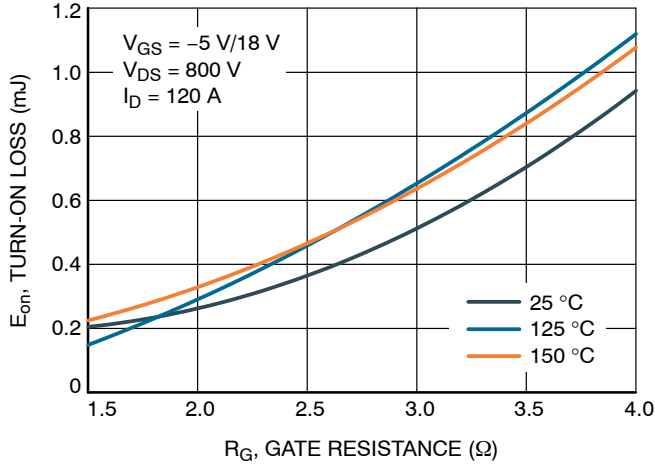


Figure 14. Typical Switching Loss  $E_{on}$  vs.  $R_g$

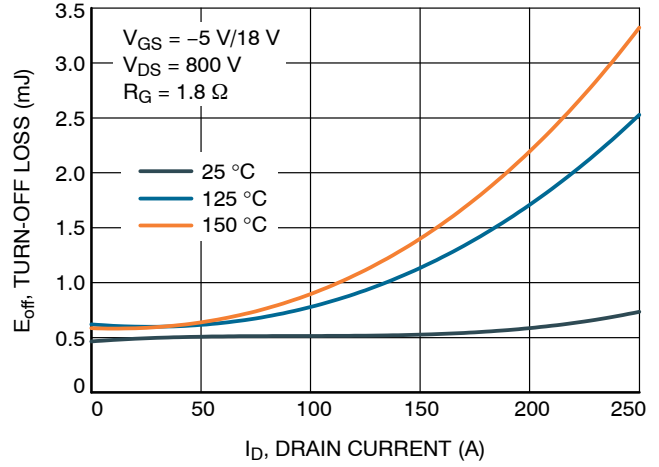


Figure 15. Err vs. Drain Current

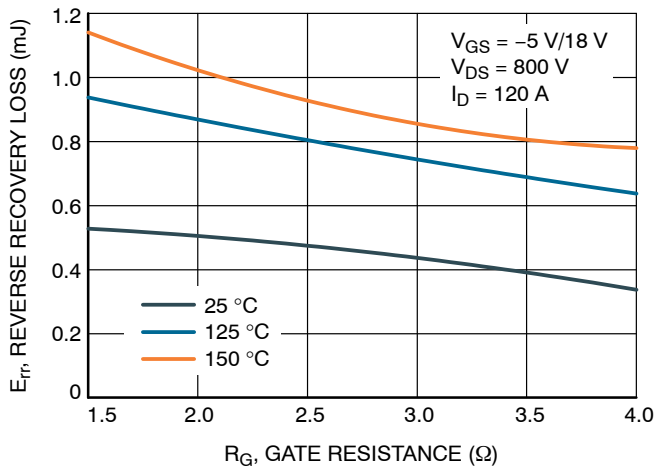


Figure 16. Err vs.  $R_g$

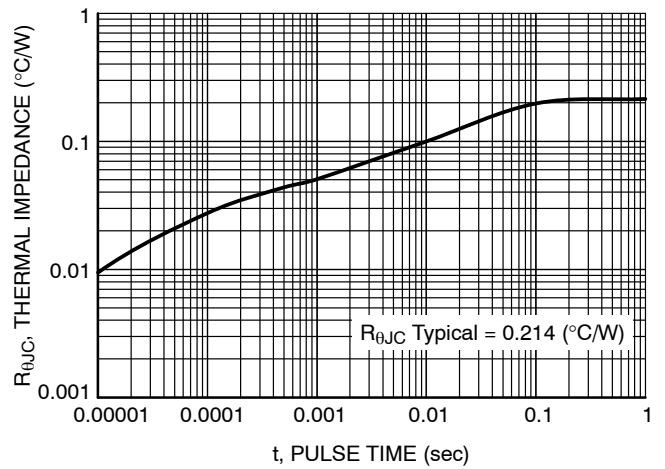


Figure 17. Thermal Response Characteristics

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## REVISION HISTORY

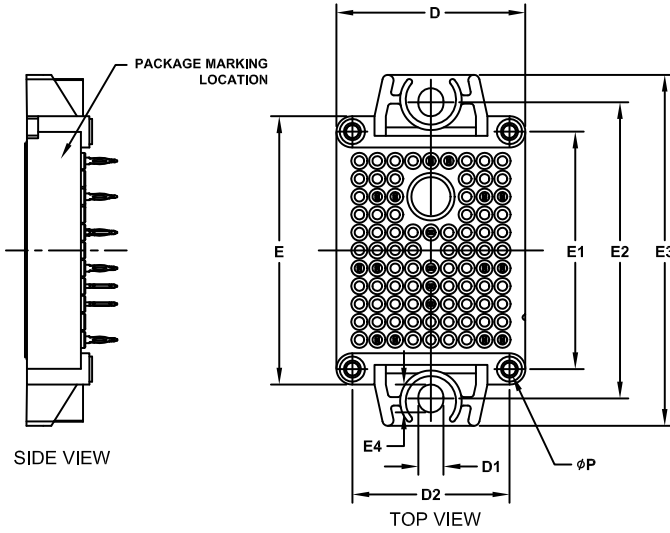
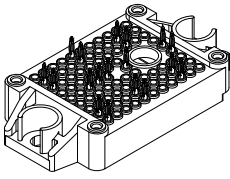
Revision	Description of Changes	Date
0	Initial document release.	5/18/2026

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## PACKAGE DIMENSIONS

PIM18 33.8x42.5 (PRESS FIT)  
CASE 180BW  
ISSUE B

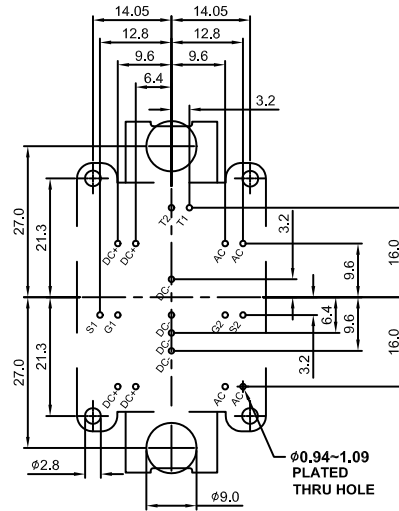
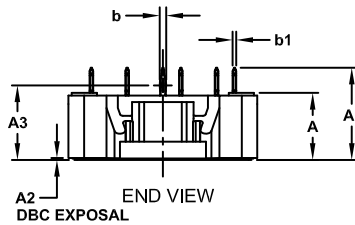
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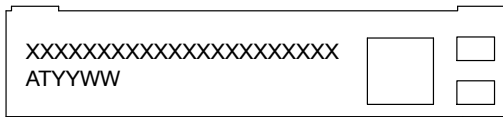
**NOTES:**

1. CONTROLLING DIMENSION: MILLIMETERS
2. PIN POSITION TOLERANCE IS  $\pm 0.4\text{mm}$

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.65	12.00	12.35
A1	16.00	16.50	17.00
A2	0.00	0.35	0.60
A3	12.85	13.35	13.85
b	1.15	1.20	1.25
b1	0.59	0.64	0.69
D	33.50	33.80	34.10
D1	4.40	4.50	4.60
D2	27.95	28.10	28.25
E	47.70	48.00	48.30
E1	42.35	42.50	42.65
E2	52.90	53.00	53.10
E3	62.30	62.80	63.30
E4	4.90	5.00	5.10
P	2.20	2.30	2.40



### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
AT = Assembly & Test Site Code  
YYWW = Year and Work Week Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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