Silicon Carbide (SiC) Module - EliteSiC, 4 mohm SiC M3 MOSFET, 1200 V, 2-PACK Half Bridge Topology, F2 Package with HPS DBC

NXH004P120M3F2PTHG

The NXH004P120M3F2PTHG is a power module containing 4 mΩ / 1200 V SiC MOSFET half-bridge and a thermistor with HPS DBC in an F2 package.

Features

- 4 mΩ / 1200 V M3S SiC MOSFET Half-Bridge
- HPS DBC
- Thermistor
- Pre-Applied Thermal Interface Material (TIM)
- Press-Fit Pins
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

Typical Applications

- Solar Inverter
- Uninterruptible Power Supplies
- Electric Vehicle Charging Stations
- Industrial Power

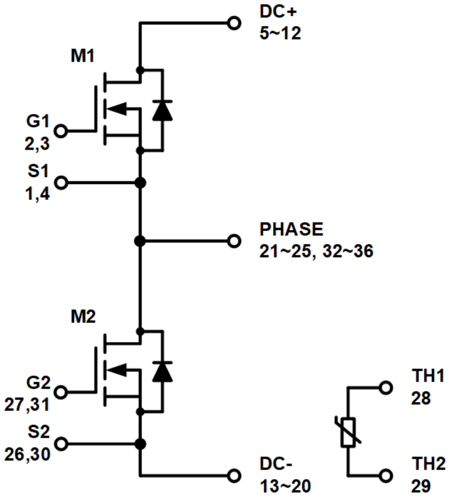
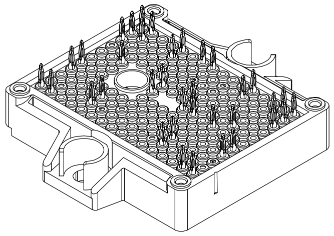


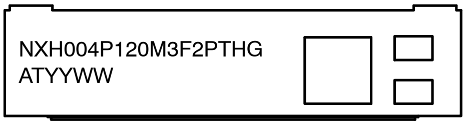
Figure 1. NXH004P120M3F2 Schematic Diagram

PACKAGE PICTURE



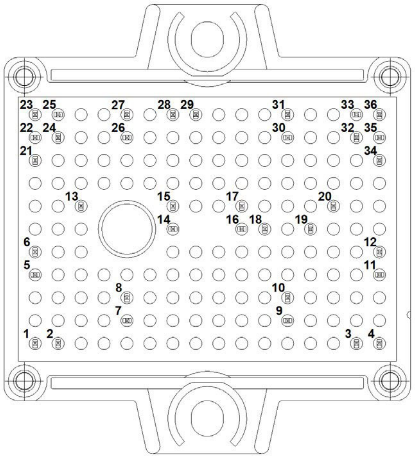
PIM36 56.7x42.5 (PRESS FIT)
CASE 180BY

MARKING DIAGRAM



NXH004P120M3F2PTHG = Specific Device Code
AT = Assembly & Test Site Code
YWW = Year and Work Week Code

PIN CONNECTIONS



See Pin Function Description for pin names

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	S1	Q1 Kelvin Emitter (High side switch)
2	G1	Q1 Gate (High side switch)
3	G1	Q1 Gate (High side switch)
4	S1	Q1 Kelvin Emitter (High side switch)
5	DC+	DC Positive Bus connection
6	DC+	DC Positive Bus connection
7	DC+	DC Positive Bus connection
8	DC+	DC Positive Bus connection
9	DC+	DC Positive Bus connection
10	DC+	DC Positive Bus connection
11	DC+	DC Positive Bus connection
12	DC+	DC Positive Bus connection
13	DC*	DC Negative Bus connection
14	DC−	DC Negative Bus connection
15	DC−	DC Negative Bus connection
16	DC−	DC Negative Bus connection
17	DC−	DC Negative Bus connection
18	DC−	DC Negative Bus connection
19	DC−	DC Negative Bus connection
20	DC−	DC Negative Bus connection
21	PHASE	Center point of half bridge
22	PHASE	Center point of half bridge
23	PHASE	Center point of half bridge
24	PHASE	Center point of half bridge
25	PHASE	Center point of half bridge
26	S2	Q2 Kelvin Emitter (Low side switch)
27	G2	Q2 Gate (Low side switch)
28	TH1	Thermistor Connection 1
29	TH2	Thermistor Connection 2
30	S2	Q2 Kelvin Emitter (Low side switch)
31	G2	Q2 Gate (Low side switch)
32	PHASE	Center point of half bridge
33	PHASE	Center point of half bridge
34	PHASE	Center point of half bridge
35	PHASE	Center point of half bridge
36	PHASE	Center point of half bridge

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
SiC MOSFET			
Drain-Source Voltage	V_{DSS}	1200	V
Gate-Source Voltage	V_{GS}	+22/−10	V
Continuous Drain Current @ T_c = 80 °C (T_J = 175 °C)	I_D	284	A
Pulsed Drain Current (T_J = 175 °C)	I_{Dpulse}	568	A
Maximum Power Dissipation @ T_c = 80 °C (T_J = 175 °C)	P_{tot}	785	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	175	°C
THERMAL PROPERTIES			
Storage Temperature Range	T_{stg}	−40 to 150	°C
TIM Layer Thickness	T_{TIM}	160 ±20	μm
INSULATION PROPERTIES			
Isolation Test Voltage, t = 1 s, 60 Hz	V_{is}	4800	V_{RMS}
Creepage Distance		12.7	mm
CTI		600	
Substrate Ceramic Material		HPS	
Substrate Ceramic Material Thickness		0.38	mm
Substrate Warpage (Note 2)	W	Max 0.18	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. Height difference between horizontal plane and substrate copper bottom.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 1200 V	–	–	300	μA
Drain-Source On Resistance	$R_{DS(ON)}$	V_{GS} = 18 V, I_D = 200 A, T_J = 25 °C	–	4.00	5.5	mΩ
		V_{GS} = 18 V, I_D = 200 A, T_J = 125 °C	–	6.45	–	
		V_{GS} = 18 V, I_D = 200 A, T_J = 150 °C	–	7.50	–	
Gate-Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 120 mA	1.8	2.8	4.4	V
Gate Leakage Current	I_{GSS}	V_{GS} = −10 V / 20 V, V_{DS} = 0 V	−600	–	600	nA
Gate-Resistance	R_G	f = 1 MHz	–	0.25	–	Ω
Input Capacitance	C_{ISS}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz	–	16410	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	72	–	
Output Capacitance	C_{OSS}		–	960	–	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Total Gate Charge	$Q_{G(TOTAL)}$	V_{DS} = 800 V, V_{GS} = −5/20 V, I_D = 200 A	–	876	–	nC
Gate-Source Charge	Q_{GS}		–	174	–	nC
Gate-Drain Charge	Q_{GD}		–	165	–	nC
Turn-on Delay Time	$t_{d(on)}$	T_J = 25 °C V_{DS}= 600 V, I_D = 200 A V_{GS} = −5 V / 18 V, R_G = 1 Ω	–	49	–	ns
Rise Time	t_r		–	15	–	
Turn-off Delay Time	$t_{d(off)}$		–	127	–	
Fall Time	t_f		–	15	–	
Turn-on Switching Loss per Pulse	E_{ON}		–	1.44	–	mJ
Turn-off Switching Loss per Pulse	E_{OFF}		–	1.03	–	
Turn-on Delay Time	$t_{d(on)}$	T_J = 150 °C V_{DS} = 600 V, I_D = 200 A V_{GS} = −5 V / 18 V, R_G = 1 Ω	–	47	–	ns
Rise Time	t_r		–	15	–	
Turn-off Delay Time	$t_{d(off)}$		–	140	–	
Fall Time	t_f		–	14	–	
Turn-on Switching Loss per Pulse	E_{ON}		–	1.77	–	mJ
Turn-off Switching Loss per Pulse	E_{OFF}		–	1.18	–	
Diode Forward Voltage	V_{SD}	I_D = 200 A, T_J = 25 °C	–	5.1	7.5	V
		I_D = 200 A, T_J = 125 °C	–	4.7	–	
		I_D = 200 A, T_J = 150 °C	–	4.6	–	
Thermal Resistance – Chip-to-Case	R_{thJC}	M1, M2	–	0.121	–	°C/W
Thermal Resistance – Chip-to-Heatsink	R_{thJH}	Thermal grease, Thickness = 2 Mil +2%, A = 2.8 W/mK	–	0.263	–	°C/W
THERMISTOR CHARACTERISTICS						
Nominal Resistance	R_{25}	T_{NTC} = 25 °C	–	5	–	kΩ
	R_{100}	T_{NTC} = 100 °C	–	493	–	Ω
	R_{150}	T_{NTC} = 150 °C	–	159.5	–	Ω
Deviation of R_{100}	ΔR/R	T_{NTC} = 100 °C	−5	–	5	%
Power Dissipation – Recommended Limit	P_D	0.15 mA, Non-self-heating Effect	–	0.1	–	mW
Power Dissipation – Absolute Maximum	P_D	5 mA	–	34.2	–	mW
Power Dissipation Constant			–	1.4	–	mW/K
B-value		B (25/50), Tolerance ±2%	–	3375	–	K
B-value		B (25/100), Tolerance ±2%	–	3436	–	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH004P120M3F2PTHG	NXH004P120M3F2PTHG	F2HALFBR: Case 180BY Press-fit Pins with pre-applied thermal interface material (TIM) (Pb-Free / Halide Free)	20 Units / Blister Tray

TYPICAL CHARACTERISTIC

(M1/M2 SiC MOSFET CHARACTERISTIC)

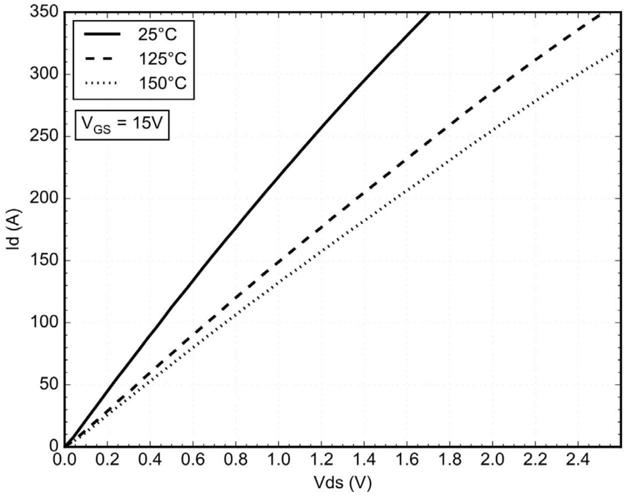


Figure 2. MOSFET Typical Output Characteristic

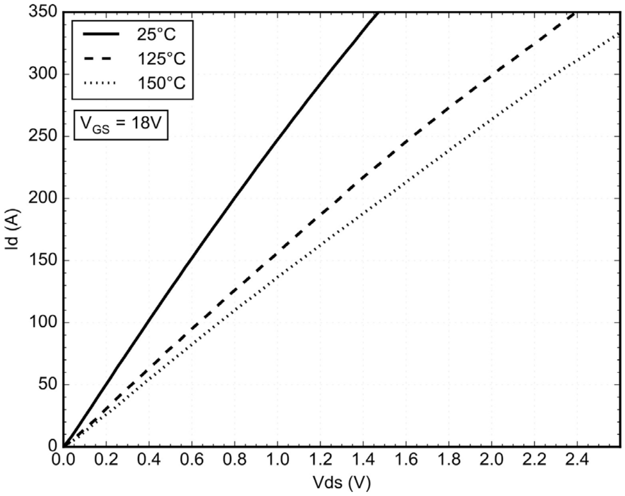


Figure 3. MOSFET Typical Output Characteristic

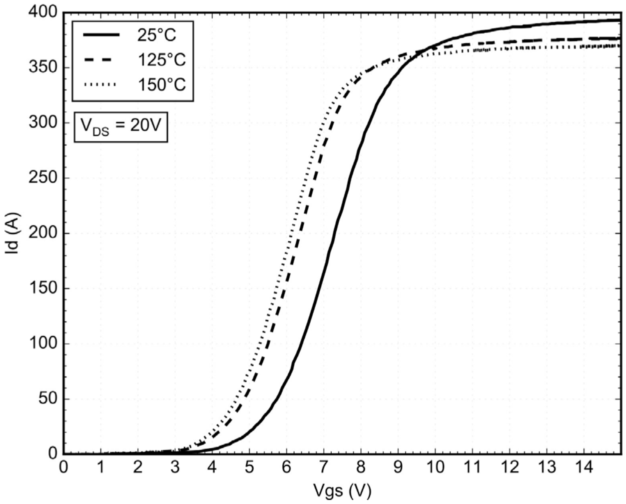


Figure 4. MOSFET Typical Transfer Characteristic

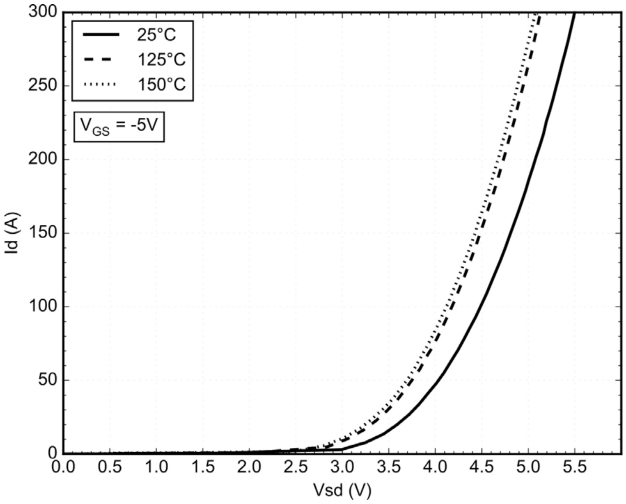


Figure 5. Body Diode Forward Characteristic

TYPICAL CHARACTERISTIC

(M1/M2 SiC MOSFET CHARACTERISTIC)

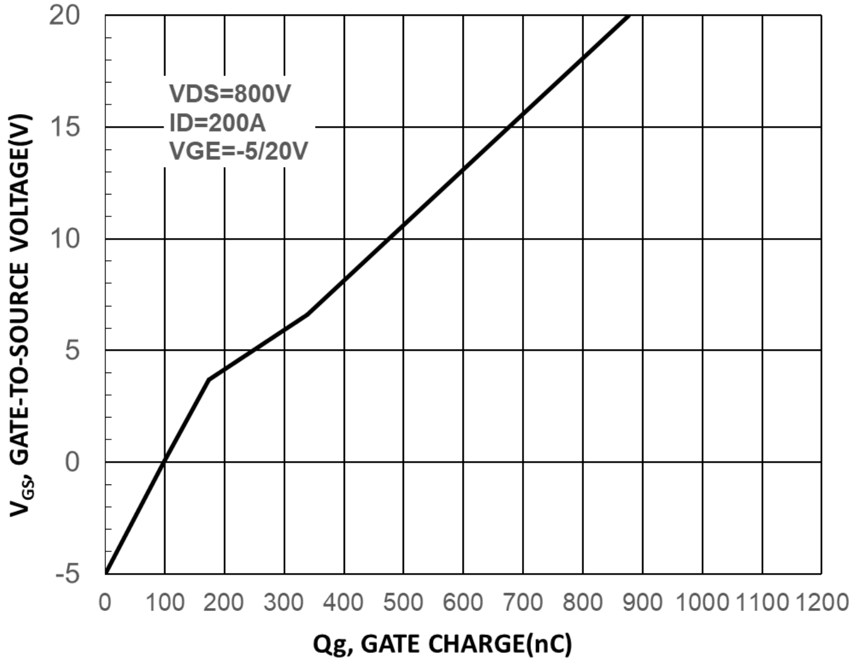


Figure 6. Gate-to-Source Voltage vs. Total Charge

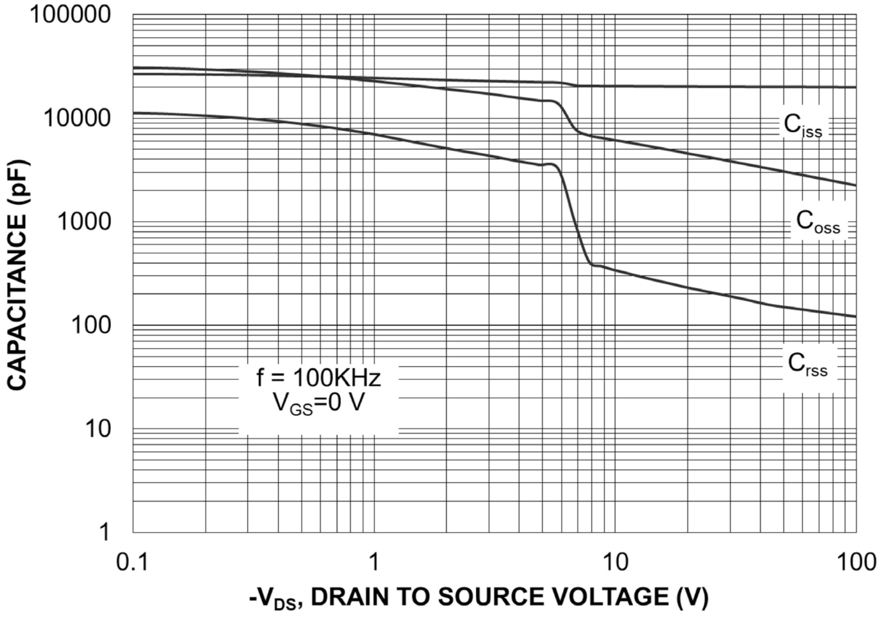


Figure 7. Capacitance vs. Drain-to-Source Voltage

TYPICAL CHARACTERISTIC

(M1/M1 SiC MOSFET SWITCHING CHARACTERISTIC)

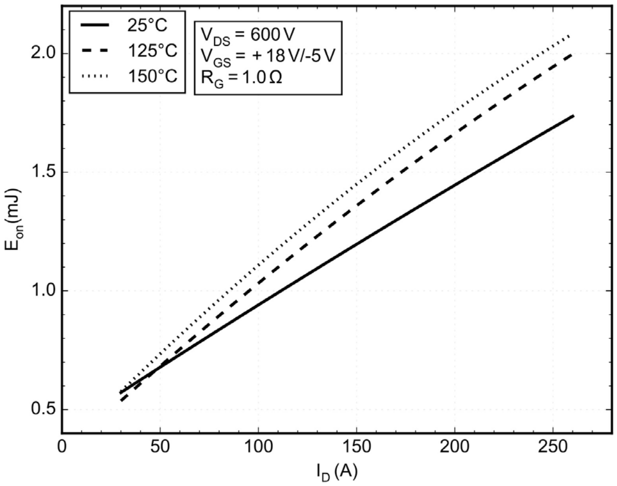


Figure 8. Typical Switching Loss Eon vs. ID

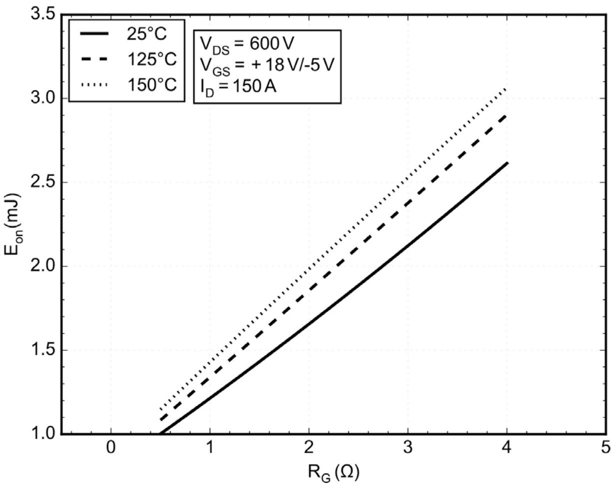


Figure 9. Typical Switching Loss Eon vs. Rg

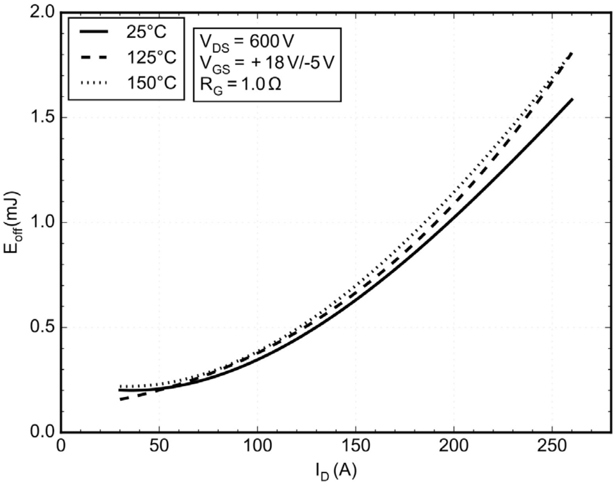


Figure 10. Typical Switching Loss Eoff vs. ID

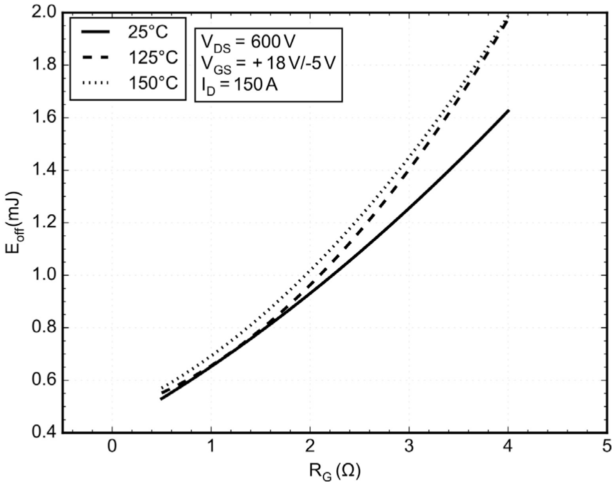


Figure 11. Typical Switching Loss Eoff vs. Rg

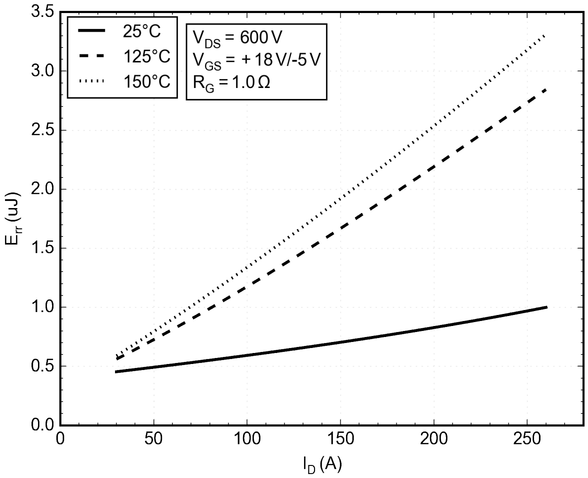


Figure 12. E_{rr} vs. I_D

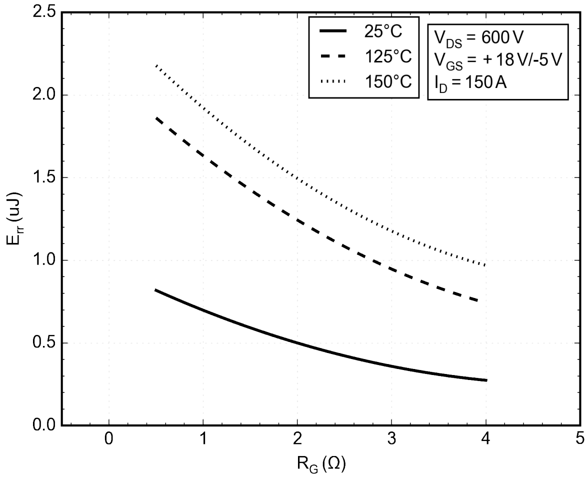


Figure 13. E_{rr} vs. R_G

TYPICAL CHARACTERISTIC

(M1/M1 SiC MOSFET SWITCHING CHARACTERISTIC)

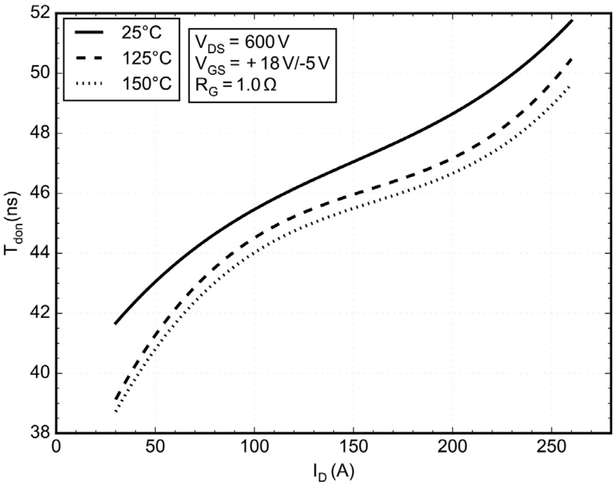


Figure 14. Typical Switching Loss Tdon vs. ID

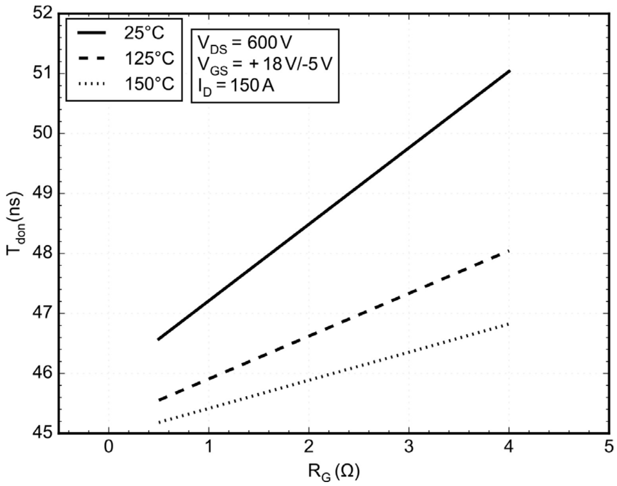


Figure 15. Typical Switching Loss Tdon vs. Rg

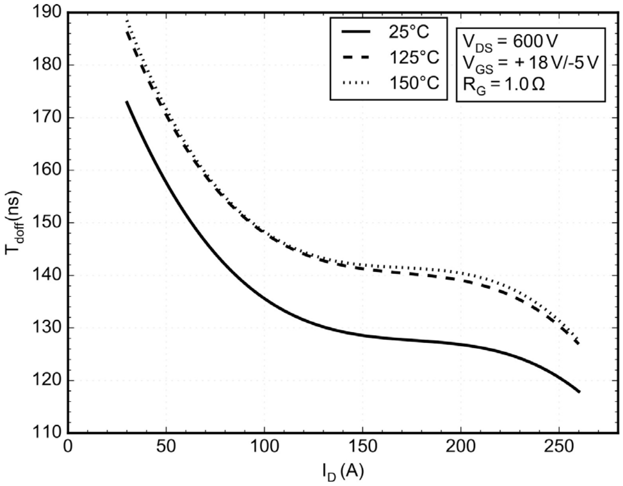


Figure 16. Typical Switching Loss Tdoff vs. ID

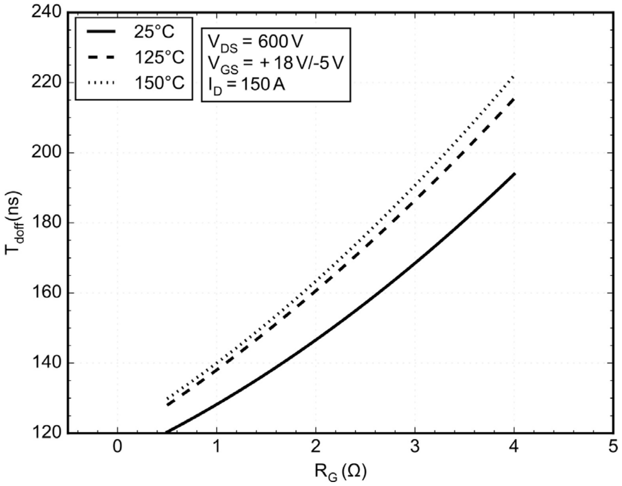


Figure 17. Typical Switching Loss Tdoff vs. Rg

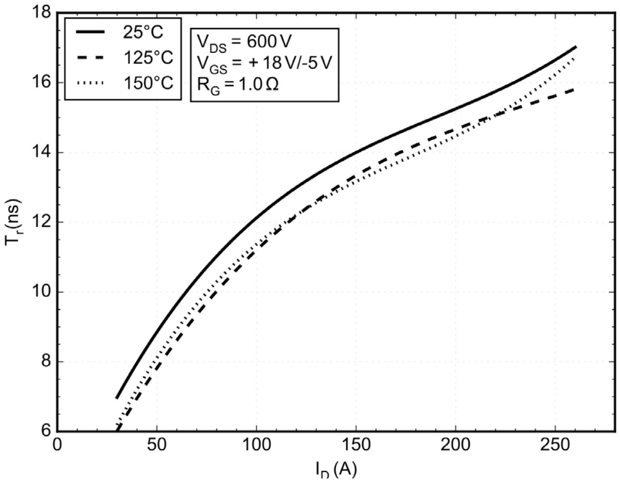


Figure 18. Typical Switching Loss Tr vs. ID

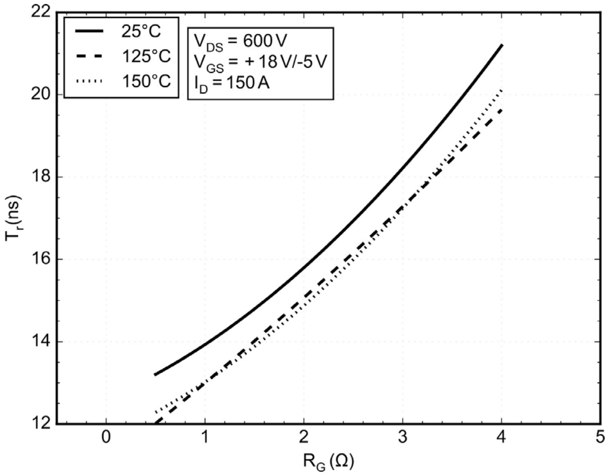


Figure 19. Typical Switching Loss Tr vs. Rg

TYPICAL CHARACTERISTIC

(M1/M1 SiC MOSFET SWITCHING CHARACTERISTIC)

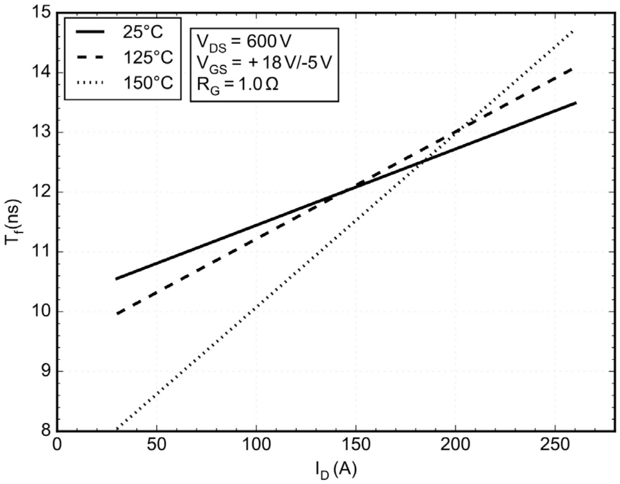


Figure 20. Typical Switching Loss Tf vs. ID

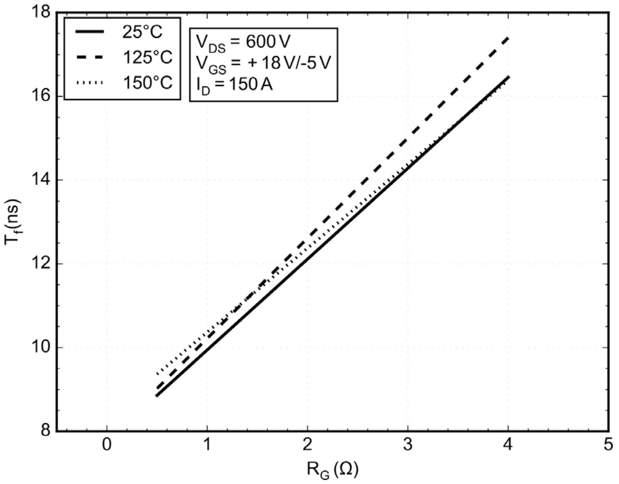


Figure 21. Typical Switching Loss Tf vs. Rg

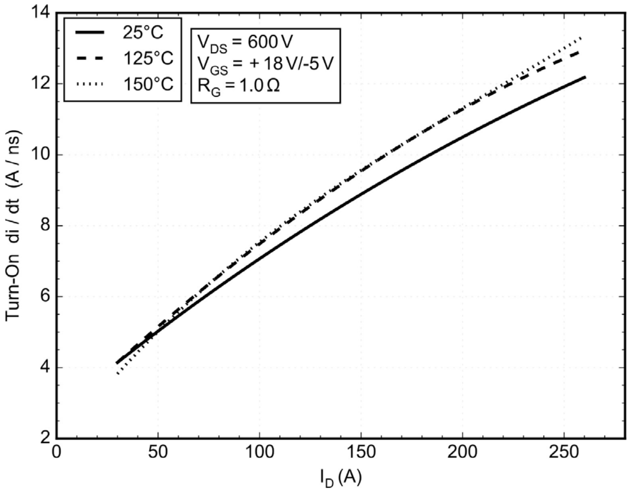


Figure 22. di/dt ON vs. ID

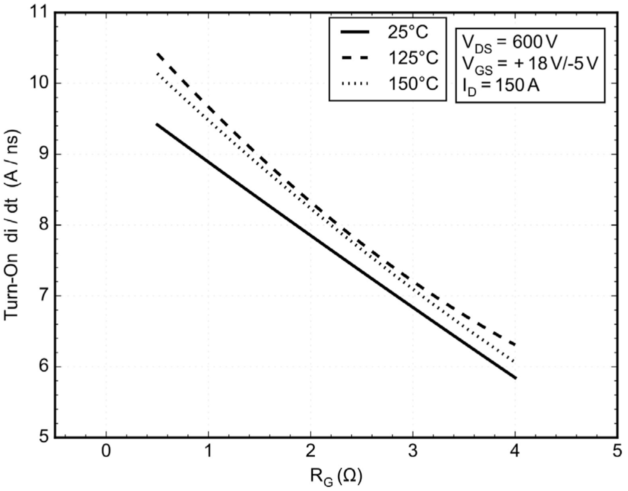


Figure 23. di/dt ON vs. RG

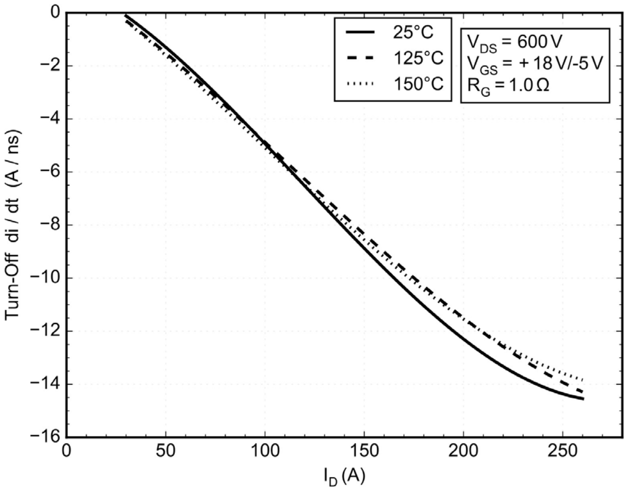


Figure 24. di/dt OFF vs. ID

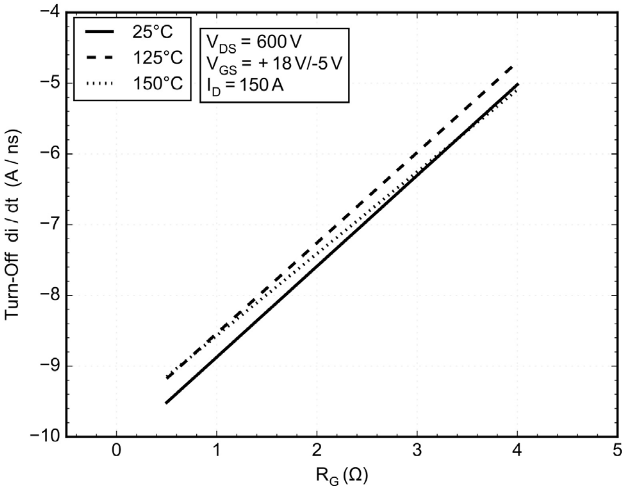


Figure 25. di/dt OFF vs. RG

TYPICAL CHARACTERISTIC

(M1/M1 SiC MOSFET SWITCHING CHARACTERISTIC)

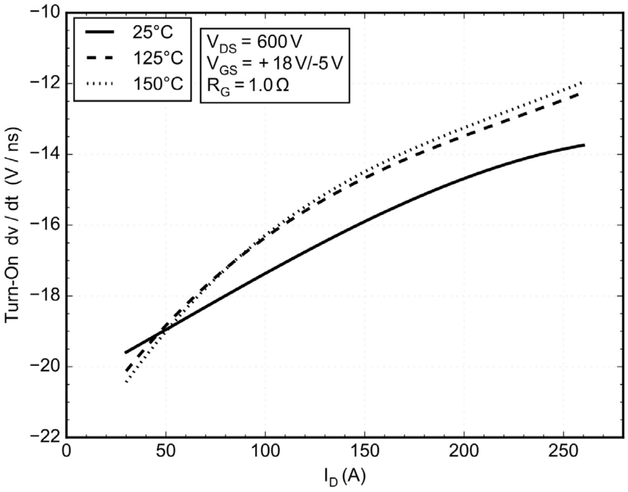


Figure 26. dv/dt ON vs. ID

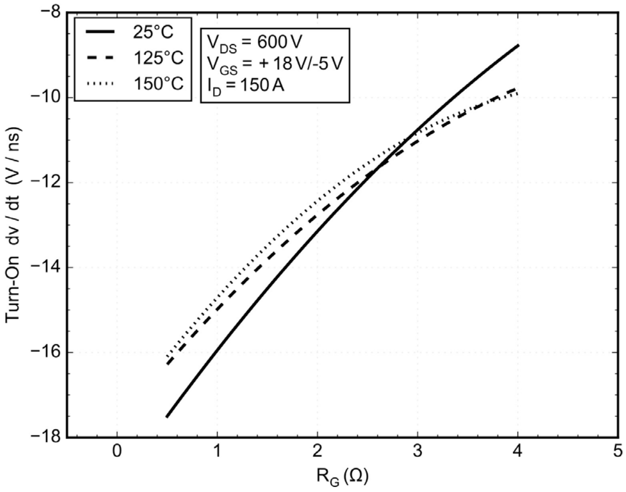


Figure 27. dv/dt ON vs. RG

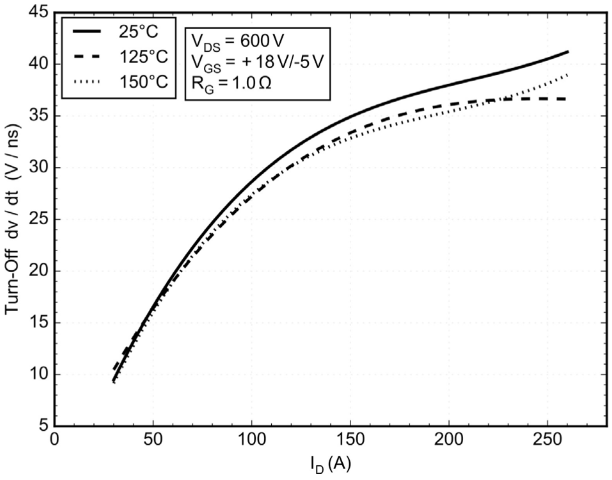


Figure 28. dv/dt OFF vs. ID

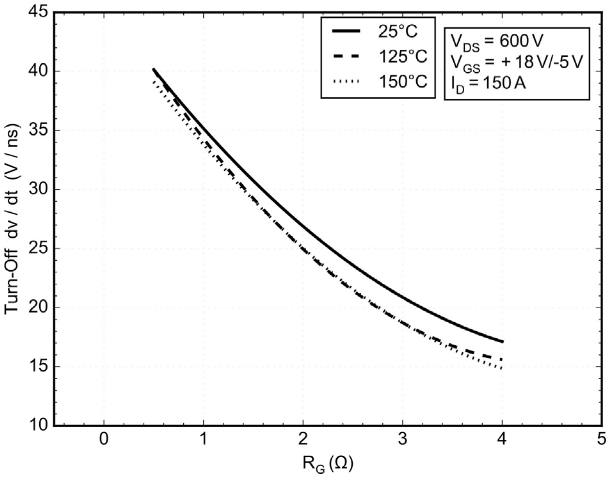


Figure 29. dv/dt OFF vs. RG

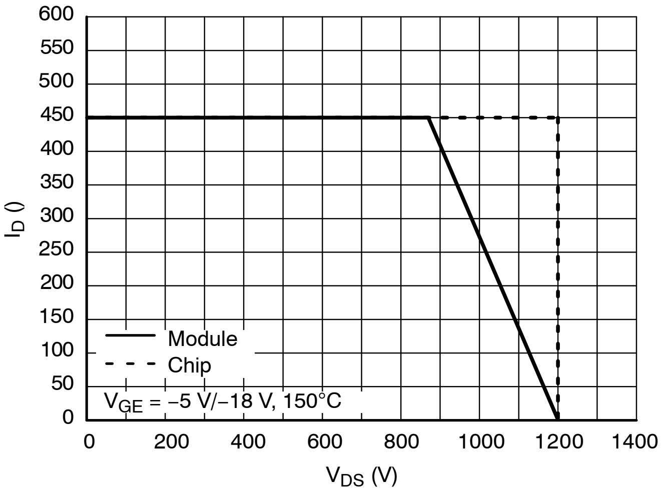


Figure 30. I_D vs. V_{DS}

TYPICAL CHARACTERISTIC

(M1/M1 SiC MOSFET CHARACTERISTIC)

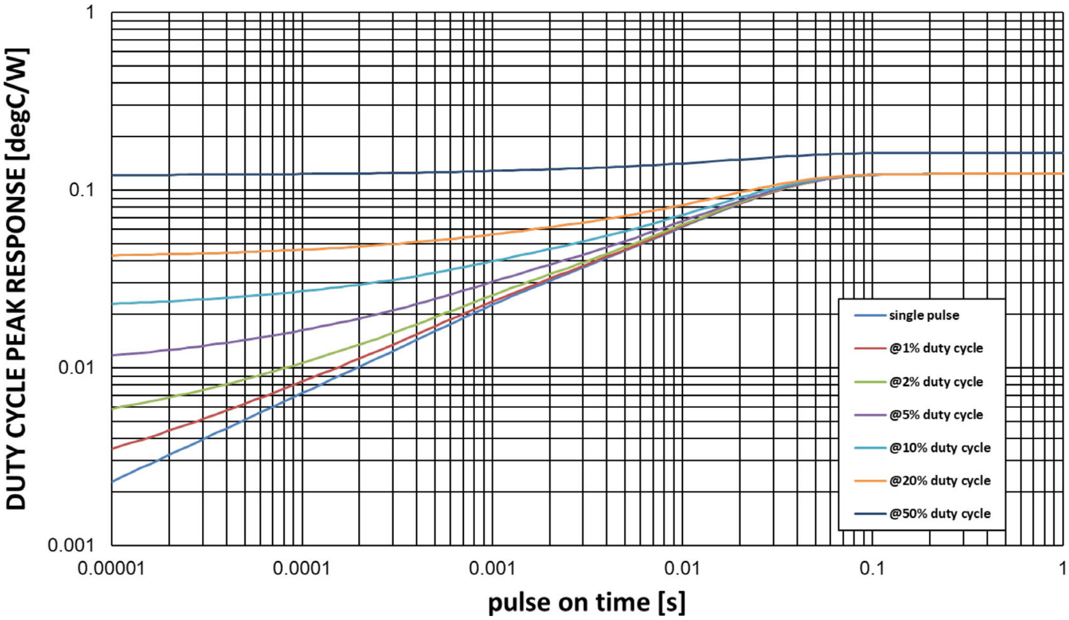


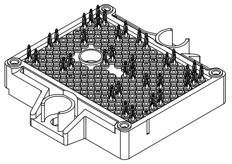
Figure 31. MOSFET Junction-to-Case Transient Thermal Impedance

Table 1. FOSTER NETWORKS – M1, M2

Foster Element #	M1		M2	
	Rth (K/W)	Cth (Ws/K)	Rth (K/W)	Cth (Ws/K)
1	0.002696906	0.004098379	0.002720288	0.004514937
2	0.003154311	0.026752259	0.00279686	0.032605348
3	0.015256456	0.052736204	0.013216449	0.058320259
4	0.014153093	0.371590626	0.012551589	0.372984673
5	0.091397895	0.28781396	0.088665137	0.266129557

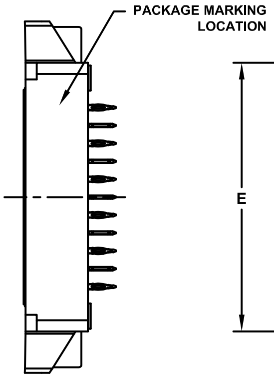
Table 2. CAUER NETWORKS – M1, M2

Cauer Element #	M1		M2	
	Rth (K/W)	Cth (Ws/K)	Rth (K/W)	Cth (Ws/K)
1	0.004167497	0.00326257	0.004133872	0.003626576
2	0.007647217	0.015697697	0.00758189	0.018148858
3	0.021401687	0.029324508	0.019509431	0.030697141
4	0.052959414	0.148179175	0.05061641	0.137728307
5	0.040482846	0.319017867	0.038108721	0.290558855

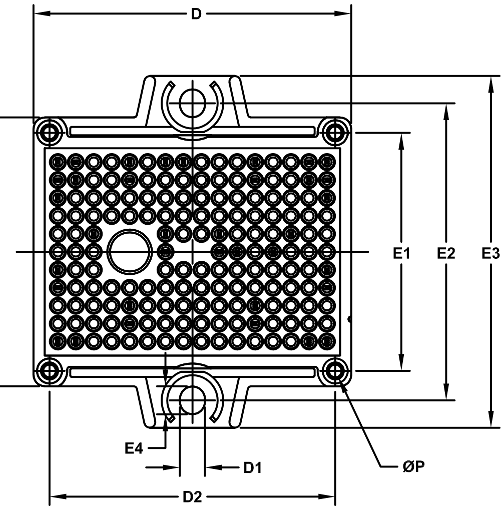


PIM36 56.70x42.50x12.00
CASE 180BY
ISSUE E

DATE 20 DEC 2023



SIDE VIEW

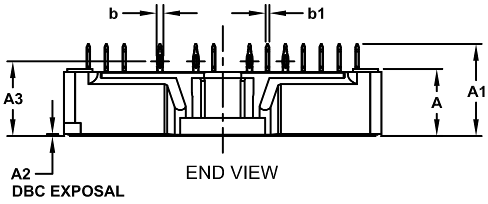


TOP VIEW

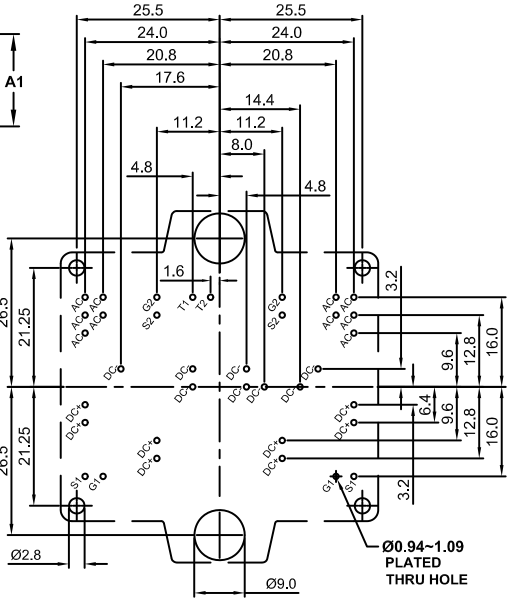
NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS
2. PIN POSITION TOLERANCE IS ± 0.4mm
3. PRESS FIT PIN

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.65	12.00	12.35
A1	16.10	16.50	16.90
A2	0.00	0.35	0.60
A3	12.95	13.35	13.75
b	1.15	1.20	1.25
b1	0.59	0.64	0.69
D	56.40	56.70	57.00
D1	4.40	4.50	4.60
D2	50.85	51.00	51.15
E	47.70	48.00	48.30
E1	42.35	42.50	42.65
E2	52.90	53.00	53.10
E3	62.30	62.80	63.30
E4	4.90	5.00	5.10
P	2.20	2.30	2.40

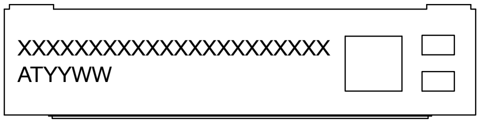


END VIEW

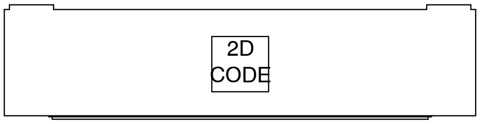


RECOMMENDED MOUNTING PATTERN

GENERIC MARKING DIAGRAM*



FRONTSIDE MARKING



BACKSIDE MARKING

XXXXX = Specific Device Code
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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