

MOSFET – SiC Power, Single N-Channel, T2PAK

650 V, 12 mΩ, 180 A

NVT2012N065M2

Features

- Typ. $R_{DS(on)}$ = 12 mΩ @ V_{GS} = 18 V
- Ultra Low Gate Charge (typ. $Q_{G(tot)}$ = 256 nC)
- Low Effective Output Capacitance (typ. C_{oss} = 431 pF)
- 100% UIL Tested
- Qualified According to AEC-Q101
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

Typical Applications

- Automotive On and Off Board Charger
- Automotive DC/DC Converter for EV/HEV

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

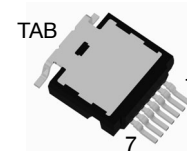
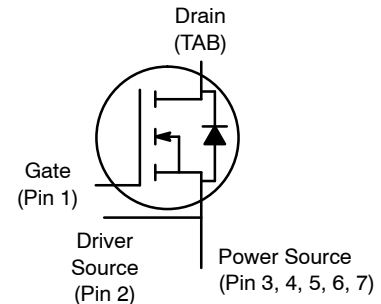
Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	650	V
Gate-to-Source Voltage			V _{GS}	+22/-8	V
Recommended Operation Values of Gate – Source Voltage		T _C < 175 °C	V _{GSop}	+18/-5	V
Continuous Drain Current R _{θJC}	Steady State	T _C = 25 °C	I _{DC}	180	A
Power Dissipation R _{θJC}			P _{DC}	750	W
Continuous Drain Current R _{θJC}	Steady State	T _C = 100 °C	I _{DC}	127	A
Power Dissipation R _{θJC}			P _{DC}	375	W
Pulsed Drain Current (Note 1)		T _A = 25 °C	I _{DM}	482	A
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +175	°C
Source Current (Body Diode)			I _S	157	A
Continuous Drain-Source Diode Forward Current			I _{SD}	157	A
Pulsed Drain-Source Diode Forward Current (Note 1)			I _{SDM}	482	A
Single Pulse Drain-to-Source Avalanche Energy (I _L = 13 A _{pk} , L = 1 mH) (Note 2)			E _{AS}	84.5	mJ

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Single pulse, limited by max junction temperature.
2. E_{AS} of 84.5 mJ is based on starting $T_J = 25\text{ °C}$; $L = 1\text{ mH}$, $I_{AS} = 13\text{ A}$, $V_{DD} = 50\text{ V}$, $V_{GS} = 18\text{ V}$.

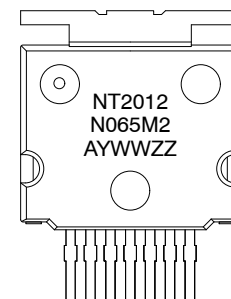
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
650 V	18 mΩ @ 18 V	180 A

N-CHANNEL MOSFET



**T2PAK
CASE 763AC**

MARKING DIAGRAM



NT2012N065M2 = Specific Device Code
A = Assembly Site
WW = Work Week Number
Y = Year of Production, Last Number
ZZ = Assembly Lot Number, Last Two Numbers

ORDERING INFORMATION

Device	Package	Shipping†
NVT2012N065M2	T2PAK-7L	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-to-Case (Note 3)	$R_{\theta JC}$	0.2	°C/W

3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

Table 2. ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$ $V_{GS} = -5\text{ V}, I_D = 1\text{ mA}$	650 650			V
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = -40\text{ }^{\circ}\text{C}$ $V_{GS} = -5\text{ V}, I_D = 1\text{ mA}, T_J = -40\text{ }^{\circ}\text{C}$ (Note 5)	650 650			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 650\text{ V}, T_J = 25\text{ }^{\circ}\text{C}$		1	40	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 650\text{ V}, T_J = 175\text{ }^{\circ}\text{C}$ (Note 5)			100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$	-250			nA
		$V_{GS} = +22\text{ V}, V_{DS} = 0\text{ V}$			250	

ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 25\text{ mA}$	1.8	2.8	4.3	V
Recommended Gate Voltage	V_{GSOP}		-5		+18	V
Drain-to-Source On Resistance (Note 5)	$R_{DS(on)}$	$V_{GS} = 18\text{ V}, I_D = 75\text{ A}, T_J = 25\text{ }^{\circ}\text{C}$		12	18	$\text{m}\Omega$
		$V_{GS} = 18\text{ V}, I_D = 75\text{ A}, T_J = 150\text{ }^{\circ}\text{C}$		14.4		
Forward Transconductance	g_{FS}	$V_{DS} = 20\text{ V}, I_D = 75\text{ A}$		75		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz},$ $V_{DS} = 325\text{ V}$ (Note 5)		5389		pF
Output Capacitance	C_{OSS}			431		
Reverse Transfer Capacitance	C_{RSS}			40		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -5/18\text{ V}, V_{DS} = 520\text{ V},$ $I_D = 75\text{ A}$ (Note 5)		256		nC
Threshold Gate Charge	$Q_{G(TH)}$			43		
Gate-to-Source Charge	Q_{GS}			72		
Gate-to-Drain Charge	Q_{GD}			73		
Gate-Resistance	R_G	$f = 1\text{ MHz}$		1.6		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -5/18\text{ V}, V_{DS} = 400\text{ V},$ $I_D = 75\text{ A}, R_G = 2\text{ }\Omega,$ $L_{\text{stray}} = 13\text{ nH},$ Inductive Load (Notes 4, 5)		62		ns
Rise Time	t_r			23		
Turn-Off Delay Time	$t_{d(OFF)}$			64		
Fall Time	t_f			12		
Turn-On Switching Loss	E_{ON}			329		μJ
Turn-Off Switching Loss	E_{OFF}			210		
Total Switching Loss	E_{TOT}			539		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = -5\text{ V}, I_{SD} = 75\text{ A}, T_J = 25\text{ }^{\circ}\text{C}$		3.7		V
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NVT2012N065M2

Table 2. ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	$V_{GS} = -5/18\text{ V}$, $I_{SD} = 75\text{ A}$, $di_S/dt = 4000\text{ A}/\mu\text{s}$, $V_{DS} = 520\text{ V}$ (Note 5)		30		ns
Reverse Recovery Charge	Q_{RR}			680		nC
Reverse Recovery Energy	E_{REC}			173		μJ
Peak Reverse Recovery Current	I_{RRM}			46		A
Charge Time	T_a			12.4		ns
Discharge Time	T_b			17		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. E_{ON}/E_{OFF} result is with body diode.

5. Defined by design, not subject to production test.

TYPICAL CHARACTERISTICS

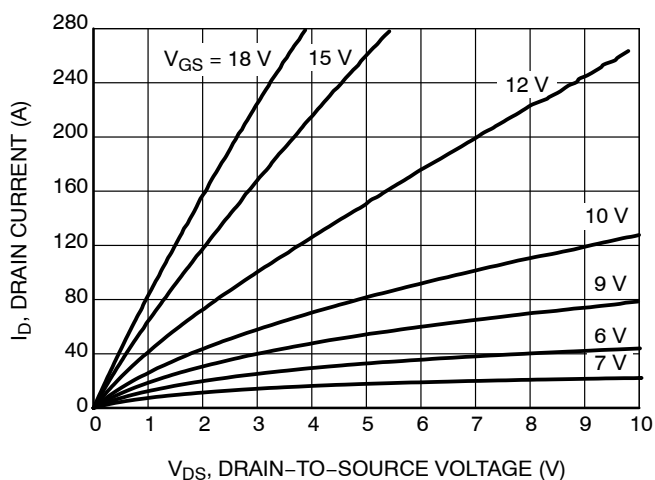


Figure 1. On-Region Characteristics

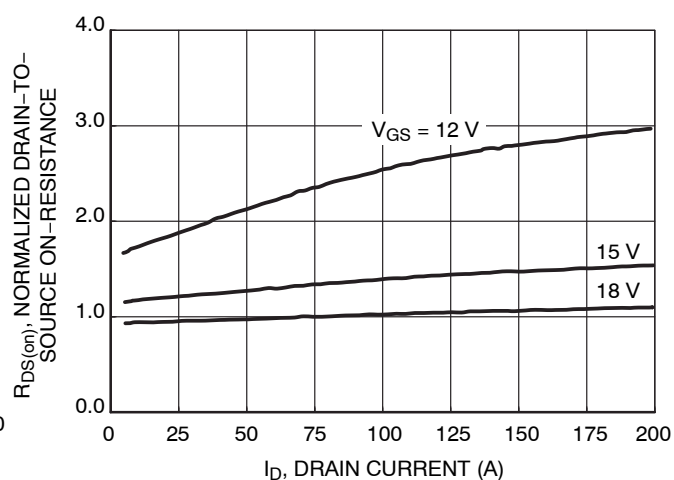


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

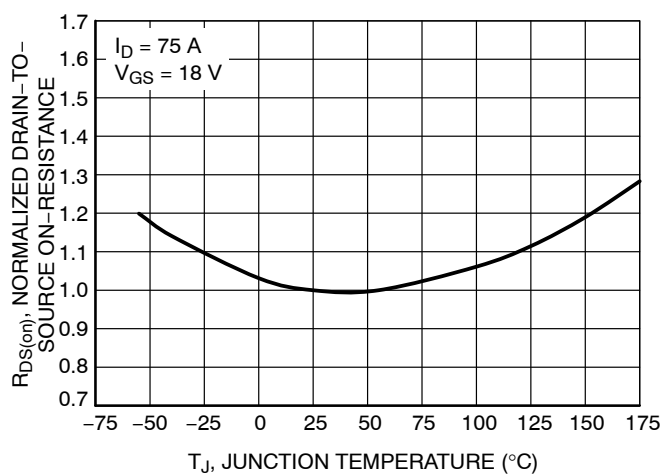


Figure 3. On-Resistance Variation with Temperature

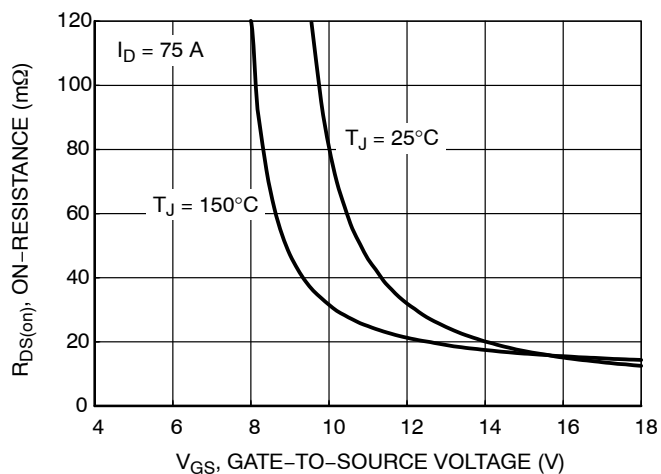


Figure 4. On-Resistance vs. Gate-to-Source Voltage

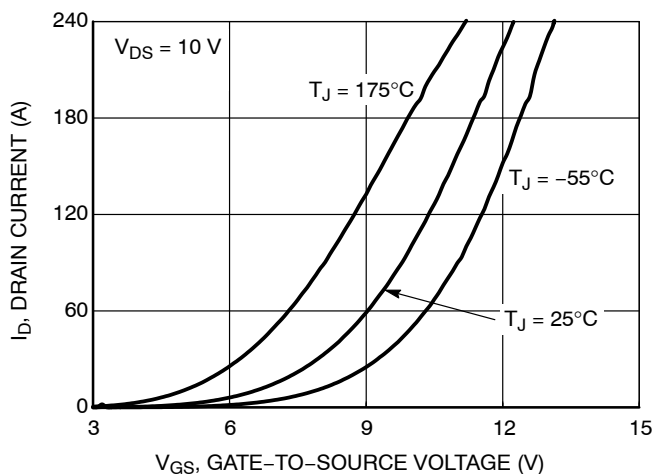


Figure 5. Transfer Characteristics

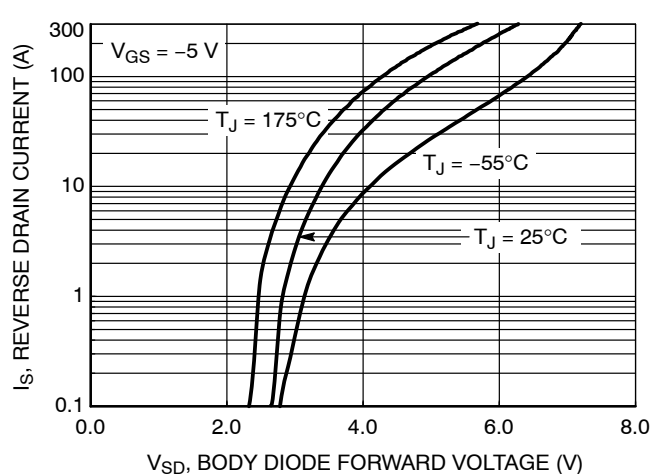


Figure 6. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS

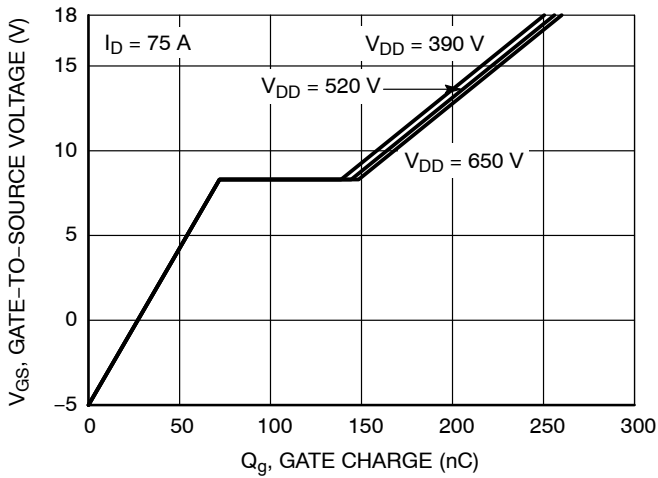


Figure 7. Gate-to-Source Voltage vs. Total Charge

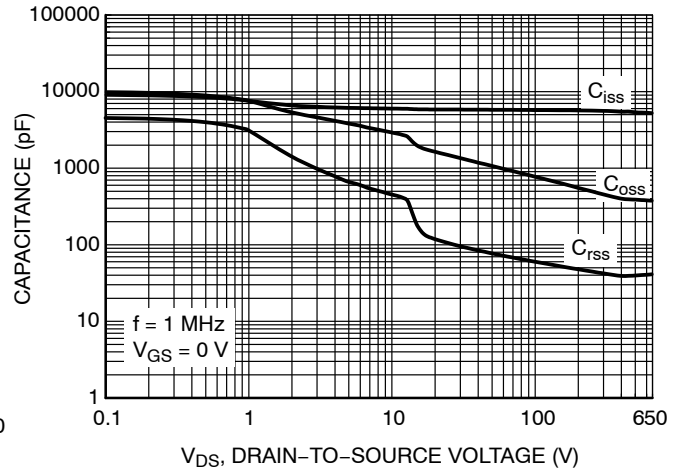


Figure 8. Capacitance vs. Drain-to-Source Voltage

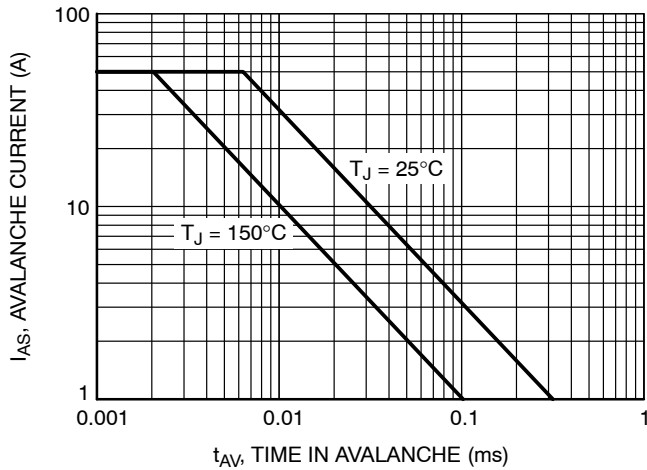


Figure 9. Unclamped Inductive Switching Capability

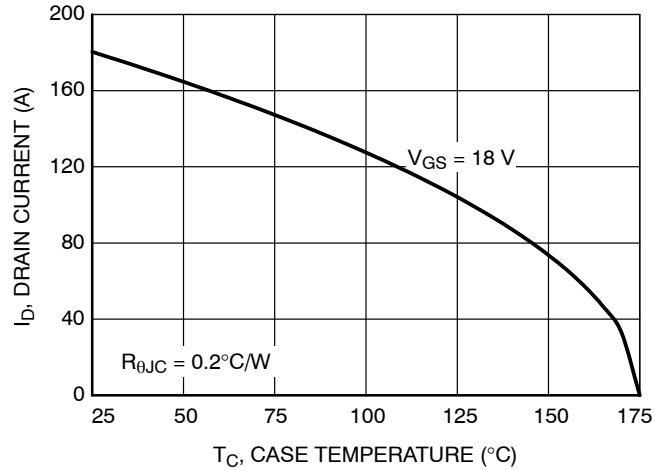


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

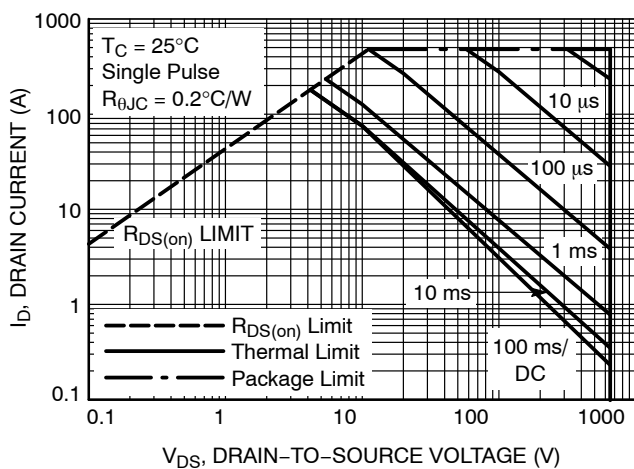


Figure 11. Safe Operating Area

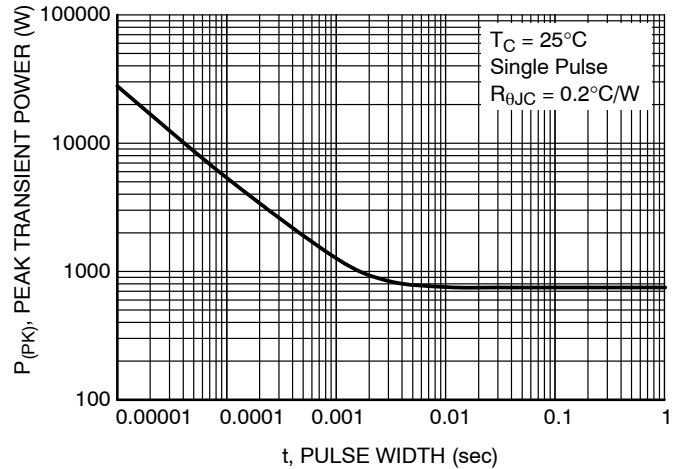
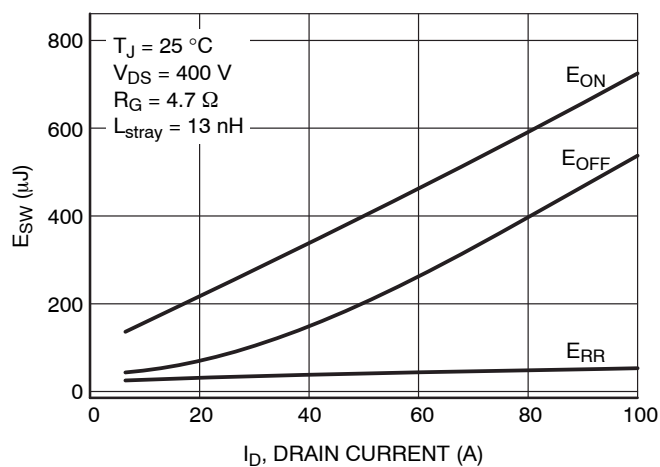
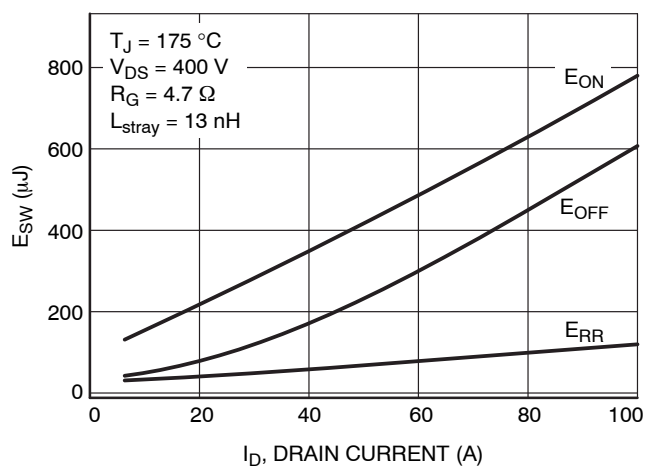
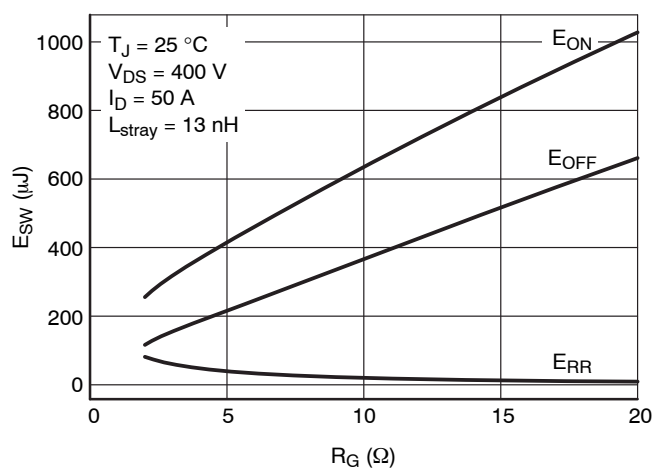
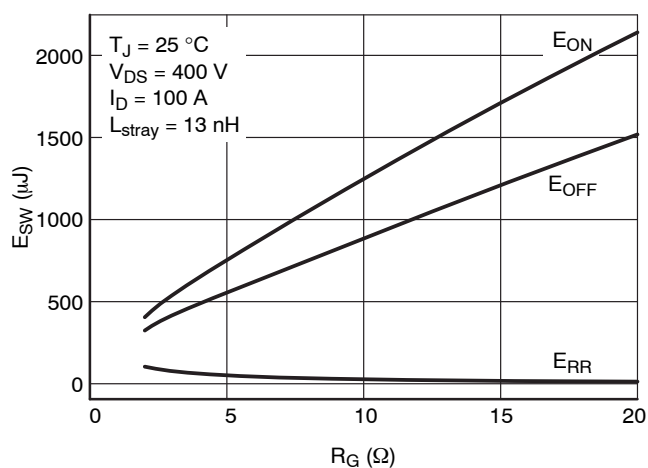
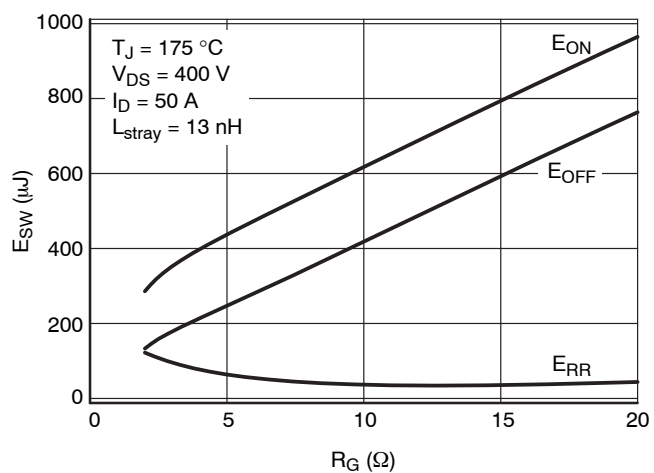
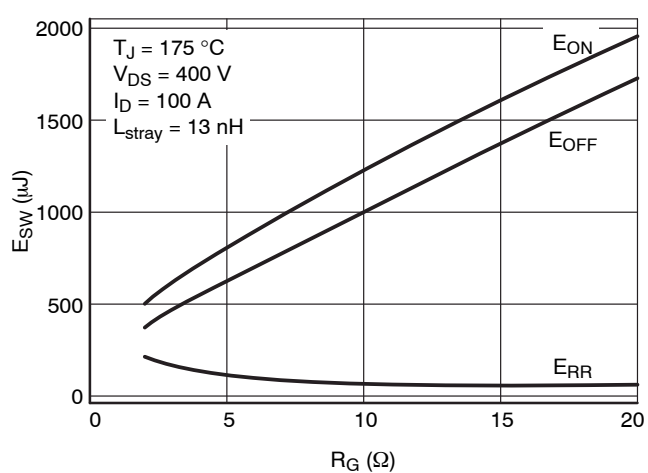


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

Figure 13. E_{SW} vs. I_D Figure 14. E_{SW} vs. I_D Figure 15. E_{SW} vs. R_G Figure 16. E_{SW} vs. R_G Figure 17. E_{SW} vs. R_G Figure 18. E_{SW} vs. R_G

TYPICAL CHARACTERISTICS

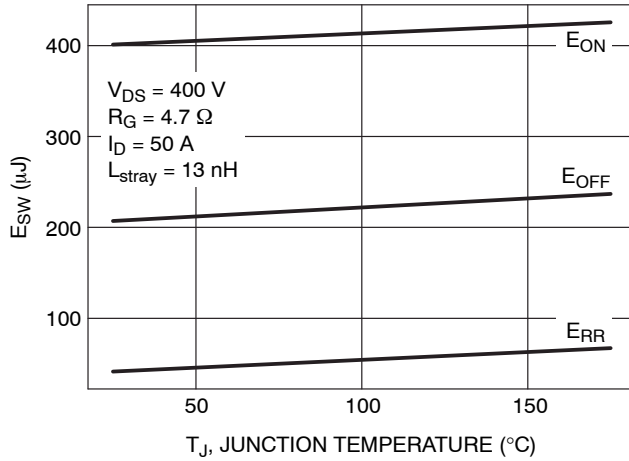


Figure 19. E_{SW} vs. T_J

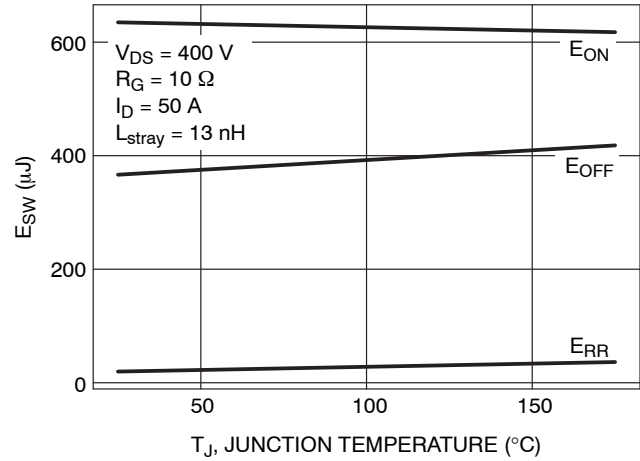


Figure 20. E_{SW} vs. T_J

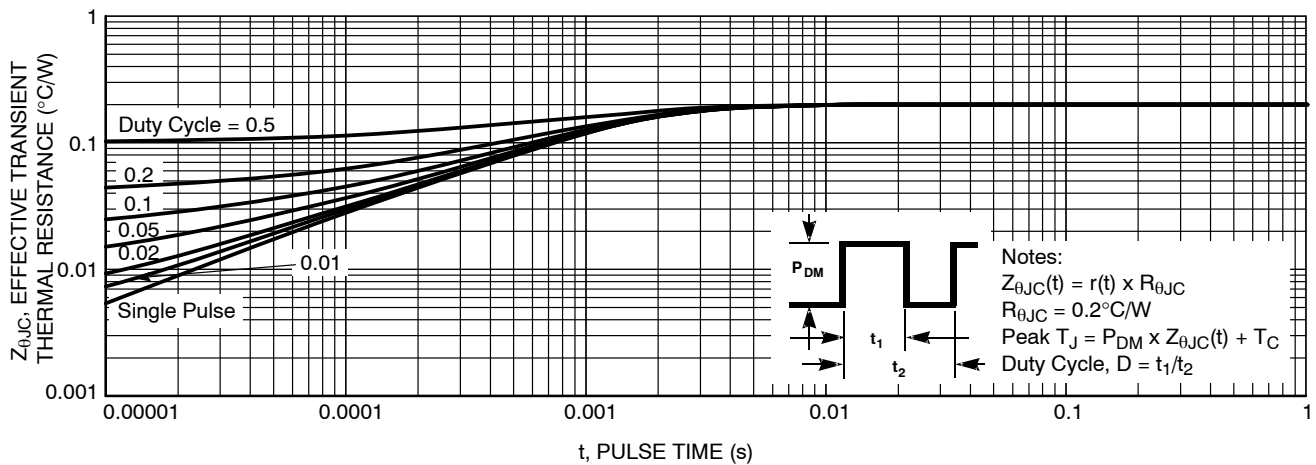


Figure 21. Junction-to-Case Transient Thermal Response Curve

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial data sheet release	9/29/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

PACKAGE DIMENSIONS

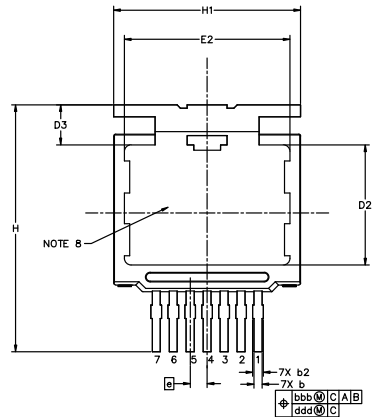
T2PAK-7 11.80x14.00x3.50, 1.27P
CASE 763AC
ISSUE A

NOTES:

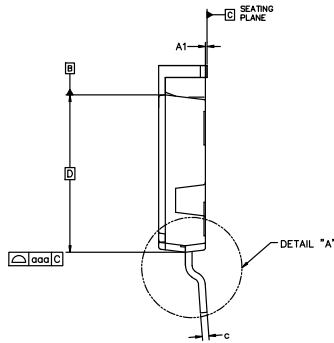
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b, b2, b3 AND c TO BE MEASURED ON FLAT SECTION OF THE LEAD BETWEEN 0.13 AND 0.25mm FROM LEAD TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO THE TERMINALS AND EXPOSED PAD.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
8. ALLOWABLE ENCROACHED FLASH ON HEAT SINK AREA MAXIMUM OF 0.05mm.
9. EJECTOR PINS $\phi 12.5$ mm REF.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	3.53	3.63	3.73
A1	0.07	0.13	0.18
A2	3.40	3.50	3.60
b	0.50	0.60	0.70
b2	0.50	0.75	1.00
b3	0.80	0.90	1.00
c	0.40	0.50	0.60
c2	0.40	0.50	0.60
D	11.80 BSC		
D2	8.90	9.00	9.10
D3	3.00	3.10	3.20
D4	3.80	3.90	4.00
D5	2.10	2.20	2.30
E	14.00 BSC		
E2	12.30	12.40	12.50
e	1.27 BSC		

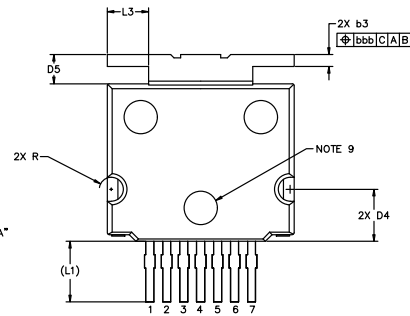
MILLIMETERS			
DIM	MIN	NOM	MAX
H	18.00	18.50	19.00
H1	13.80	14.00	14.20
L	2.42	2.52	2.62
L1	4.53 REF		
L2	0.25 BSC		
L3	3.00	3.10	3.20
R	0.80	---	1.00
θ	0°	---	8°
$\theta 1$	0°	---	8°
TOLERANCE FORM AND POSITION			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		



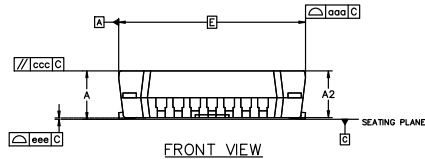
TOP VIEW



SIDE VIEW



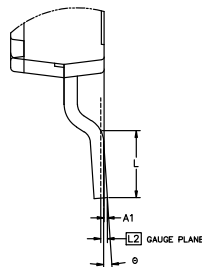
BOTTOM VIEW



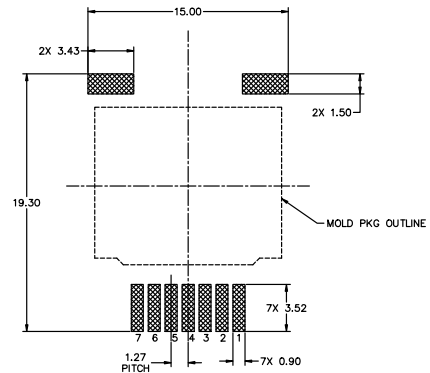
FRONT VIEW



END VIEW



DETAIL "A"
SCALE 2:1



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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