

# MOSFET – SiC Power, Single N-Channel, T2PAK

650 V, 12 mΩ, 180 A

**NVT2012N065M2**

## Features

- Typ.  $R_{DS(on)} = 12 \text{ m}\Omega$  @  $V_{GS} = 18 \text{ V}$
- Ultra Low Gate Charge (typ.  $Q_{G(\text{tot})} = 256 \text{ nC}$ )
- Low Effective Output Capacitance (typ.  $C_{oss} = 431 \text{ pF}$ )
- 100% UIL Tested
- Qualified According to AEC-Q101
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

## Typical Applications

- Automotive On and Off Board Charger
- Automotive DC/DC Converter for EV/HEV

## MAXIMUM RATINGS (T<sub>J</sub> = 25 °C unless otherwise noted)

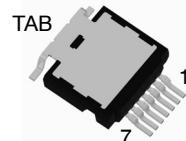
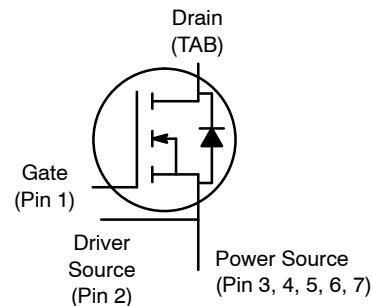
Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V <sub>DSS</sub>	650	V	
Gate-to-Source Voltage		V <sub>GS</sub>	+22/-8	V	
Recommended Operation Values of Gate – Source Voltage	T <sub>C</sub> < 175 °C	V <sub>GSop</sub>	+18/-5	V	
Continuous Drain Current R <sub>θJC</sub>	Steady State	T <sub>C</sub> = 25 °C	I <sub>DC</sub>	180	A
Power Dissipation R <sub>θJC</sub>			P <sub>DC</sub>	750	W
Continuous Drain Current R <sub>θJC</sub>	Steady State	T <sub>C</sub> = 100 °C	I <sub>DC</sub>	127	A
Power Dissipation R <sub>θJC</sub>			P <sub>DC</sub>	375	W
Pulsed Drain Current (Note 1)		T <sub>A</sub> = 25 °C	I <sub>DM</sub>	482	A
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175		°C
Source Current (Body Diode)		I <sub>S</sub>	157	A	
Continuous Drain-Source Diode Forward Current		I <sub>SD</sub>	157	A	
Pulsed Drain-Source Diode Forward Current (Note 1)		I <sub>SDM</sub>	482	A	
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L</sub> = 13 A <sub>pk</sub> , L = 1 mH) (Note 2)		E <sub>AS</sub>	84.5	mJ	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Single pulse, limited by max junction temperature.
2. E<sub>AS</sub> of 84.5 mJ is based on starting T<sub>J</sub> = 25 °C; L = 1 mH, I<sub>AS</sub> = 13 A, V<sub>DD</sub> = 50 V, V<sub>GS</sub> = 18 V.

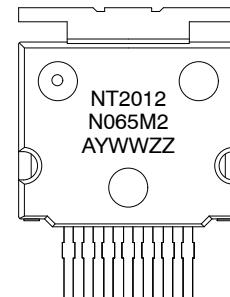
V <sub>(BR)DSS</sub>	R <sub>DS(ON) MAX</sub>	I <sub>D MAX</sub>
650 V	18 mΩ @ 18 V	180 A

## N-CHANNEL MOSFET



T2PAK  
CASE 763AC

## MARKING DIAGRAM



NT2012N065M2 = Specific Device Code

A = Assembly Site

WW = Work Week Number

Y = Year of Production, Last Number

ZZ = Assembly Lot Number, Last Two Numbers

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NVT2012N065M2	T2PAK-7L	800 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**Table 1. THERMAL CHARACTERISTICS**

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-to-Case (Note 3)	$R_{\theta JC}$	0.2	°C/W

3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

**Table 2. ELECTRICAL CHARACTERISTICS** ( $T_J = 25$  °C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 1$ mA $V_{GS} = -5$ V, $I_D = 1$ mA	650 650			V
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 1$ mA, $T_J = -40$ °C $V_{GS} = -5$ V, $I_D = 1$ mA, $T_J = -40$ °C (Note 5)	650 650			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0$ V, $V_{DS} = 650$ V, $T_J = 25$ °C		1	40	$\mu$ A
		$V_{GS} = 0$ V, $V_{DS} = 650$ V, $T_J = 175$ °C (Note 5)			100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = -8$ V, $V_{DS} = 0$ V	-250			nA
		$V_{GS} = +22$ V, $V_{DS} = 0$ V			250	
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 25$ mA	1.8	2.8	4.3	V
Recommended Gate Voltage	$V_{GSOP}$		-5		+18	V
Drain-to-Source On Resistance (Note 5)	$R_{DS(on)}$	$V_{GS} = 18$ V, $I_D = 75$ A, $T_J = 25$ °C		12	18	$m\Omega$
		$V_{GS} = 18$ V, $I_D = 75$ A, $T_J = 150$ °C		14.4		
Forward Transconductance	$g_{FS}$	$V_{DS} = 20$ V, $I_D = 75$ A		75		S
<b>CHARGES, CAPACITANCES &amp; GATE RESISTANCE</b>						
Input Capacitance	$C_{ISS}$	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = 325$ V (Note 5)		5389		$pF$
Output Capacitance	$C_{OSS}$			431		
Reverse Transfer Capacitance	$C_{RSS}$			40		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -5/18$ V, $V_{DS} = 520$ V, $I_D = 75$ A (Note 5)		256		$nC$
Threshold Gate Charge	$Q_{G(TH)}$			43		
Gate-to-Source Charge	$Q_{GS}$			72		
Gate-to-Drain Charge	$Q_{GD}$			73		
Gate-Resistance	$R_G$		$f = 1$ MHz		1.6	$\Omega$
<b>SWITCHING CHARACTERISTICS</b>						
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -5/18$ V, $V_{DS} = 400$ V, $I_D = 75$ A, $R_G = 2$ $\Omega$ , $L_{stray} = 13$ nH, Inductive Load (Notes 4, 5)		62		ns
Rise Time	$t_r$			23		
Turn-Off Delay Time	$t_{d(OFF)}$			64		
Fall Time	$t_f$			12		
Turn-On Switching Loss	$E_{ON}$			329		$\mu J$
Turn-Off Switching Loss	$E_{OFF}$			210		
Total Switching Loss	$E_{TOT}$			539		
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
Forward Diode Voltage	$V_{SD}$	$V_{GS} = -5$ V, $I_{SD} = 75$ A, $T_J = 25$ °C		3.7		V

**Table 2. ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
Reverse Recovery Time	$t_{RR}$	$V_{GS} = -5/18 \text{ V}$ , $I_{SD} = 75 \text{ A}$ , $dI_S/dt = 4000 \text{ A}/\mu\text{s}$ , $V_{DS} = 520 \text{ V}$ (Note 5)	30			ns
Reverse Recovery Charge	$Q_{RR}$		680			nC
Reverse Recovery Energy	$E_{REC}$		173			$\mu\text{J}$
Peak Reverse Recovery Current	$I_{RRM}$		46			A
Charge Time	$T_a$		12.4			ns
Discharge Time	$T_b$		17			ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4.  $E_{ON}/E_{OFF}$  result is with body diode.

5. Defined by design, not subject to production test.

## TYPICAL CHARACTERISTICS

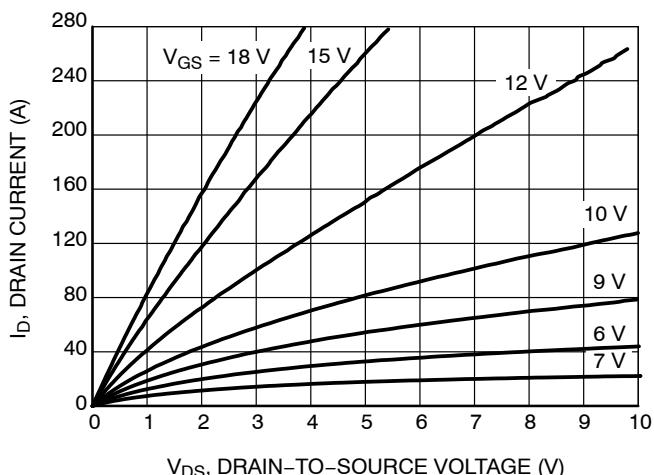


Figure 1. On-Region Characteristics

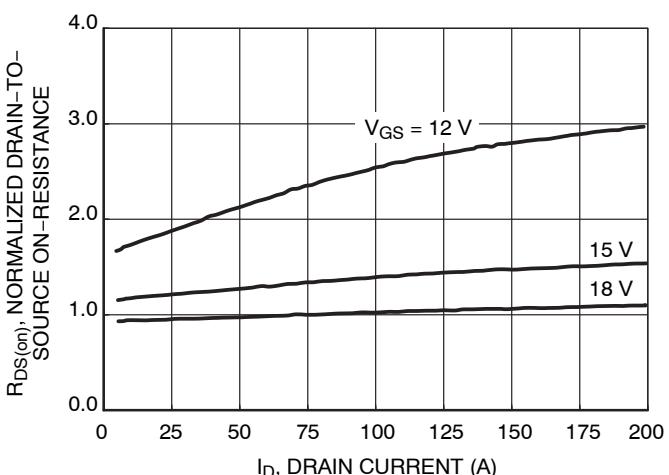


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

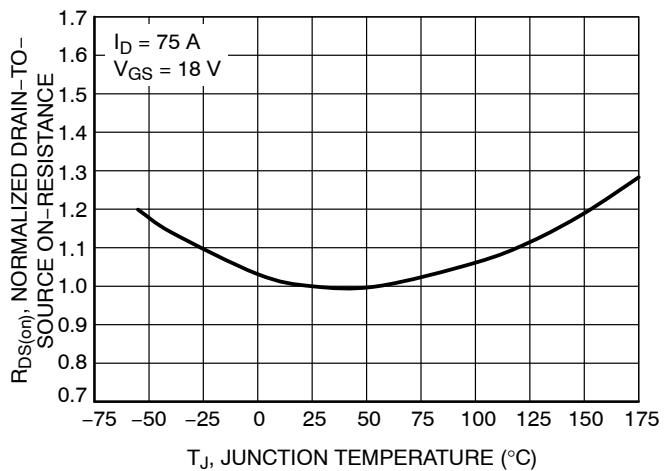


Figure 3. On-Resistance Variation with Temperature

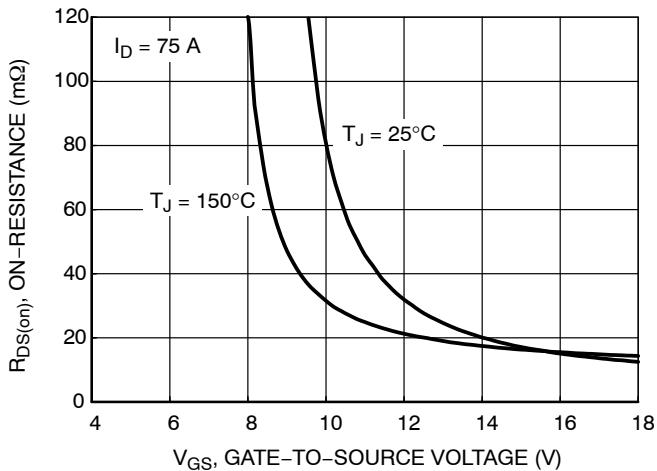


Figure 4. On-Resistance vs. Gate-to-Source Voltage

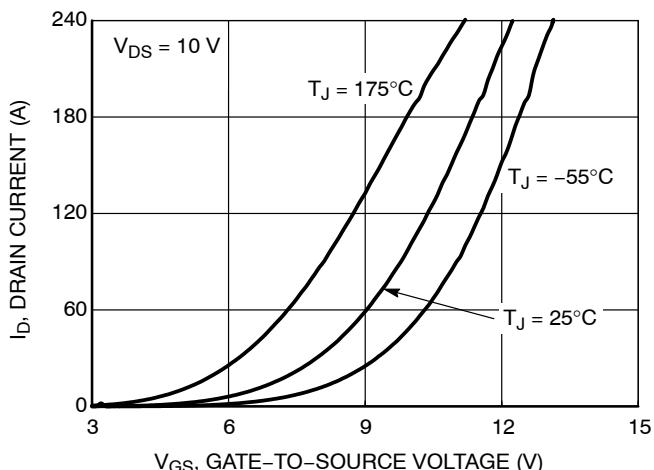


Figure 5. Transfer Characteristics

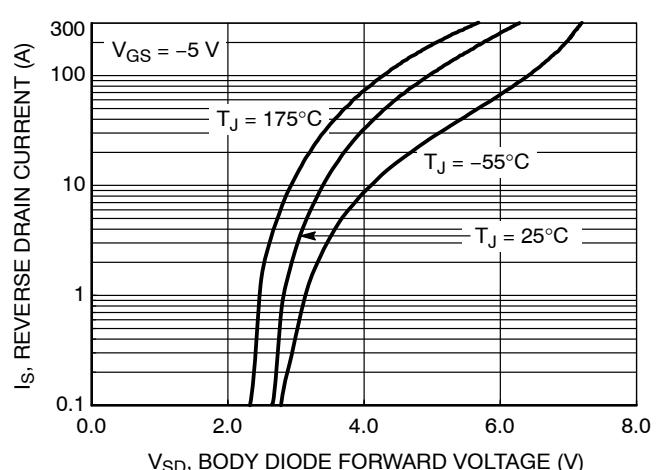


Figure 6. Diode Forward Voltage vs. Current

## TYPICAL CHARACTERISTICS

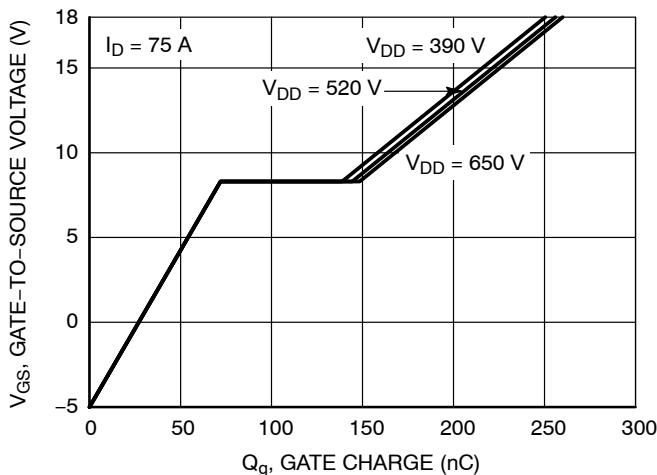


Figure 7. Gate-to-Source Voltage vs. Total Charge

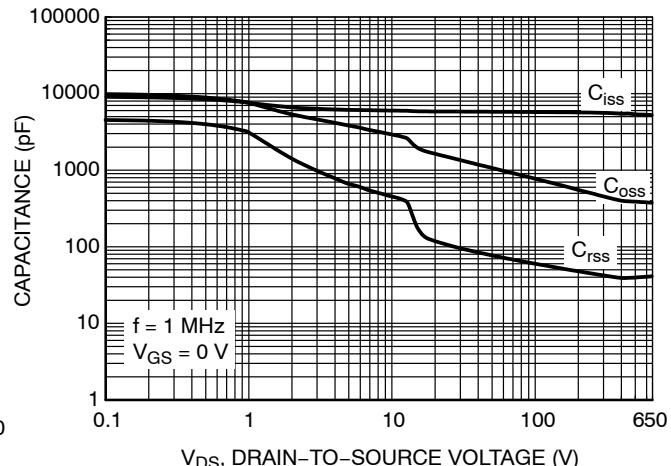


Figure 8. Capacitance vs. Drain-to-Source Voltage

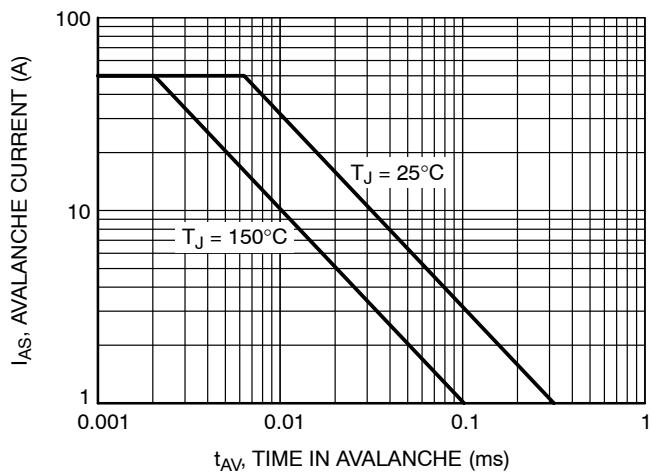


Figure 9. Unclamped Inductive Switching Capability

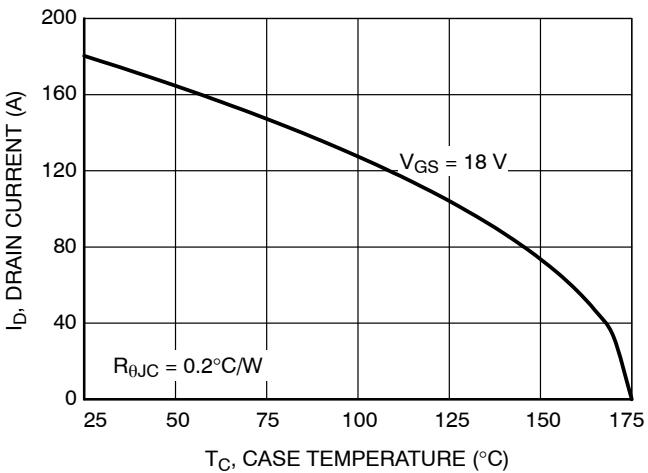


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

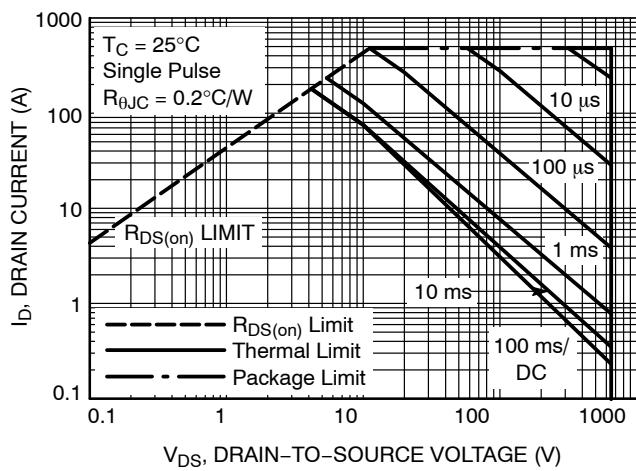


Figure 11. Safe Operating Area

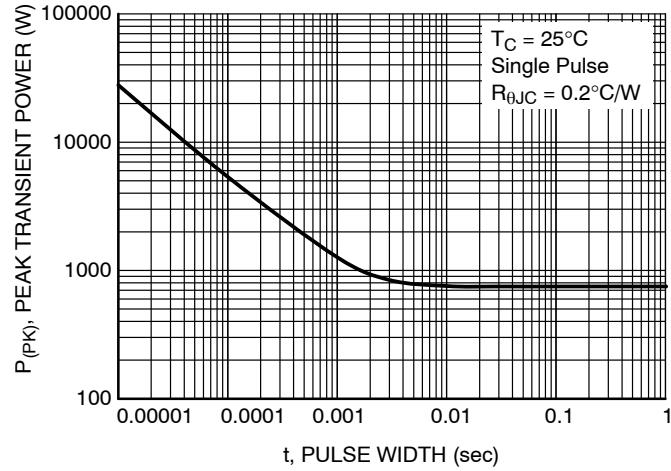


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

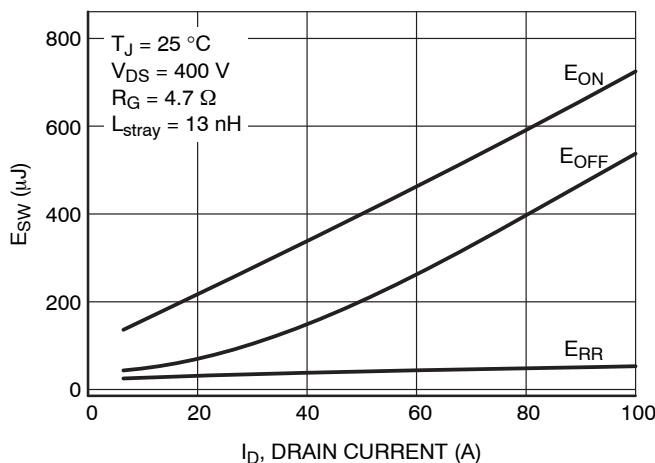


Figure 13.  $E_{SW}$  vs.  $I_D$

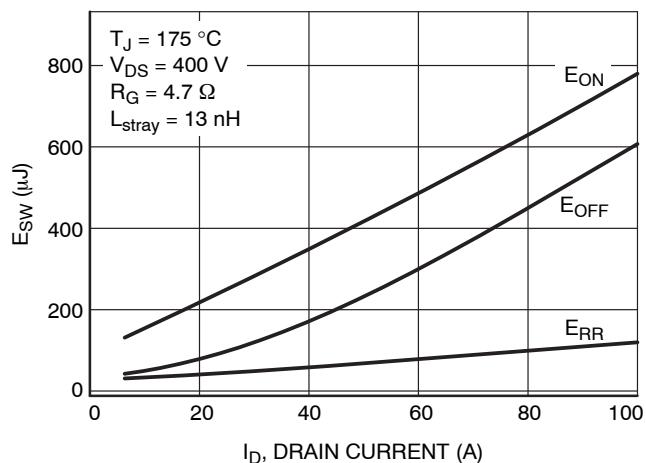


Figure 14.  $E_{SW}$  vs.  $I_D$

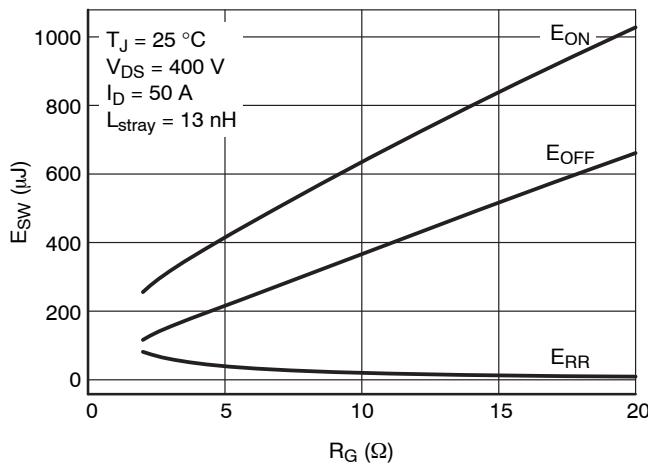


Figure 15.  $E_{SW}$  vs.  $R_G$

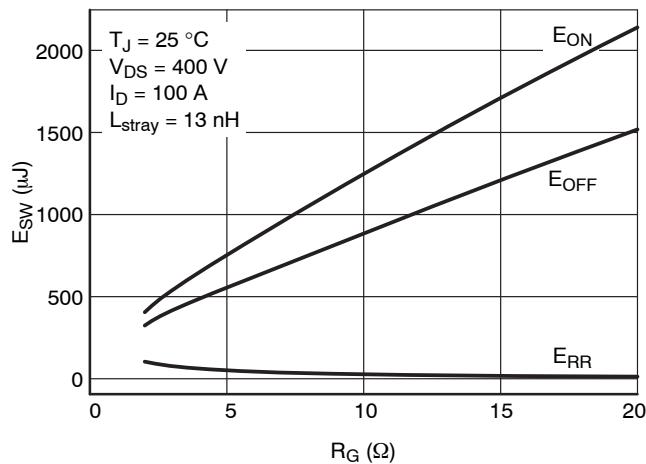


Figure 16.  $E_{SW}$  vs.  $R_G$

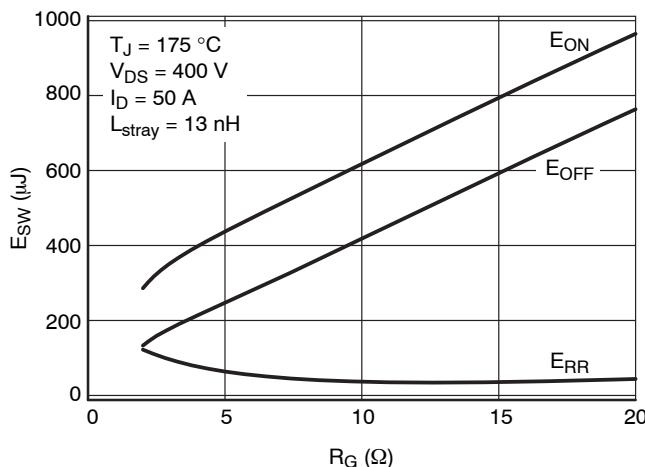


Figure 17.  $E_{SW}$  vs.  $R_G$

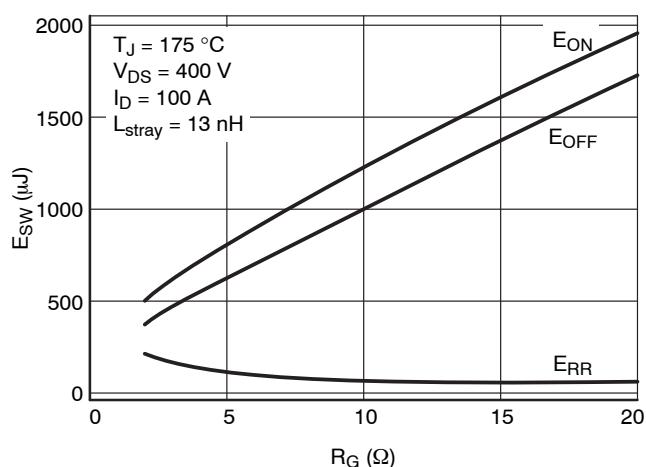


Figure 18.  $E_{SW}$  vs.  $R_G$

## TYPICAL CHARACTERISTICS

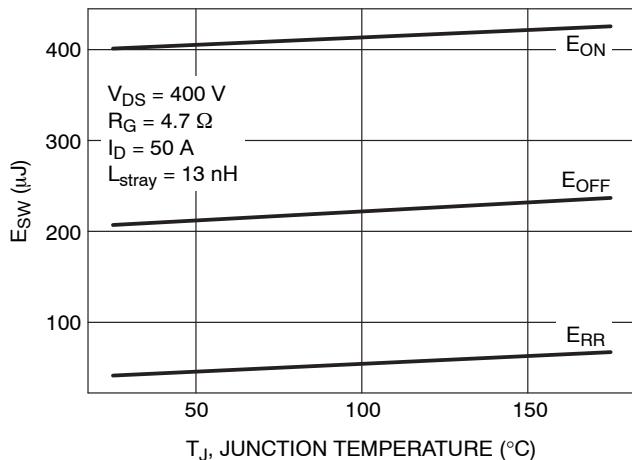
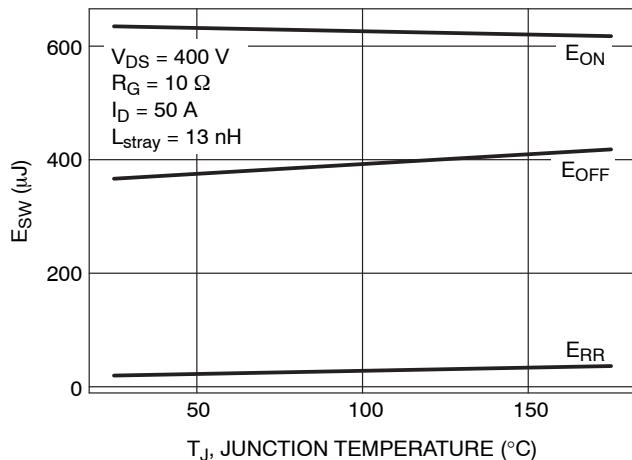
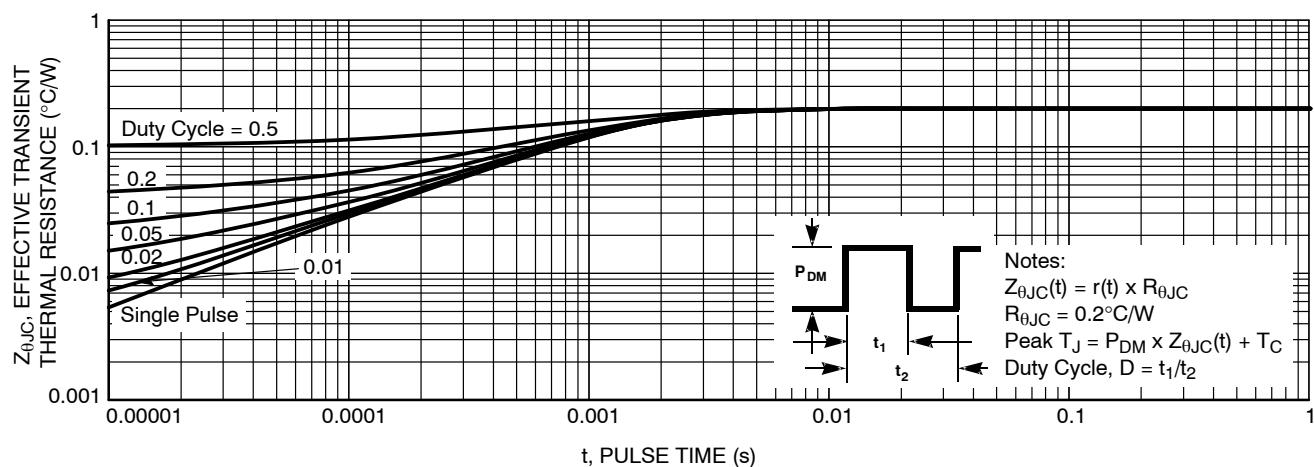
Figure 19.  $E_{SW}$  vs.  $T_J$ Figure 20.  $E_{SW}$  vs.  $T_J$ 

Figure 21. Junction-to-Case Transient Thermal Response Curve

## REVISION HISTORY

Revision	Description of Changes	Date
0	Initial data sheet release	9/29/2025

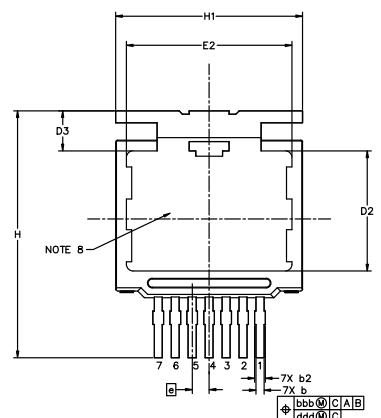
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

## PACKAGE DIMENSIONS

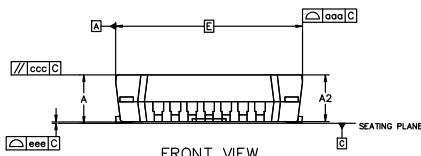
T2PAK-7 11.80x14.00x3.50, 1.27P  
CASE 763AC  
ISSUE A

## NOTES:

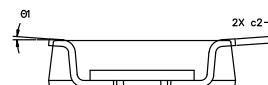
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b, b2, b3 AND c TO BE MEASURED ON FLAT SECTION OF THE LEAD BETWEEN 0.13 AND 0.25mm FROM LEAD TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO THE TERMINALS AND EXPOSED PAD.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
8. ALLOWABLE ENCROACHED FLASH ON HEAT SINK AREA MAXIMUM OF 0.05mm.
9. EJECTOR PINS Ø12.5mm REF.



TOP VIEW



FRONT VIEW



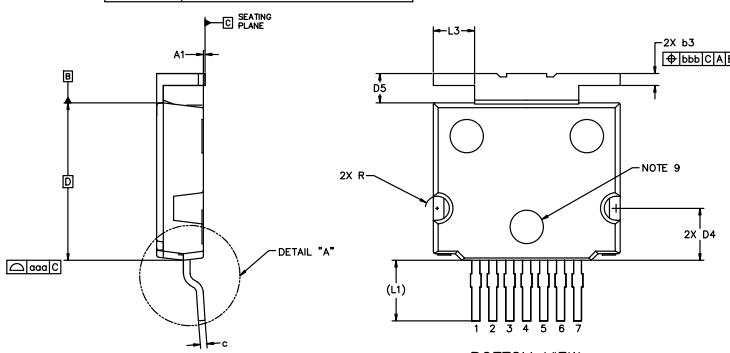
END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	3.53	3.63	3.73
A1	0.07	0.13	0.18
A2	3.40	3.50	3.60
b	0.50	0.60	0.70
b2	0.50	0.75	1.00
b3	0.80	0.90	1.00
c	0.40	0.50	0.60
c2	0.40	0.50	0.60
D	11.80 BSC		
D2	8.90	9.00	9.10
D3	3.00	3.10	3.20
D4	3.80	3.90	4.00
D5	2.10	2.20	2.30
E	14.00 BSC		
E2	12.30	12.40	12.50
e	1.27 BSC		

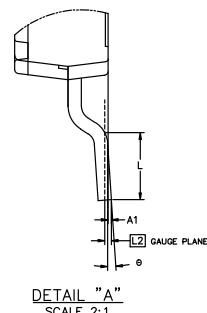
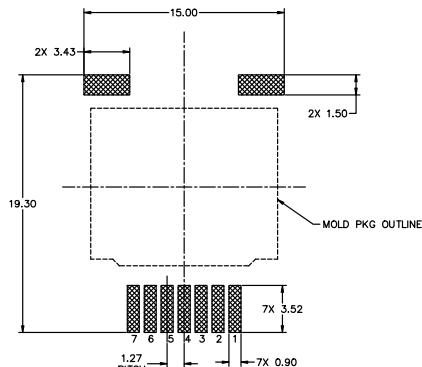
MILLIMETERS			
DIM	MIN	NOM	MAX
H	18.00	18.50	19.00
H1	13.80	14.00	14.20
L	2.42	2.52	2.62
L1	4.53 REF		
L2	0.25 BSC		
L3	3.00	3.10	3.20
R	0.80	---	1.00
θ	0°	---	8°
θ1	0°	---	8°

## TOLERANCE FORM AND POSITION

aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.05



SIDE VIEW

DETAIL "A"  
SCALE 2:1

BOTTOM VIEW



MOLD PKG OUTLINE

**RECOMMENDED MOUNTING FOOTPRINT**  
\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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