

# MOSFET – Power, Single N-Channel

**60 V, 2.0 mΩ, 185 A**

## NVMYS2D2N06CL

### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- LFAK4 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Value	Unit	
$V_{DSS}$	Drain-to-Source Voltage		60	V	
$V_{GS}$	Gate-to-Source Voltage		$\pm 20$	V	
$I_D$	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	$T_C = 25\text{ }^\circ\text{C}$	185	A
			$T_C = 100\text{ }^\circ\text{C}$	131	
$P_D$	Power Dissipation $R_{\theta JC}$ (Notes 1, 2)		$T_C = 25\text{ }^\circ\text{C}$	134	W
			$T_C = 100\text{ }^\circ\text{C}$	67	
$I_D$	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25\text{ }^\circ\text{C}$	31	A
			$T_A = 100\text{ }^\circ\text{C}$	22	
$P_D$	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		$T_A = 25\text{ }^\circ\text{C}$	3.9	W
			$T_A = 100\text{ }^\circ\text{C}$	1.9	
$I_{DM}$	Pulsed Drain Current	$T_A = 25\text{ }^\circ\text{C}, t_p = 10\text{ }\mu\text{s}$	900	A	
$T_J, T_{stg}$	Operating Junction and Storage Temperature		-55 to +175	$^\circ\text{C}$	
$I_S$	Source Current (Body Diode)		112	A	
$E_{AS}$	Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25\text{ }^\circ\text{C}, I_{L(pk)} = 11.9\text{ A}$ )		941	mJ	
$T_L$	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

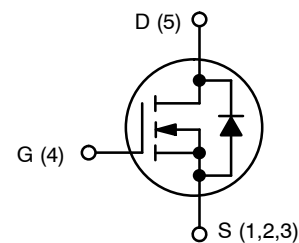
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case - Steady State	1.12	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient - Steady State (Note 2)	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on) MAX}$	$I_D MAX$
60 V	2.0 mΩ @ 10 V	185 A
	2.7 mΩ @ 4.5 V	

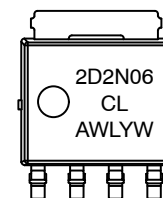


**LFAK4  
CASE 760AB**



**N-CHANNEL MOSFET**

### MARKING DIAGRAM



- 2D6N06CL = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- W = Work Week

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

# NVMYS2D2N06CL

## ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	
<b>OFF CHARACTERISTICS</b>							
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60	-	-	V	
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient		-	26	-	mV/ $^\circ\text{C}$	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25\text{ }^\circ\text{C}$	-	-	10	$\mu\text{A}$
			$T_J = 125\text{ }^\circ\text{C}$	-	-	100	
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$	-	-	100	nA	

## ON CHARACTERISTICS (Note 4)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 180\text{ }\mu\text{A}$	1.2	-	2.0	V	
$V_{GS(TH)}/T_J$	Negative Threshold Temperature Coefficient		-	-5.3	-	mV/ $^\circ\text{C}$	
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}$	$I_D = 50\text{ A}$	-	1.6	1.9	m $\Omega$
		$V_{GS} = 4.5\text{ V}$	$I_D = 50\text{ A}$	-	2.1	2.6	
$g_{FS}$	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 50\text{ A}$	-	135	-	S	

## CHARGES, CAPACITANCES & GATE RESISTANCE

$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$	-	4850	-	pF
$C_{OSS}$	Output Capacitance		-	2450	-	
$C_{RSS}$	Reverse Transfer Capacitance		-	25	-	
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}; I_D = 50\text{ A}$	-	31	-	nC
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}; I_D = 50\text{ A}$	-	69	-	
$Q_{G(TH)}$	Threshold Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}; I_D = 50\text{ A}$	-	6.3	-	
$Q_{GS}$	Gate-to-Source Charge		-	11.5	-	
$Q_{GD}$	Gate-to-Drain Charge		-	7.6	-	
$V_{GP}$	Plateau Voltage		-	2.7	-	V

## SWITCHING CHARACTERISTICS (Note 5)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 50\text{ A}, R_G = 2.5\text{ }\Omega$	-	13	-	ns
$t_r$	Rise Time		-	20	-	
$t_{d(OFF)}$	Turn-Off Delay Time		-	53	-	
$t_f$	Fall Time		-	9.4	-	

## DRAIN-SOURCE DIODE CHARACTERISTICS

$V_{SD}$	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25\text{ }^\circ\text{C}$	-	0.8	1.2	V
			$T_J = 125\text{ }^\circ\text{C}$	-	0.7	-	
$t_{RR}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, dI_S/dt = 20\text{ A}/\mu\text{s}, I_S = 50\text{ A}$	-	64	-	ns	
$t_a$	Charge Time		-	40	-		
$t_b$	Discharge Time		-	24	-		
$Q_{RR}$	Reverse Recovery Charge		-	84	-	nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

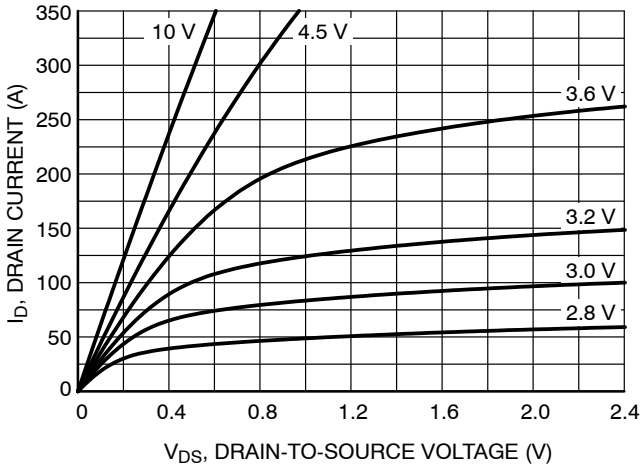


Figure 1. On-Region Characteristics

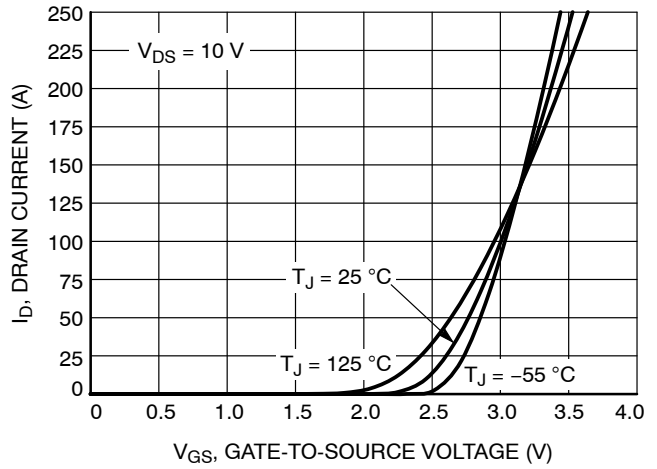


Figure 2. Transfer Characteristics

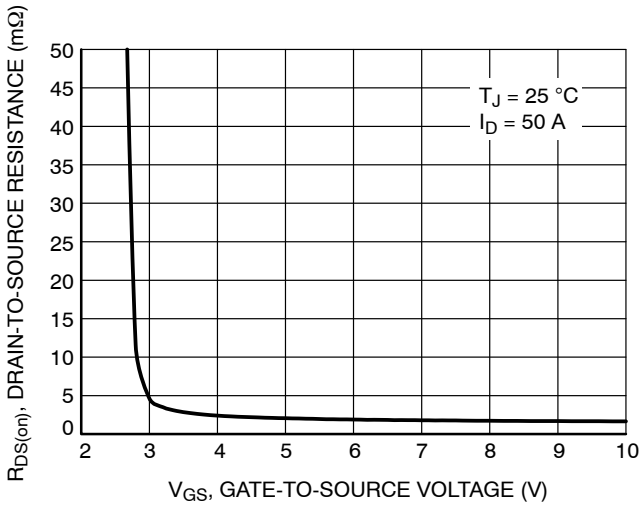


Figure 3. On-Resistance vs. Gate-to-Source Voltage

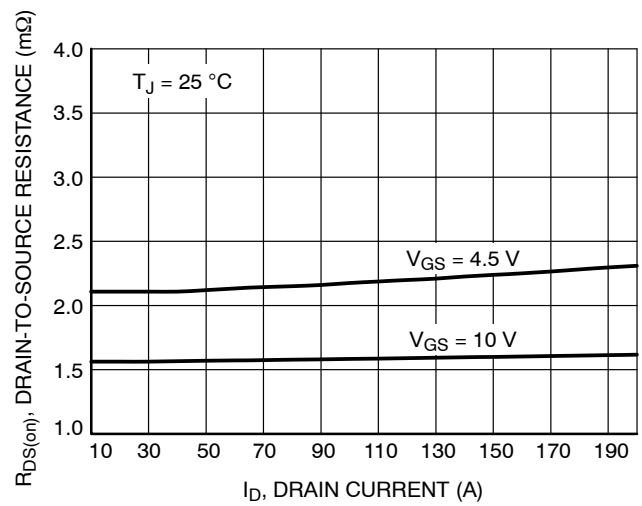


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

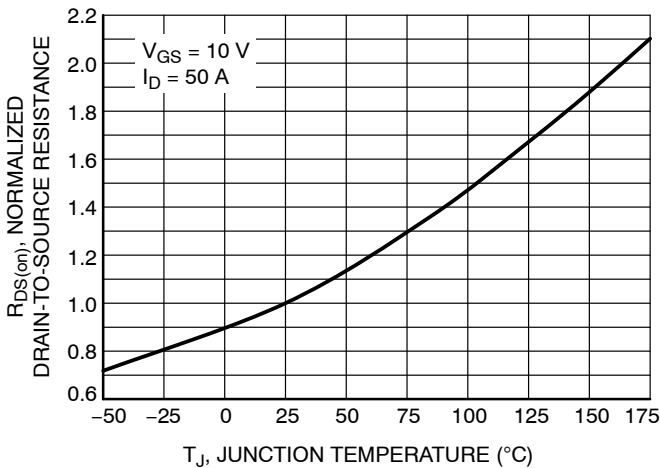


Figure 5. On-Resistance Variation with Temperature

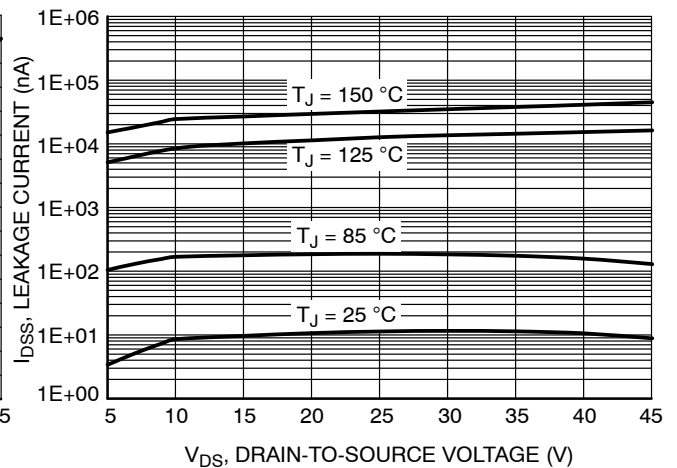


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

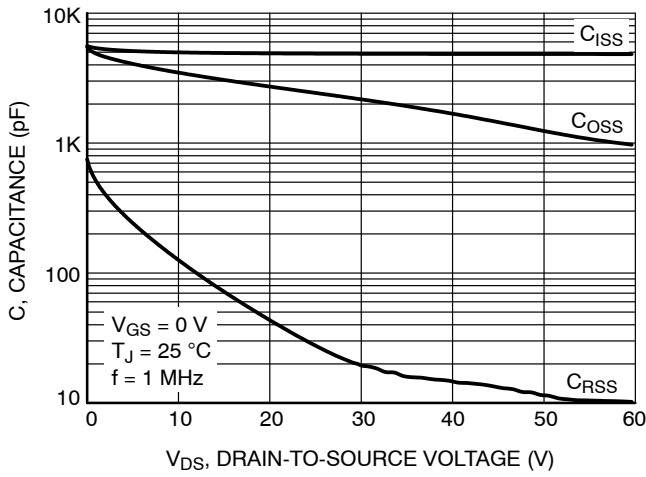


Figure 7. Capacitance Variation

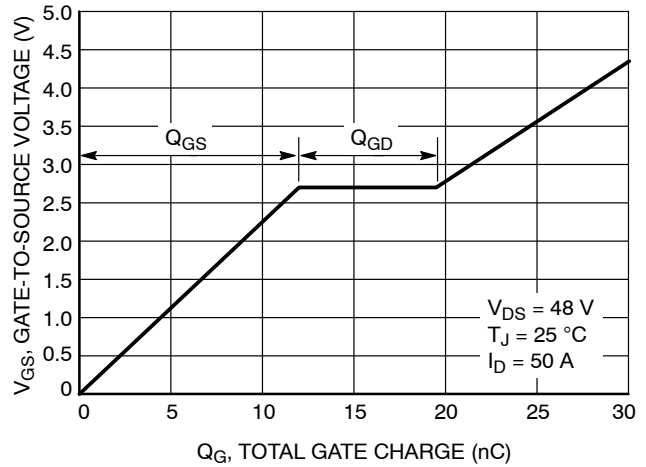


Figure 8. Gate-to-Source Voltage vs. Total Charge

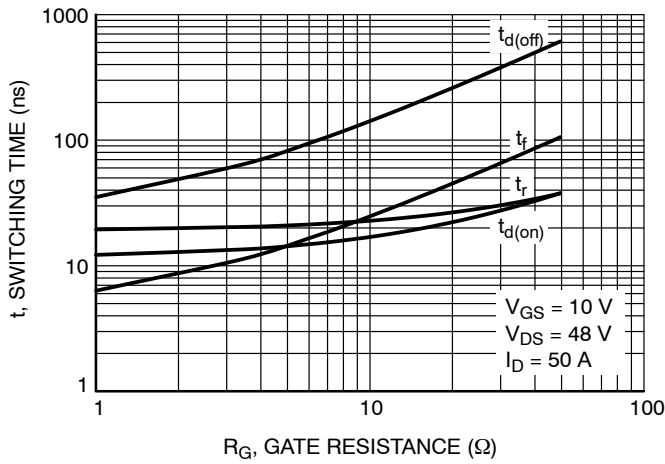


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

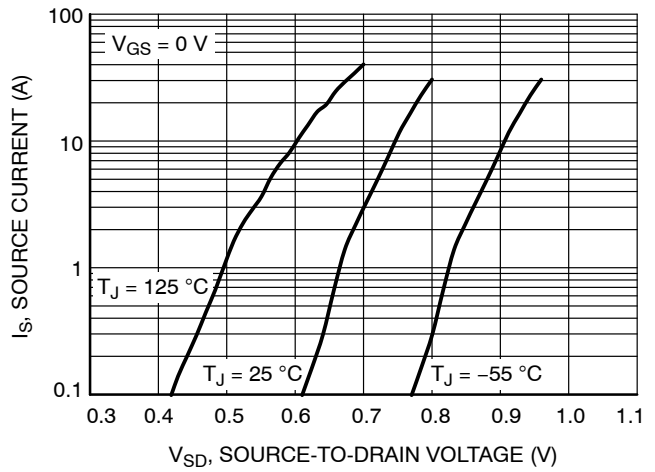


Figure 10. Diode Forward Voltage vs. Current

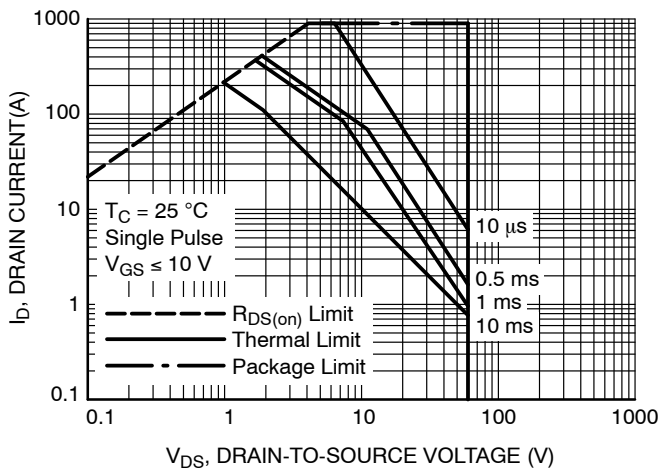


Figure 11. Maximum Rated Forward Biased Safe Operating Area

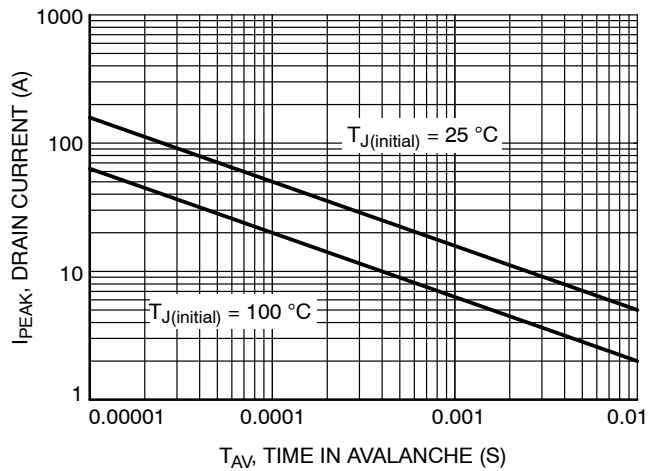


Figure 12. Maximum Drain Current vs. Time in Avalanche

# NVMYS2D2N06CL

## TYPICAL CHARACTERISTICS (continued)

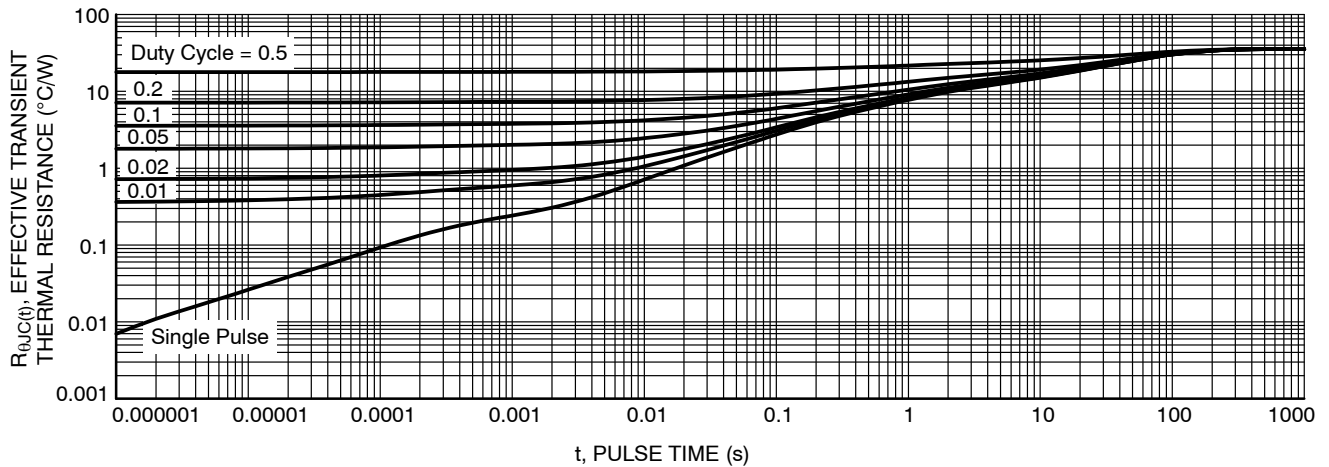


Figure 13. Thermal Response

### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NVMYS2D2N06CLTWG	2D2N06CL	LFP4K4 (Pb-Free)	3,000 / Tape & Reel

<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

NVMYS2D2N06CL

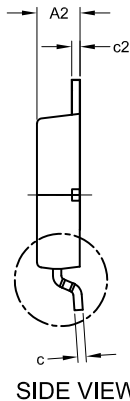
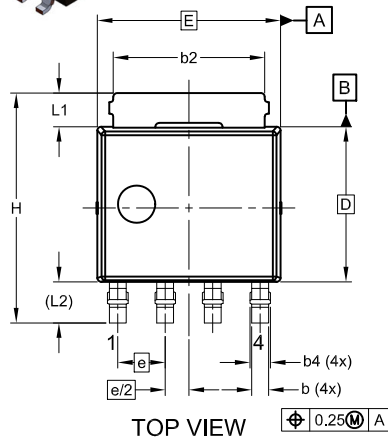
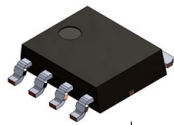
REVISION HISTORY

Revision	Description of Changes	Date
1	Rebranded the Data Sheet to <b>onsemi</b> .	11/19/2025

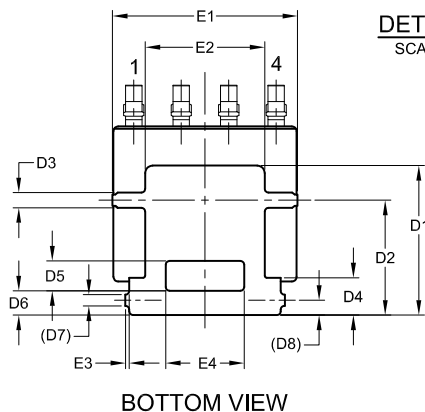
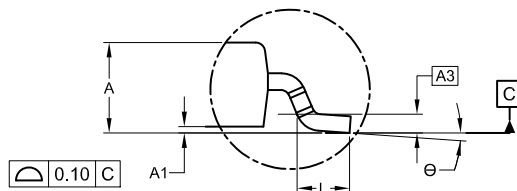
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

LFLPAK4 4.90x4.15x1.15MM, 1.27P  
CASE 760AB  
ISSUE D

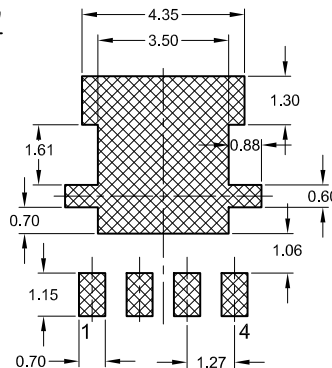
DATE 22 MAY 2024



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
  4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

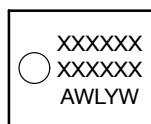


DETAIL 'A'  
SCALE: 2:1



MILLIMETER			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 BSC		
b	0.40	0.45	0.50
b2	3.80	4.10	4.40
b4	0.45	0.55	0.65
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.15 BSC		
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
D4	0.90	1.00	1.10
D5	0.70	0.80	0.90
D6	0.55	0.65	0.75
D7	0.31 REF		
D8	0.40 REF		
E	4.90 BSC		
E1	4.85	4.95	5.05
E2	3.10	3.20	3.30
E3	0.00	0.10	0.20
E4	2.00	2.10	2.20
e	1.27 BSC		
e/2	0.635 BSC		
e1	0.40 REF		
H	6.00	6.15	6.30
L	0.50	0.70	0.90
L1	0.80	0.90	1.00
L2	1.10 REF		
Θ	0°	4°	8°

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- W = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

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DESCRIPTION:	LFLPAK4 4.90x4.15x1.15MM, 1.27P	PAGE 1 OF 1

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