

# MOSFET – Power, Single N-Channel

**60 V, 0.68 mΩ, 477 A**

## NVMTS0D7N06CL

### Features

- Small Footprint (8x8 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- Power 88 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- Wettable Flank Option for Enhanced Optical Inspection
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Value	Unit	
$V_{DSS}$	Drain-to-Source Voltage		60	V	
$V_{GS}$	Gate-to-Source Voltage		$\pm 20$	V	
$I_D$	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25\text{ }^\circ\text{C}$	477	A
			$T_C = 100\text{ }^\circ\text{C}$	337.6	
$P_D$	Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25\text{ }^\circ\text{C}$	294.6	W
			$T_C = 100\text{ }^\circ\text{C}$	147.3	
$I_D$	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25\text{ }^\circ\text{C}$	62.2	A
			$T_A = 100\text{ }^\circ\text{C}$	44.0	
$P_D$	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25\text{ }^\circ\text{C}$	5.0	W
			$T_A = 100\text{ }^\circ\text{C}$	2.5	
$I_{DM}$	Pulsed Drain Current	$T_A = 25\text{ }^\circ\text{C}, t_p = 10\text{ }\mu\text{s}$	900	A	
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range		-55 to +175	$^\circ\text{C}$	
$I_S$	Source Current (Body Diode)		245.5	A	
$E_{AS}$	Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 40\text{ A}$ )		1754	mJ	
$T_L$	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		260	$^\circ\text{C}$	

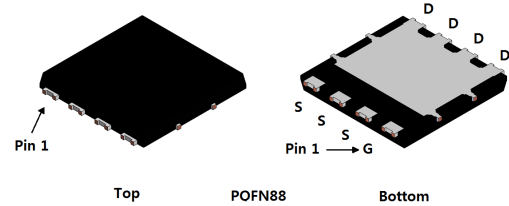
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

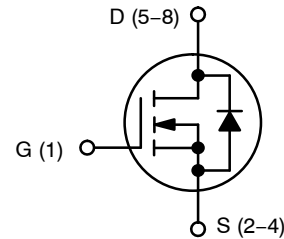
Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	0.5	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	30	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
60 V	0.68 mΩ @ 10 V	477 A
	0.90 mΩ @ 4.5 V	

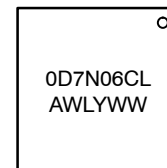


DFNW8  
CASE 507AP



N-CHANNEL MOSFET

### MARKING DIAGRAM



- A = Assembly Location
- WL = Wafer Lot Code
- Y = Year Code
- WW = Work Week Code

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVMTS0D7N06CL

## ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	
<b>OFF CHARACTERISTICS</b>							
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60	-	-	V	
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , ref to $25\text{ }^\circ\text{C}$	-	16.8	-	mV/ $^\circ\text{C}$	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25\text{ }^\circ\text{C}$	-	-	10	$\mu\text{A}$
			$T_J = 125\text{ }^\circ\text{C}$	-	-	250	
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$	-	-	100	nA	

## ON CHARACTERISTICS (Note 4)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.0	-	2.5	V	
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , ref to $25\text{ }^\circ\text{C}$	-	-5.63	-	mV/ $^\circ\text{C}$	
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}$	$I_D = 50\text{ A}$	-	0.52	0.68	m $\Omega$
		$V_{GS} = 4.5\text{ V}$	$I_D = 50\text{ A}$	-	0.69	0.90	
$g_{FS}$	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 50\text{ A}$	-	310	-	S	

## CHARGES, CAPACITANCES & GATE RESISTANCE

$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$	-	1620	-	pF	
$C_{OSS}$	Output Capacitance		-	8490	-		
$C_{RSS}$	Reverse Transfer Capacitance		-	270	-		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$	-	103	-	nC	
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$	-	225	-		
$Q_{G(TH)}$	Threshold Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$	-	21.6	-		
$Q_{GS}$	Gate-to-Source Charge		-	36.5	-		
$Q_{GD}$	Gate-to-Drain Charge		-	20.7	-		
$V_{GP}$	Plateau Voltage		-	2.46	-		V

## SWITCHING CHARACTERISTICS (Note 5)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 30\text{ V}, I_D = 50\text{ A}, R_G = 2.5\text{ }\Omega$	-	35.3	-	ns
$t_r$	Rise Time		-	26.3	-	
$t_{d(OFF)}$	Turn-Off Delay Time		-	263	-	
$t_f$	Fall Time		-	60.7	-	

## DRAIN-SOURCE DIODE CHARACTERISTICS

$V_{SD}$	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25\text{ }^\circ\text{C}$	-	0.67	1.2	V
			$T_J = 125\text{ }^\circ\text{C}$	-	0.59	-	
$t_{RR}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$	-	115	-	ns	
$t_a$	Charge Time		-	70	-		
$t_b$	Discharge Time		-	45	-		
$Q_{RR}$	Reverse Recovery Charge		-	307	-		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

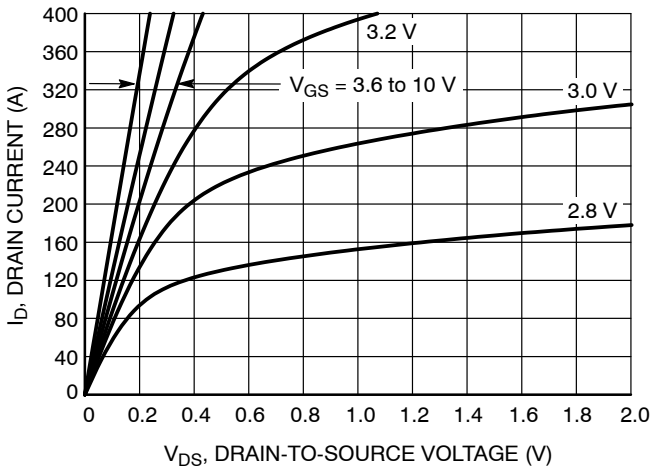


Figure 1. On-Region Characteristics

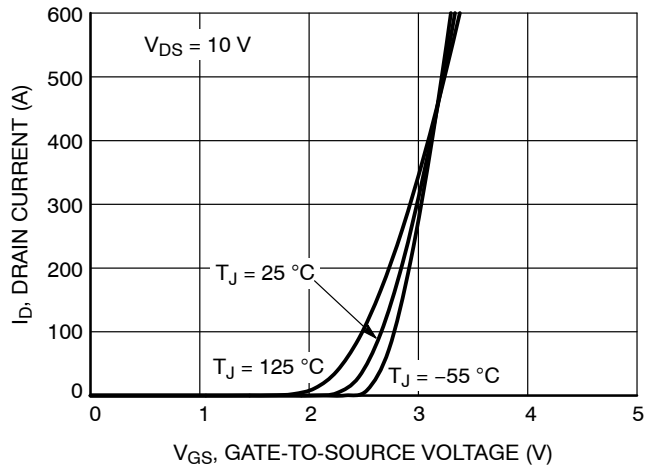


Figure 2. Transfer Characteristics

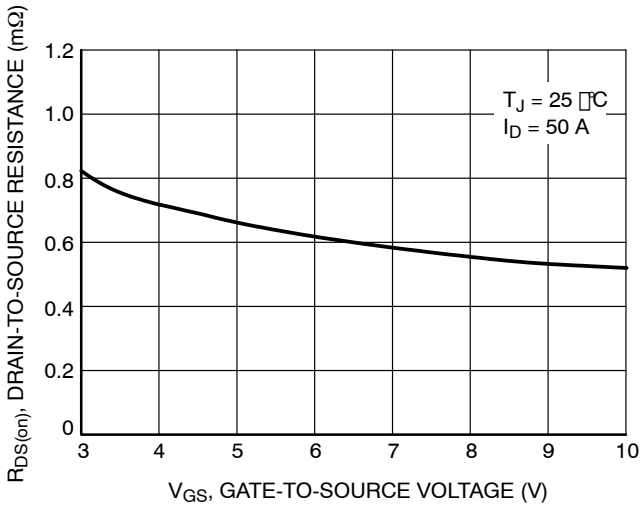


Figure 3. On-Resistance vs. Gate-to-Source Voltage

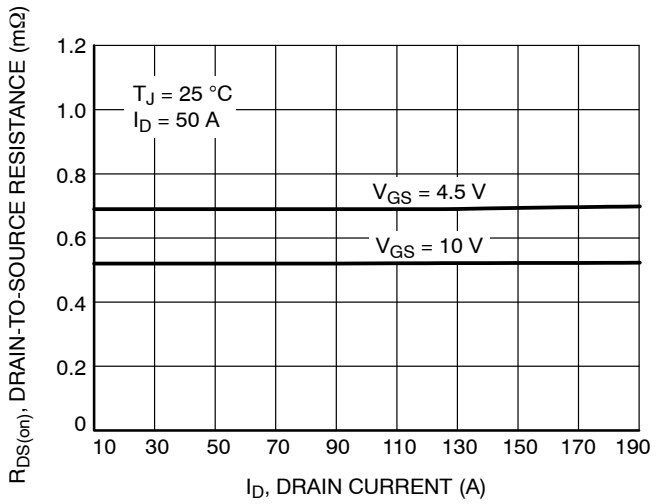


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

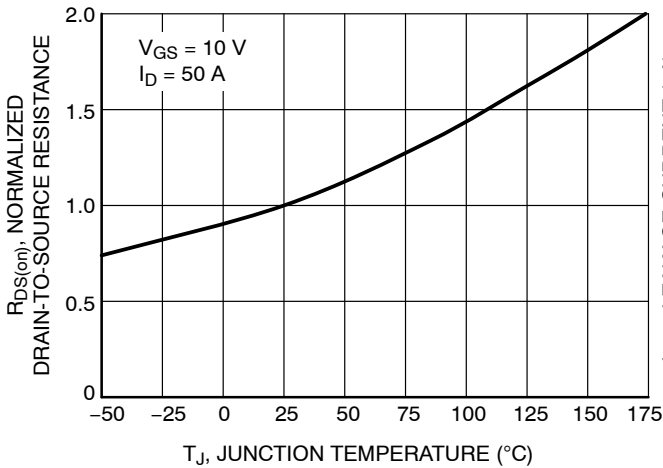


Figure 5. On-Resistance Variation with Temperature

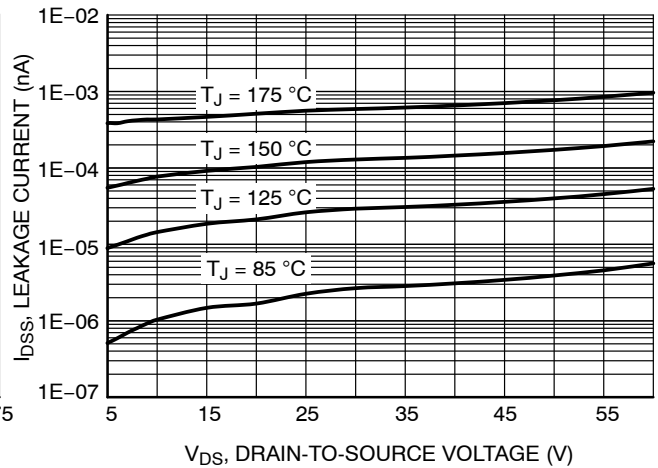


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

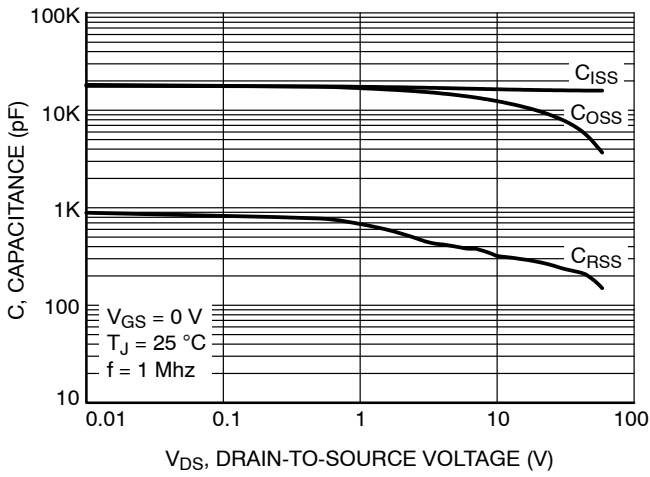


Figure 7. Capacitance Variation

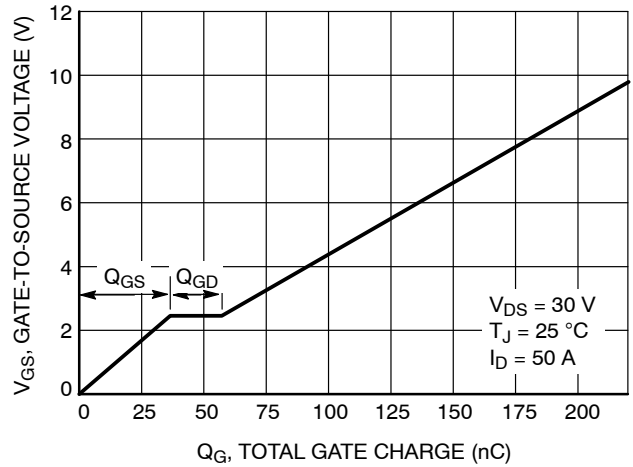


Figure 8. Gate-to-Source Voltage vs. Total Charge

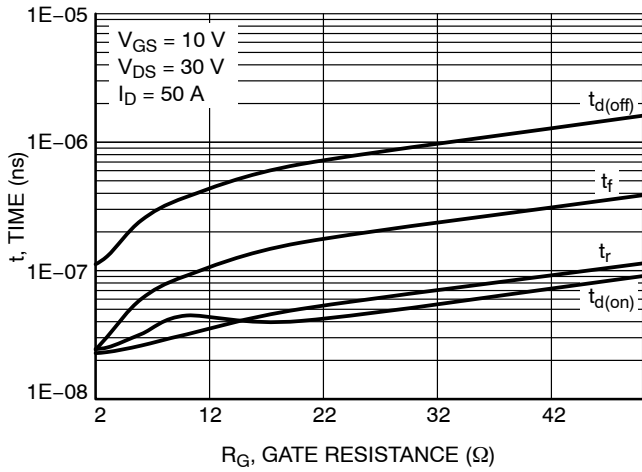


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

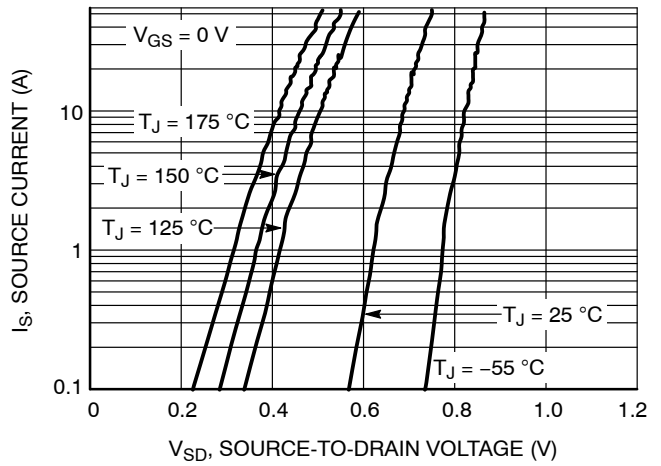


Figure 10. Diode Forward Voltage vs. Current

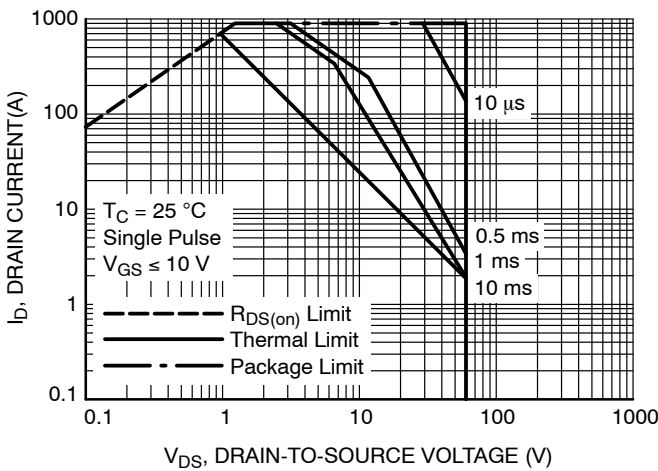


Figure 11. Maximum Rated Forward Biased Safe Operating Area

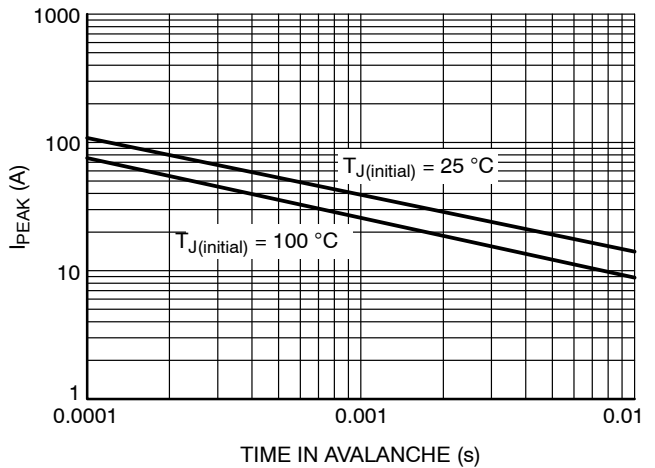
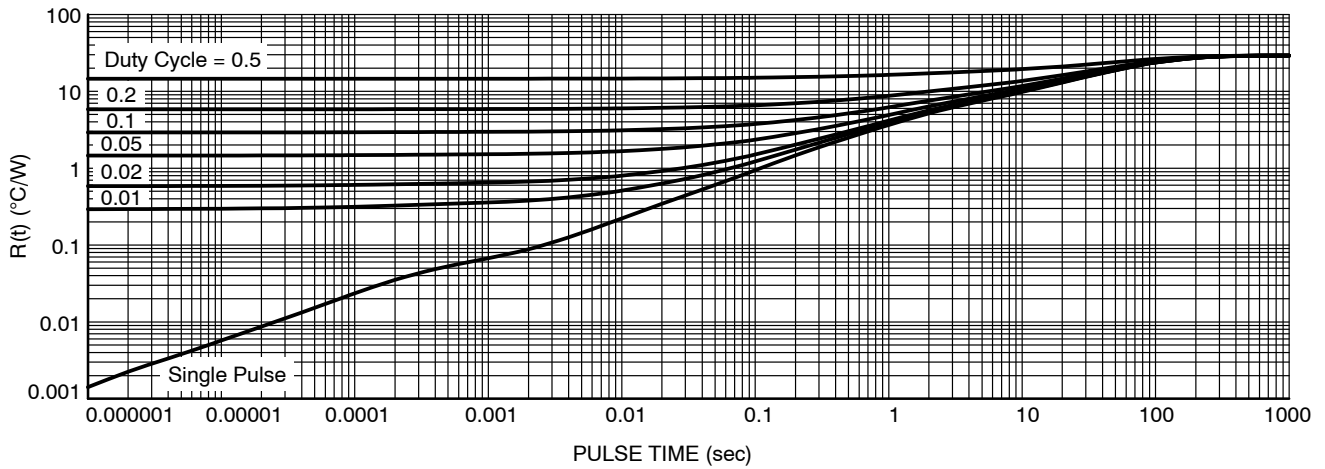


Figure 12. Maximum Drain Current vs. Time in Avalanche

# NVMTS0D7N06CL

## TYPICAL CHARACTERISTICS (continued)



**Figure 13. Thermal Characteristics**

### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMTS0D7N06CLTXG	0D7N06CL	DFNW8 (Pb-Free)	3,000 / Tape & Reel

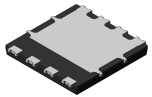
† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# NVMTS0D7N06CL

## REVISION HISTORY

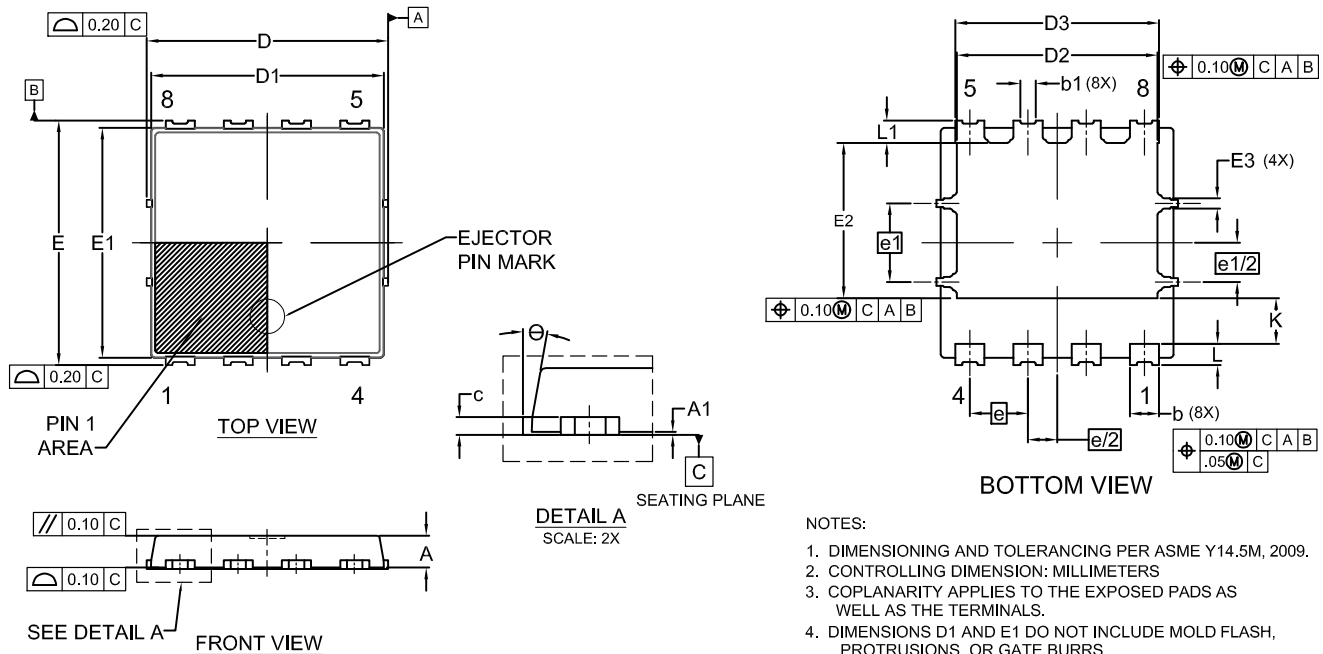
Revision	Description of Changes	Date
4	Rebranded the Data Sheet to <b>onsemi</b> format.	01/23/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

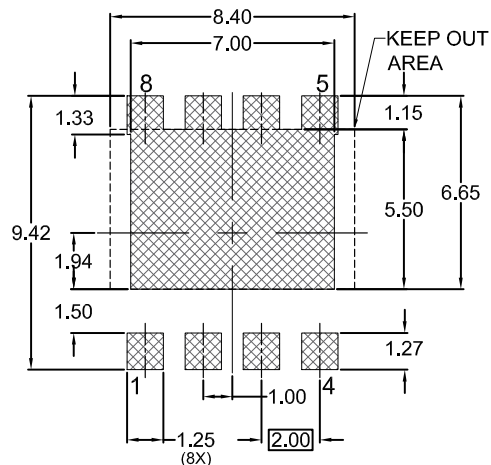


TDFNW8 8.30x8.40x1.10, 2.00P  
CASE 507AP  
ISSUE E

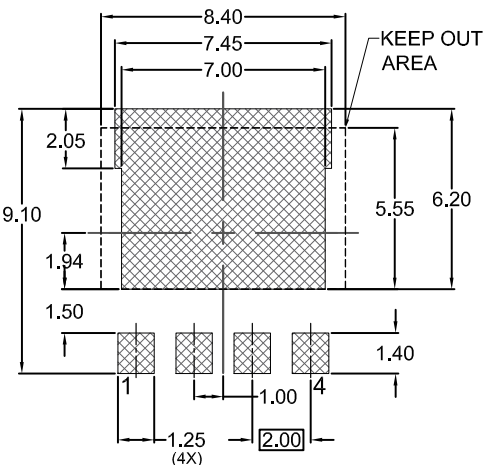
DATE 08 MAY 2024



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
  2. CONTROLLING DIMENSION: MILLIMETERS
  3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
  4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
  5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



RECOMMENDED LAND PATTERN\*



UNIVERSAL LAND PATTERN\*

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	---	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
θ	0°	---	12°

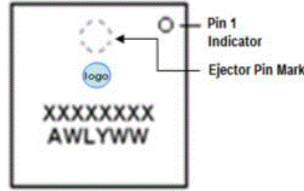
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**TDFNW8 8.30x8.40x1.10, 2.00P**  
**CASE 507AP**  
**ISSUE E**

DATE 08 MAY 2024

**GENERIC  
MARKING DIAGRAM\***



XXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot Code  
Y = Year Code  
WW = Work Week Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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