

# MOSFET – Power, Single N-Channel

60 V, 0.81 mΩ, 398.2 A

## NVMTS001N06CL

### Features

- Small Footprint (8x8 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- Power 88 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- Wettable Flank Plated for Enhanced Optical Inspection
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	60	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25\text{ }^\circ\text{C}$	398.2	A
		$T_C = 100\text{ }^\circ\text{C}$	281.6	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25\text{ }^\circ\text{C}$	244.0	W
		$T_C = 100\text{ }^\circ\text{C}$	122.0	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25\text{ }^\circ\text{C}$	56.9	A
		$T_A = 100\text{ }^\circ\text{C}$	40.2	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25\text{ }^\circ\text{C}$	5.0	W
		$T_A = 100\text{ }^\circ\text{C}$	2.5	
Pulsed Drain Current	$T_A = 25\text{ }^\circ\text{C}, t_p = 10\text{ }\mu\text{s}$	$I_{DM}$	900	A
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	203.4	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 30\text{ A}$ )	$E_{AS}$	887	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

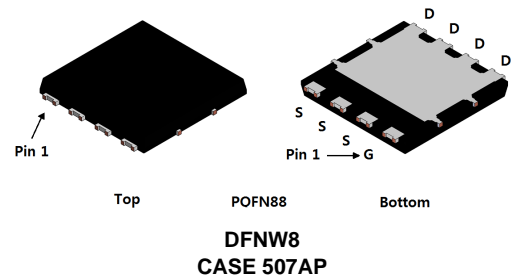
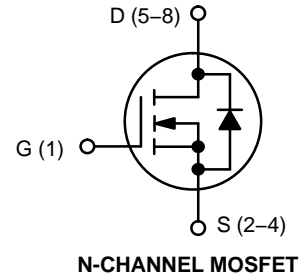
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

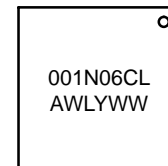
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	0.614	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	30.1	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
60 V	0.81 mΩ @ 10 V	398.2 A
	1.05 mΩ @ 4.5 V	



### MARKING DIAGRAM



- A = Assembly Location
- WL = Wafer Lot Code
- Y = Year Code
- WW = Work Week Code

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVMTS001N06CL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA, ref to 25 °C		25		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 60 V	T <sub>J</sub> = 25 °C		10	μA
			T <sub>J</sub> = 125 °C		250	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.2		2.2	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA, ref to 25 °C		-5.53		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A		0.73	0.81	mΩ
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 50 A		0.94	1.05	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 50 A		275		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 25 V		12300		pF
Output Capacitance	C <sub>OSS</sub>			6225		
Reverse Transfer Capacitance	C <sub>RSS</sub>			130		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 30 V; I <sub>D</sub> = 50 A		165		nC
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 30 V; I <sub>D</sub> = 50 A		74.3		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			15.6		nC
Gate-to-Source Charge	Q <sub>GS</sub>			28.7		
Gate-to-Drain Charge	Q <sub>GD</sub>			14.7		
Plateau Voltage	V <sub>GP</sub>				2.59	

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 30 V, I <sub>D</sub> = 50 A, R <sub>G</sub> = 2.5 Ω		47.2		ns
Rise Time	t <sub>r</sub>			25.2		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			70.7		
Fall Time	t <sub>f</sub>			23.3		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 50 A	T <sub>J</sub> = 25 °C		0.77	1.2	V
			T <sub>J</sub> = 125 °C		0.63		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 50 A			98.9		ns
Charge Time	t <sub>a</sub>				66.8		
Discharge Time	t <sub>b</sub>				32.1		
Reverse Recovery Charge	Q <sub>RR</sub>					229	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

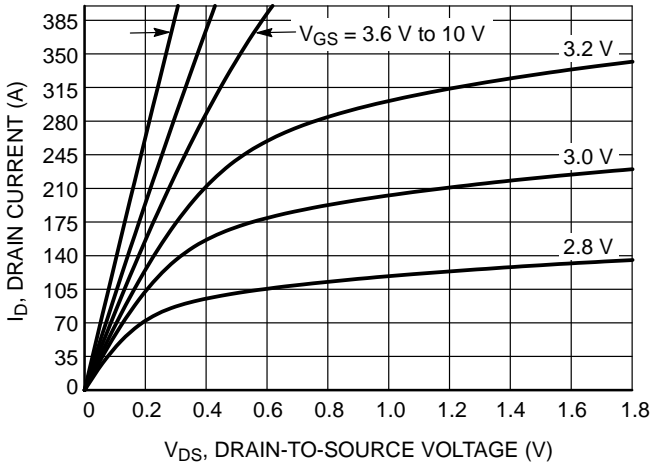


Figure 1. On-Region Characteristics

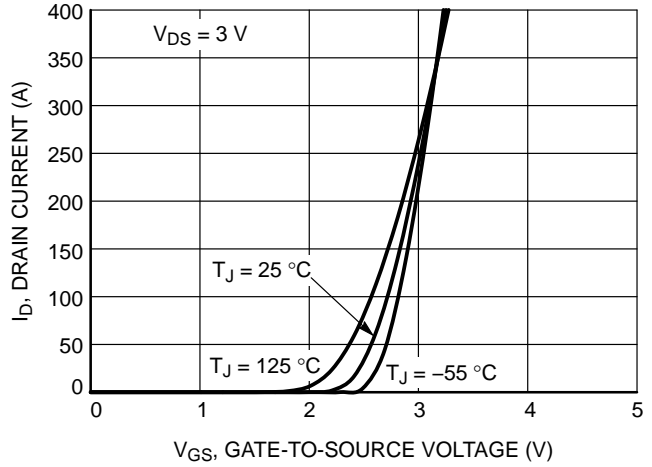


Figure 2. Transfer Characteristics

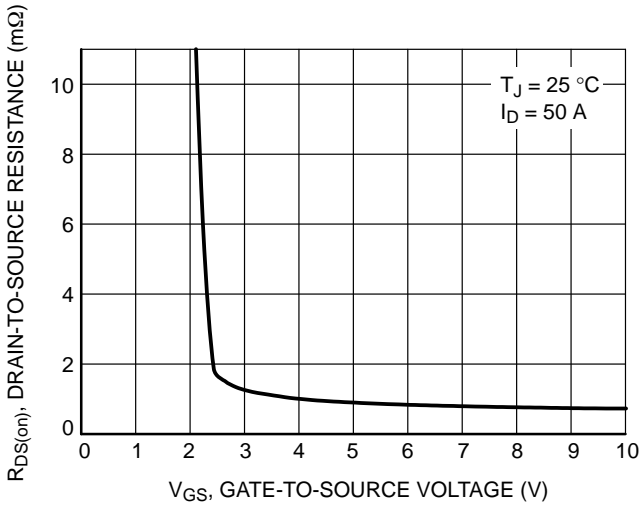


Figure 3. On-Resistance vs. Gate-to-Source Voltage

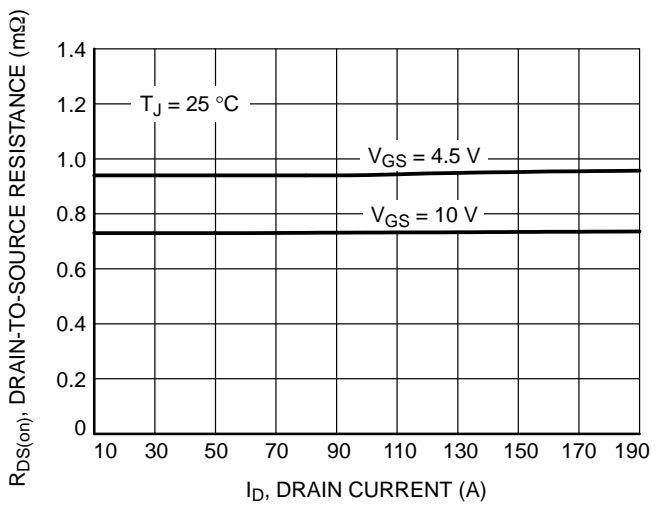


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

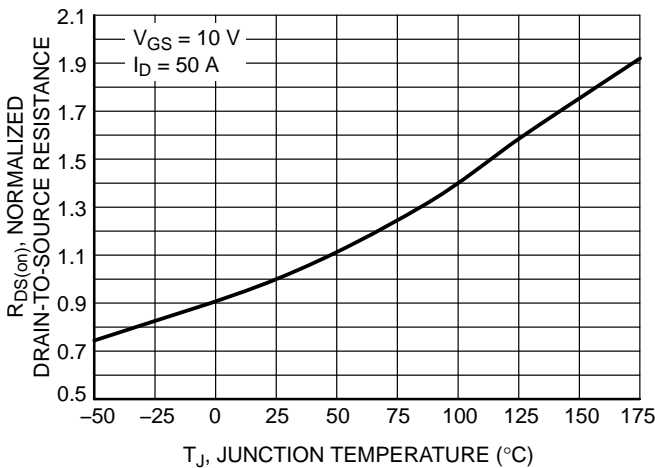


Figure 5. On-Resistance Variation with Temperature

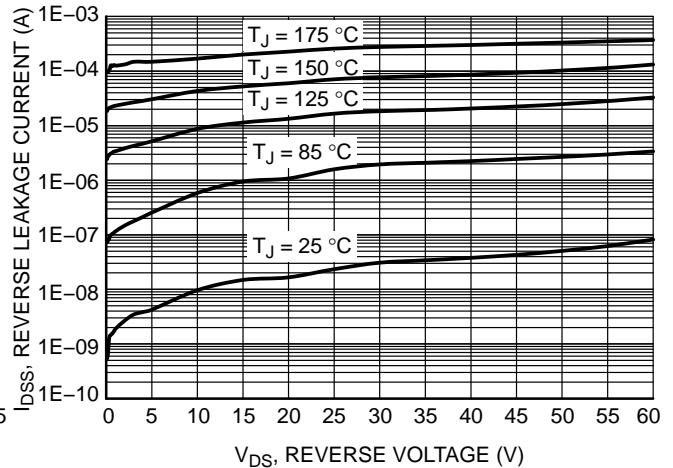


Figure 6. Reverse Leakage Current vs. Voltage

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## TYPICAL CHARACTERISTICS

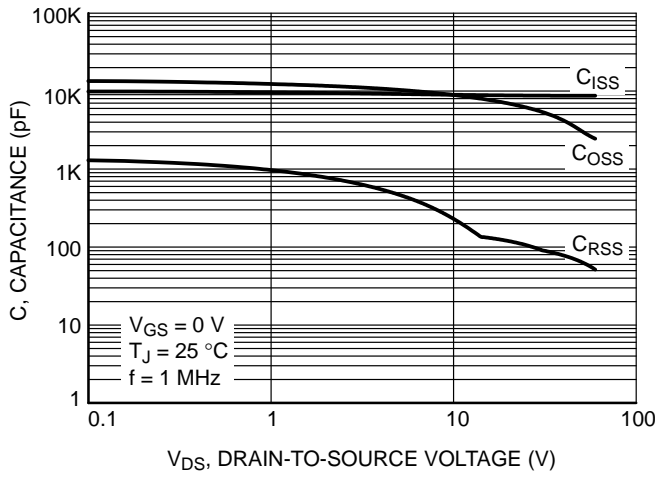


Figure 7. Capacitance Variation

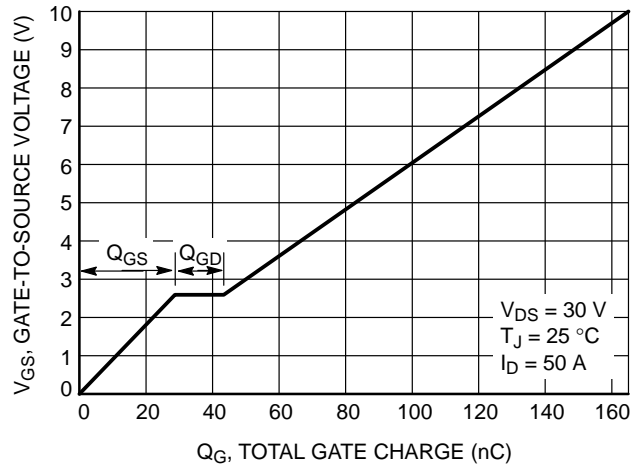


Figure 8. Gate-to-Source Voltage vs. Total Charge

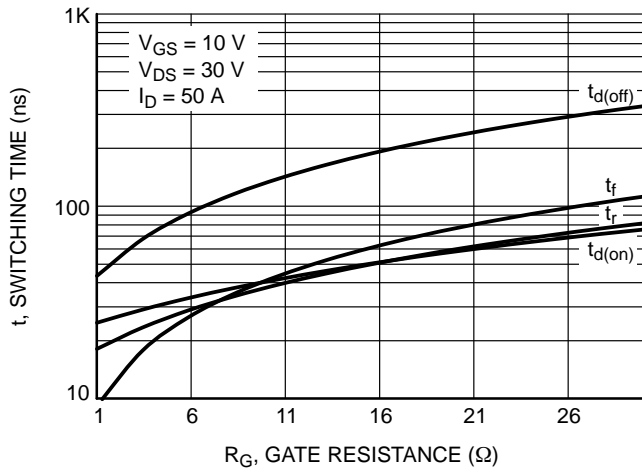


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

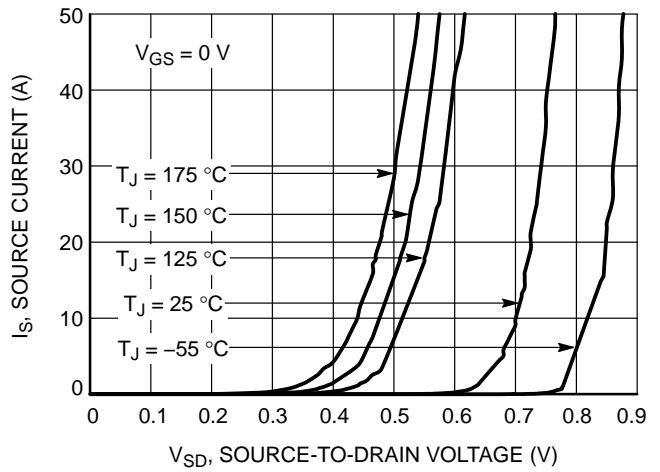


Figure 10. Diode Forward Voltage vs. Current

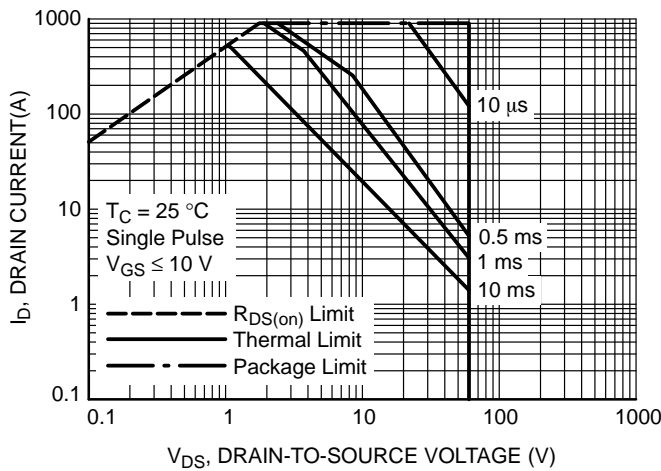


Figure 11. Maximum Rated Forward Biased Safe Operating Area

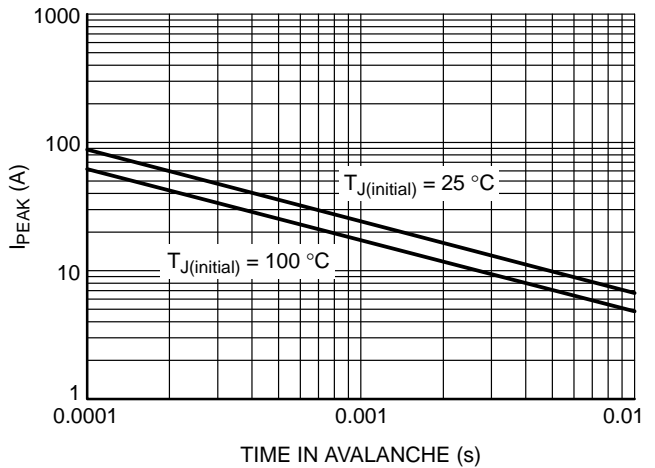


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

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## TYPICAL CHARACTERISTICS

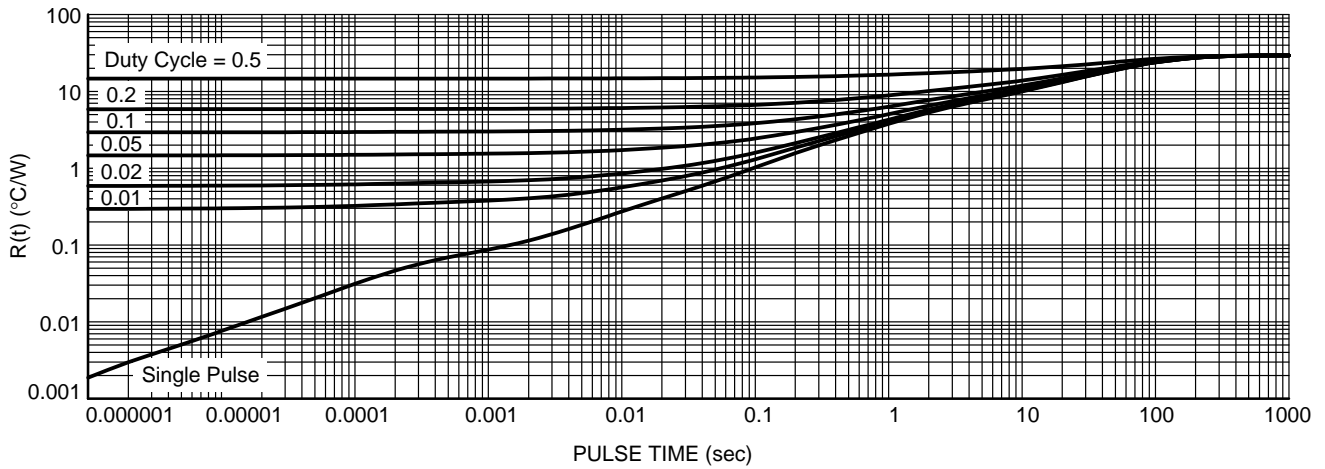


Figure 13. Thermal Characteristics

### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NVMTS001N06CLTXG	001N06CL	DFNW8 (Pb-Free)	3000 / Tape & Reel

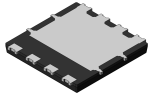
<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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## REVISION HISTORY

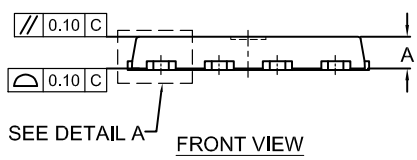
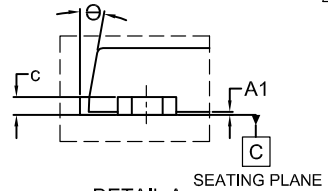
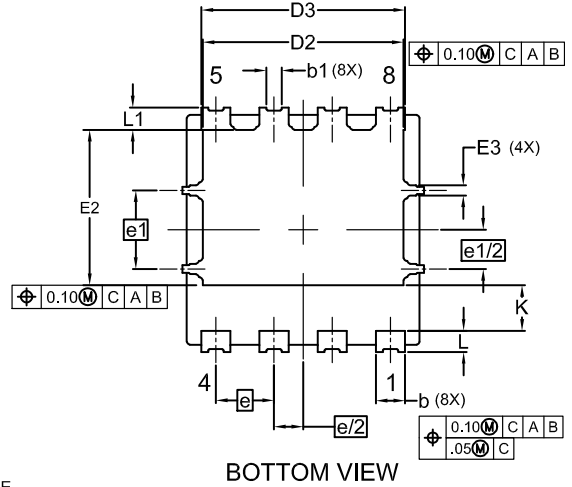
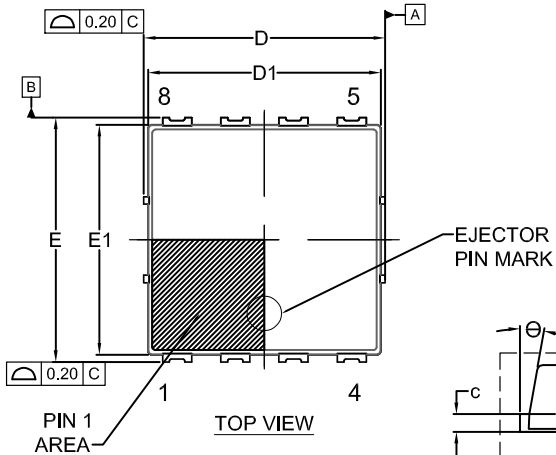
Revision	Description of Changes	Date
3	Rebranded the document to <b>onsemi</b> format.	2/3/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

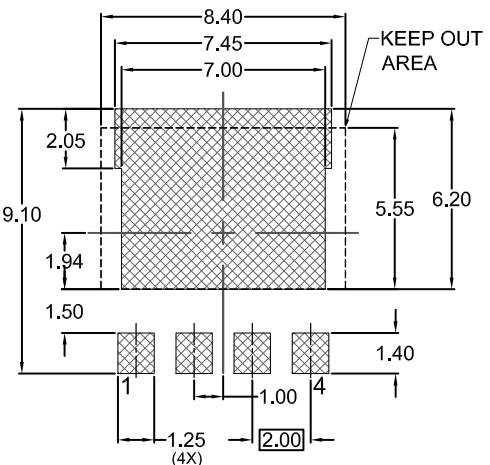
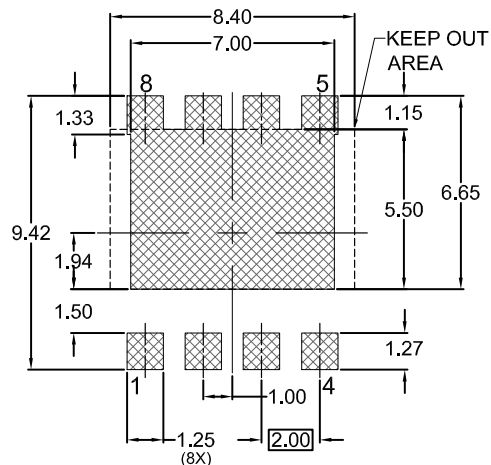


TDFNW8 8.30x8.40x1.10, 2.00P  
CASE 507AP  
ISSUE E

DATE 08 MAY 2024



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
  2. CONTROLLING DIMENSION: MILLIMETERS
  3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
  4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
  5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	---	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	---	12°

RECOMMENDED LAND PATTERN\*  
\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

UNIVERSAL LAND PATTERN\*

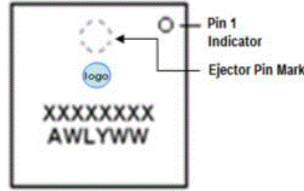
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**CASE 507AP**  
**ISSUE E**

DATE 08 MAY 2024

**GENERIC  
MARKING DIAGRAM\***



XXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot Code  
Y = Year Code  
WW = Work Week Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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