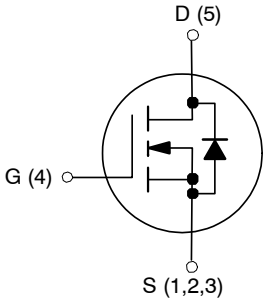
MOSFET - Power, Single N-Channel, STD Gate, SO8FL

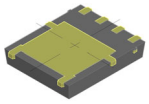
80 V, 4.5 mΩ, 92 A

NVMFWS4D5N08X

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	4.5 mΩ @ 10 V	92 A



N−CHANNEL MOSFET



DFNW5
(SO8FL WF)
CASE 507BA

Features

- Low Q_{RR}, Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Synchronous Rectification (SR) in DC−DC and AC−DC
- Primary Switch in Isolated DC−DC Converter
- Motor Drives
- Automotive 48 V System

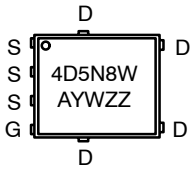
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	80	V
Gate−to−Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	92	A
	T_C = 100°C		65	
Power Dissipation (Note 1)	T_C = 25°C	P_D	82	W
Pulsed Drain Current	T_C = 25°C, t_P = 100 μs	I_{DM}	350	A
Pulsed Source Current (Body Diode)		I_{SM}	350	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)		I_S	126	A
Single Pulse Avalanche Energy (Note 3) (I_{PK} = 35 A)		E_{AS}	61	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using a 1 in^2, 1 oz. Cu pad
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. E_{AS} of 61 mJ is based on started T_J = 25°C, I_{AS} = 35 A, V_{DD} = 64 V, V_{GS} = 10 V, 100% avalanche tested

MARKING DIAGRAM



4D5N8W = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NVMFWS4D5N08XT1G	DFNW5 (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case (Note 5)	$R_{\theta JC}$	1.83	°C/W
Thermal Resistance, Junction−to−Ambient (Notes 4, 5)	$R_{\theta JA}$	39	

4. Surface−mounted on FR4 board using 1 in^2 pad, 1 oz. Cu.
5. $R_{\theta JA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	80			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25°C		31.7		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, T_J = 25°C			1	μA
		V_{DS} = 80 V, T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 19 A		4.0	4.5	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 96 μA	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 96 μA		−7.5		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 19 A		61		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 Mhz		1700		pF
Output Capacitance	C_{OSS}			490		
Reverse Transfer Capacitance	C_{RSS}			7		
Output Charge	Q_{OSS}			35		
Total Gate Charge	$Q_{G(tot)}$	V_{DD} = 40 V, I_D = 19 A, V_{GS} = 10 V		24		nC
Threshold Gate Charge	$Q_{G(th)}$			5		
Gate−to−Source Charge	Q_{GS}			8		
Gate−to−Drain Charge	Q_{GD}			4		
Gate Plateau Voltage	V_{GP}			4.7		V
Gate Resistance	R_G	f = 1 Mhz		1.45		Ω
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(on)}$	Resistive Load V_{GS} = 0/10 V, V_{DD} = 64 V, I_D = 19 A, R_G = 2.5 Ω		18		ns
Rise Time	t_r			7		
Turn−Off Delay Time	$t_{d(off)}$			27		
Fall Time	t_f			5		
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_{SD} = 19 A, T_J = 25°C		0.82	1.2	V
		V_{GS} = 0 V, I_{SD} = 19 A, T_J = 125°C		0.67		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_{SD} = 19 A, dI/dt = 1000 A/μs, V_{DD} = 64 V		20		ns
Charge Time	T_A			10		
Discharge Time	T_B			10		
Reverse Recovery Charge	Q_{RR}			104		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

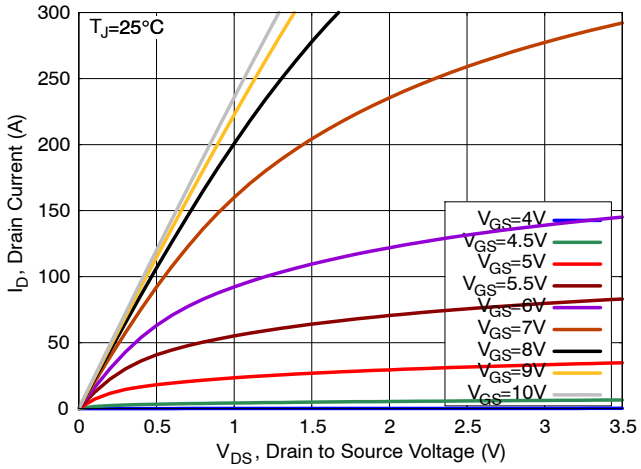


Figure 1. On−Region Characteristics

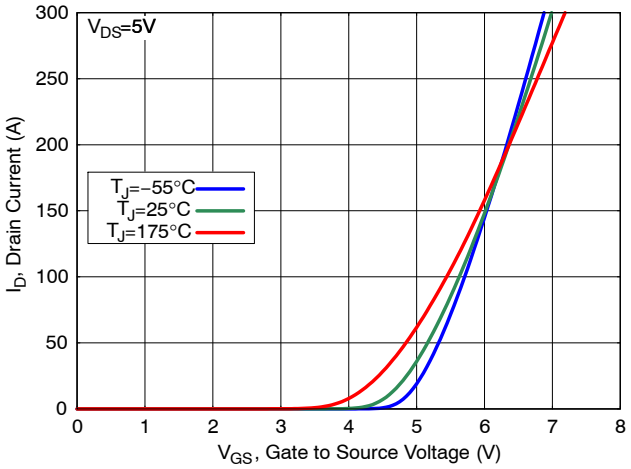


Figure 2. Transfer Characteristics

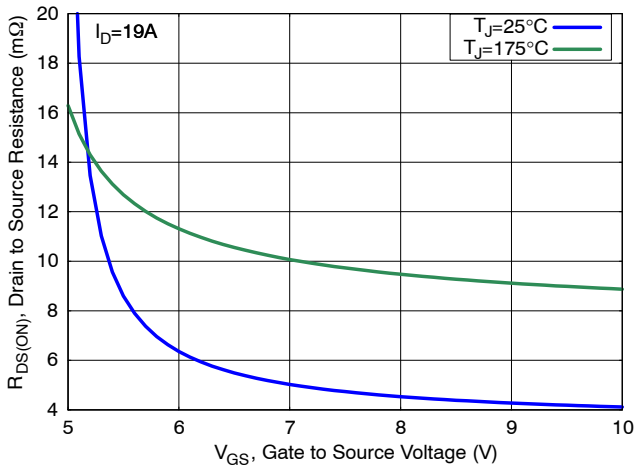


Figure 3. On−Resistance vs. V_{GS}

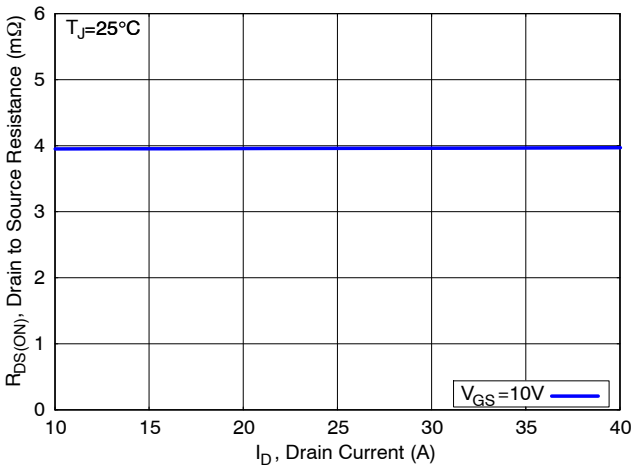


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

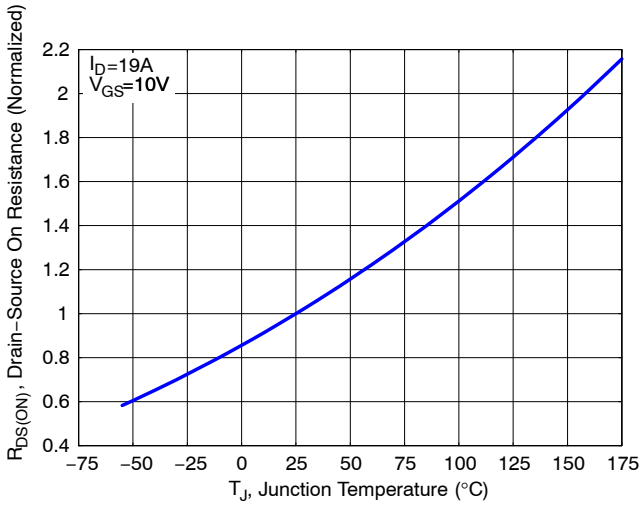


Figure 5. On−Resistance Variation with Temperature

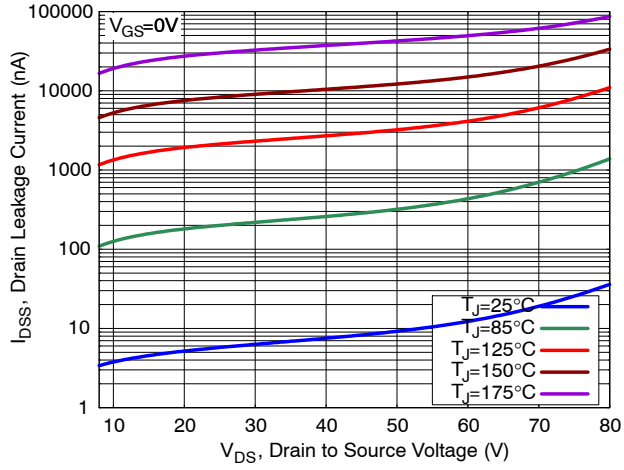


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

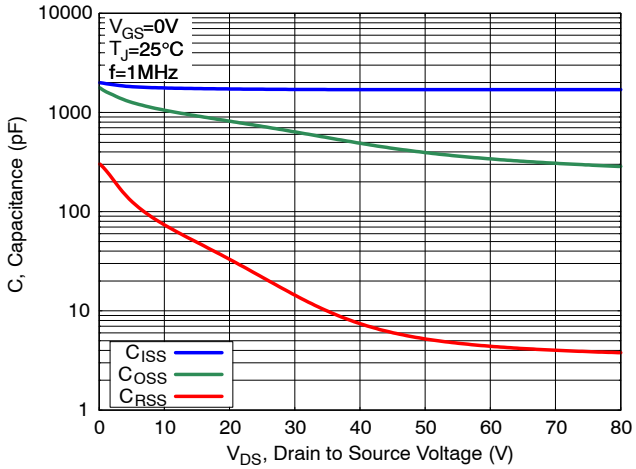


Figure 7. Capacitance Characteristics

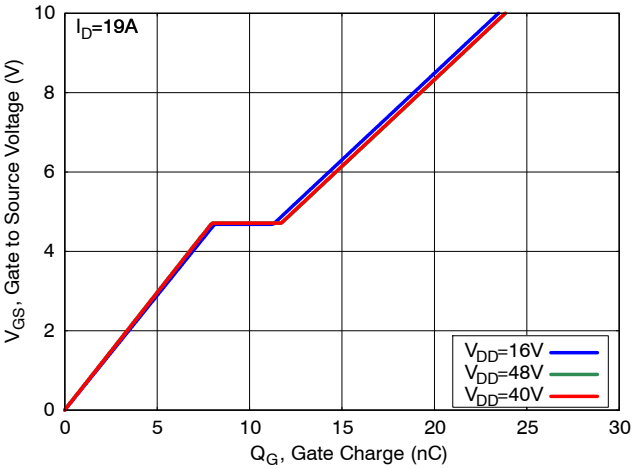


Figure 8. Gate Charge Characteristics

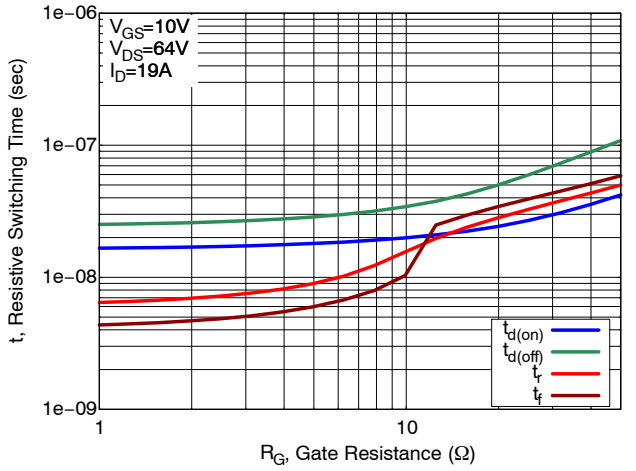


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

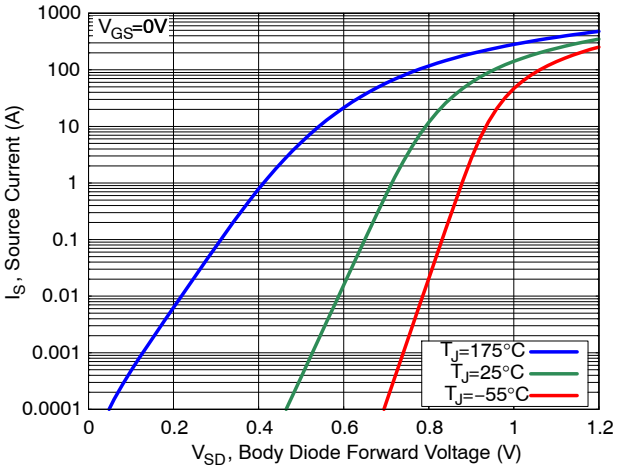


Figure 10. Diode Forward Characteristics

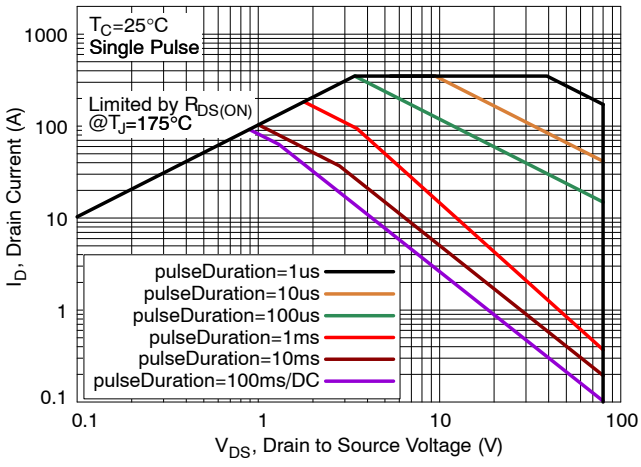


Figure 11. Safe Operating Area (SOA)

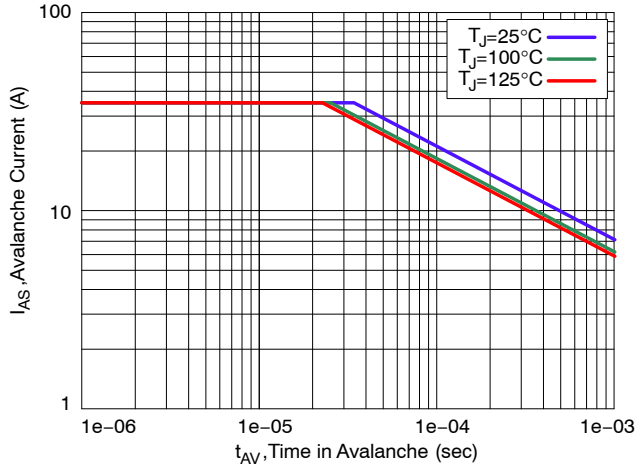


Figure 12. Avalanche Current vs Pulse Time (UIS)

TYPICAL CHARACTERISTICS

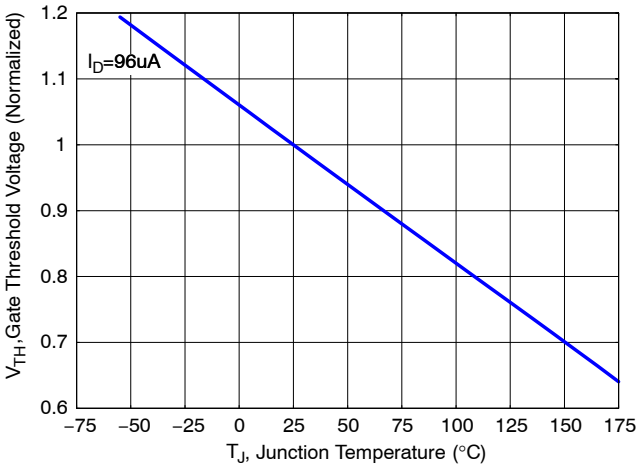


Figure 13. Gate Threshold Voltage vs. Junction Temperature

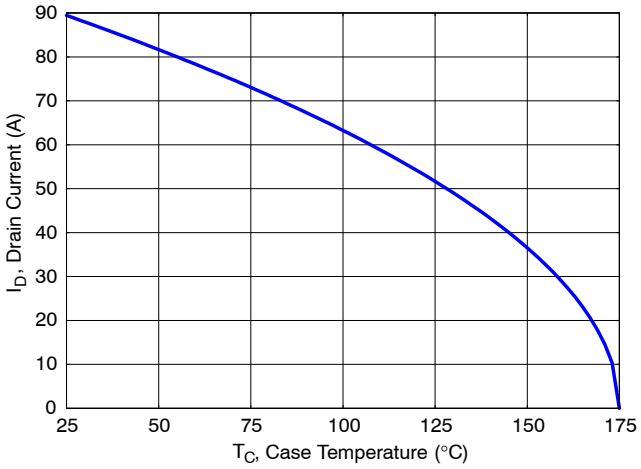


Figure 14. Maximum Current vs. Case Temperature

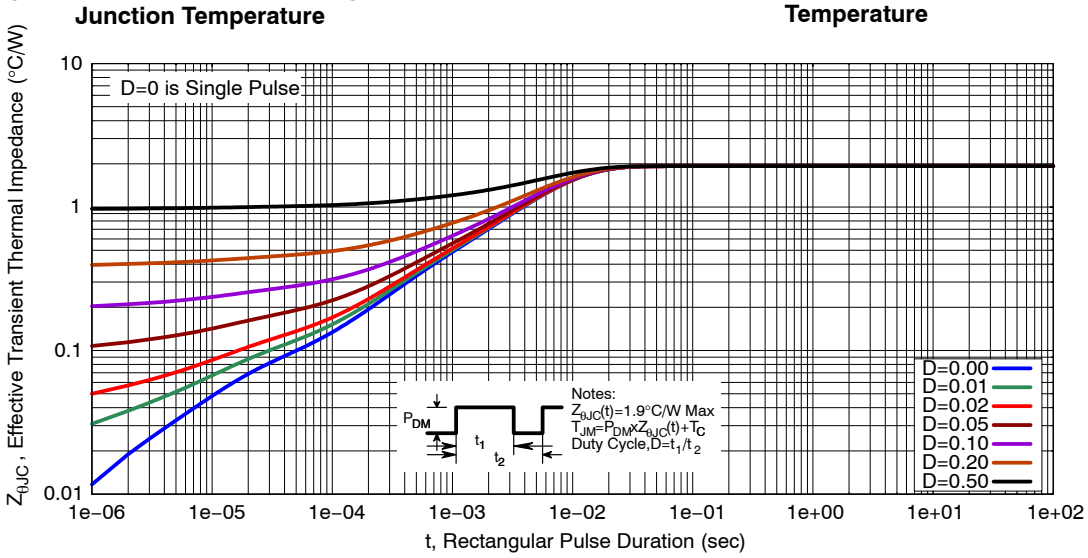
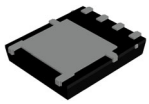
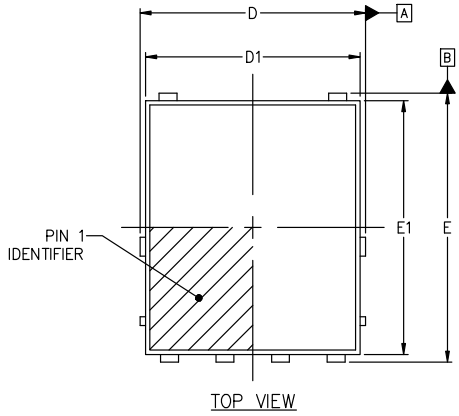


Figure 15. Transient Thermal Response



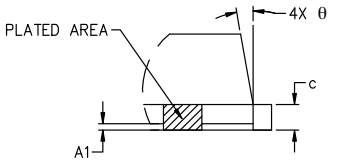
DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BA
ISSUE C

DATE 19 SEP 2024

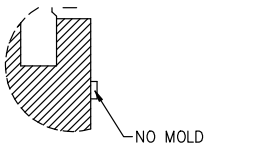


NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M−2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

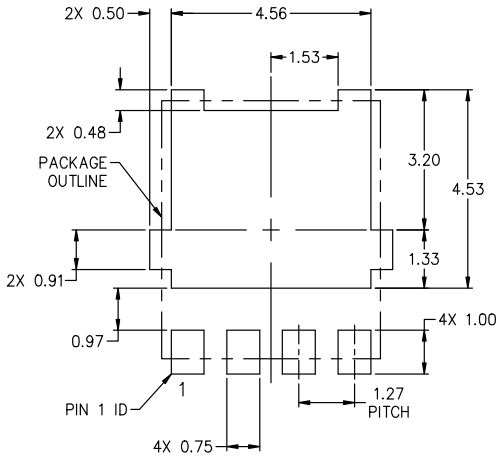


DETAIL "A"
SCALE 2:1



DETAIL "B"
SCALE 2:1

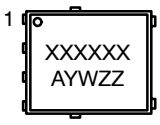
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
θ	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFNW5 4.90x5.90x1.00, 1.27P**	**PAGE 1 OF 1**

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