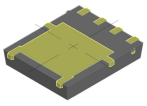
MOSFET – Power, Single N-Channel, STD Gate, SO8FL

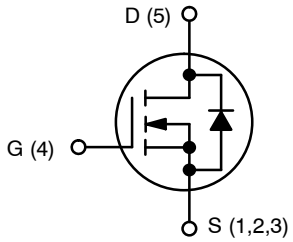
80 V, 1.43 mΩ, 253 A

NVMFWS1D5N08X

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	1.43 mΩ @ 10 V	253 A



DFNW5
(SO8FL WF)
CASE 507BA



N-CHANNEL MOSFET

Features

- Low Q_{RR}, Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen-Free/BFR-Free and are RoHS Compliant

Applications

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
- Motor Drives
- Automotive 48 V System

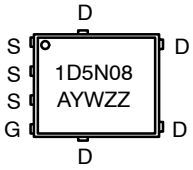
MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain-to-Source Voltage		80	V
V_{GS}	Gate-to-Source Voltage		±20	V
I_D	Continuous Drain Current (Note 1)	T_C = 25 °C	253	A
		T_C = 100 °C	179	
P_D	Power Dissipation (Note 1)	T_C = 25 °C	194	W
I_{DM}	Pulsed Drain Current	T_C = 25 °C, t_p = 100 μs	1071	A
I_{SM}	Pulsed Source Current (Body Diode)		1071	
T_J, T_{stg}	Operating Junction and Storage Temperature Range		−55 to +175	°C
I_S	Source Current (Body Diode)		303	A
E_{AS}	Single Pulse Avalanche Energy (I_{PK} = 67 A) (Note 3)		225	mJ
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Actual continuous current will be limited by thermal & electromechanical application board design.
3. E_{AS} of 225 mJ is based on started T_J = 25 °C, I_{AS} = 67 A, V_{DD} = 64 V, V_{GS} = 10 V, 100% avalanche tested

MARKING DIAGRAM



1D5N08 = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.77	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Notes 4, 5)	39	

4. Surface-mounted on FR4 board using a 1 in^2, 1 oz. Cu pad.
5. $R_{\theta JA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA	80			V
$\Delta V_{(BR)DSS}/\Delta T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25 °C		17.8		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, T_J = 25 °C			1	μA
		V_{DS} = 80 V, T_J = 125 °C			250	
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
ON CHARACTERISTICS						
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 10 V, I_D = 50 A		1.24	1.43	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 330 μA	2.4		3.6	V
$\Delta V_{GS(TH)}/\Delta T_J$	Gate Threshold Voltage Temperature Coefficient	V_{GS} = V_{DS}, I_D = 330 μA		−7.32		mV/°C
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 50 A		176		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz		5880		pF
C_{OSS}	Output Capacitance			1690		
C_{RSS}	Reverse Transfer Capacitance			25		
Q_{OSS}	Output Charge			121		nC
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 6 V, V_{DD} = 40 V; I_D = 50 A		51		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DD} = 40 V; I_D = 50 A		83		
$Q_{G(TH)}$	Threshold Gate Charge			18		
Q_{GS}	Gate-to-Source Charge			27		
Q_{GD}	Gate-to-Drain Charge			13		
V_{GP}	Gate Plateau Voltage			4.6		V
R_G	Gate Resistance	f = 1 MHz		0.6		Ω
SWITCHING CHARACTERISTICS						
$t_{d(ON)}$	Turn-On Delay Time	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 64 V, I_D = 50 A, R_G = 2.5 Ω		24		ns
t_r	Rise Time			10		
$t_{d(OFF)}$	Turn-Off Delay Time			45		
t_f	Fall Time			9		
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 50 A, T_J = 25 °C		0.81	1.2	V
		V_{GS} = 0 V, I_S = 50 A, T_J = 125 °C		0.66		
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 50 A, dI/dt = 1000 A/μs, V_{DD} = 64 V		36		ns
t_a	Charge Time			19		
t_b	Discharge Time			18		
Q_{RR}	Reverse Recovery Charge			290		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

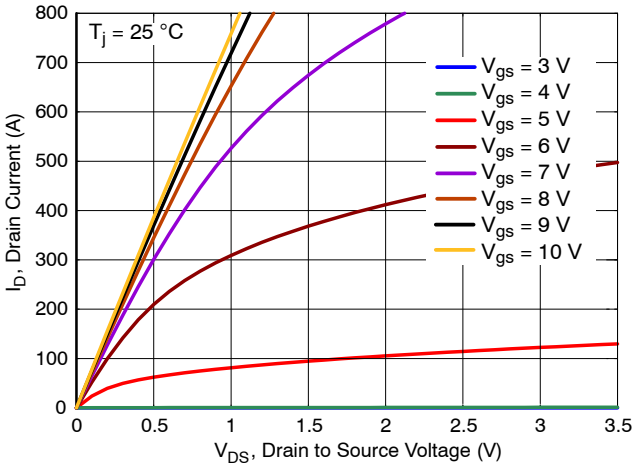


Figure 1. On-Region Characteristics

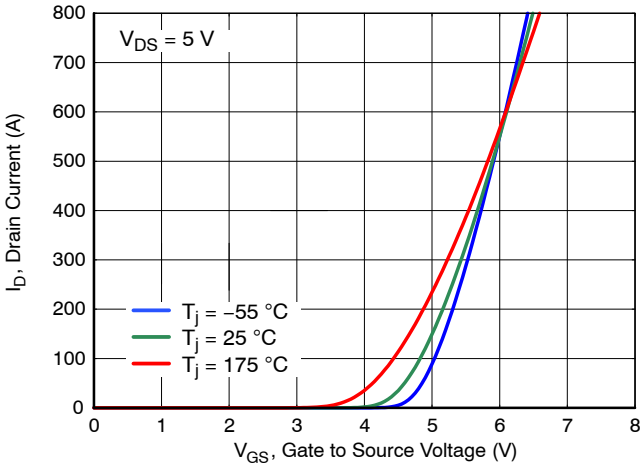


Figure 2. Transfer Characteristics

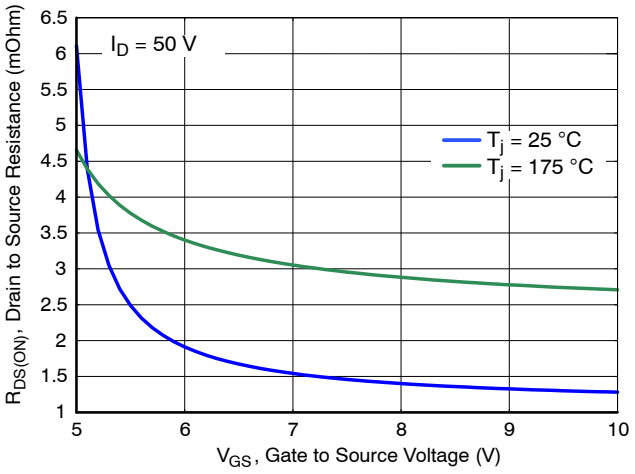


Figure 3. On-Resistance vs. Gate Voltage

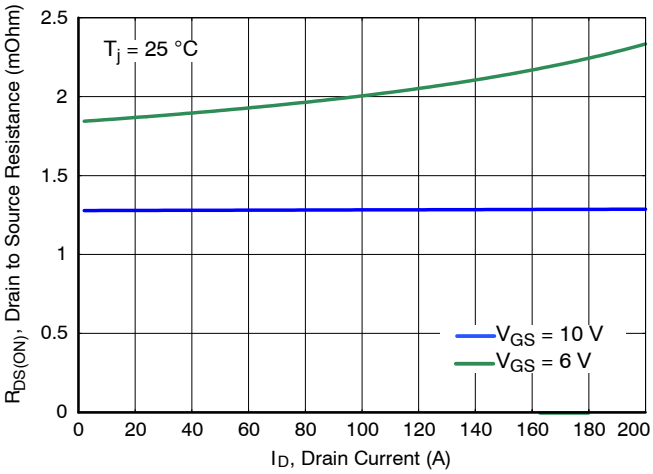


Figure 4. On-Resistance vs. Drain Current

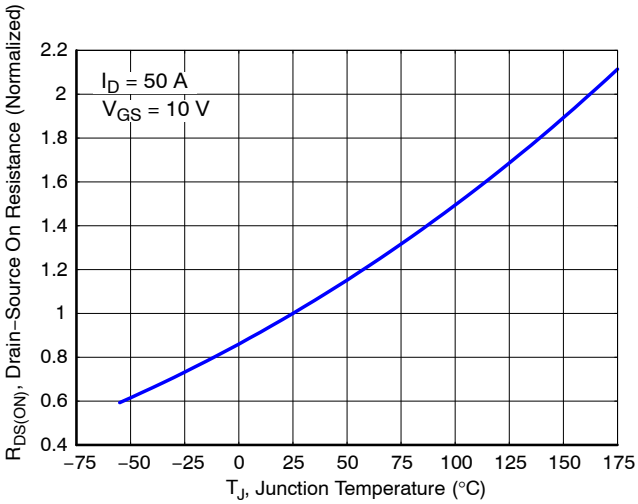


Figure 5. Normalized On-Resistance vs. Junction Temperature

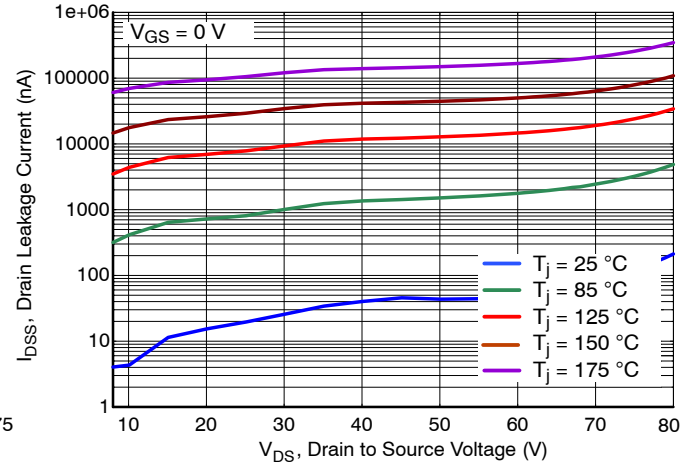


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

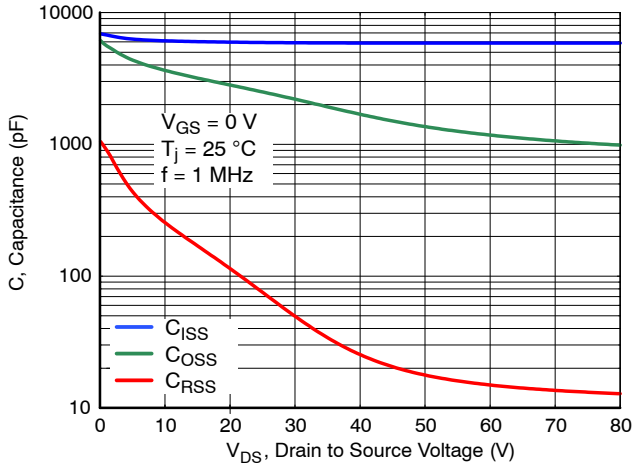


Figure 7. Capacitance Characteristics

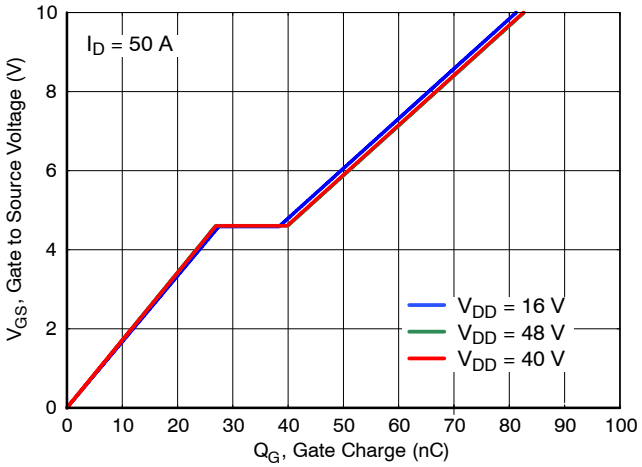


Figure 8. Gate Charge Characteristics

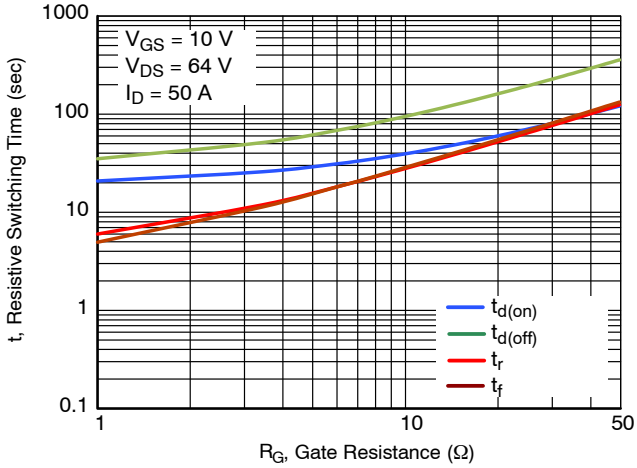


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

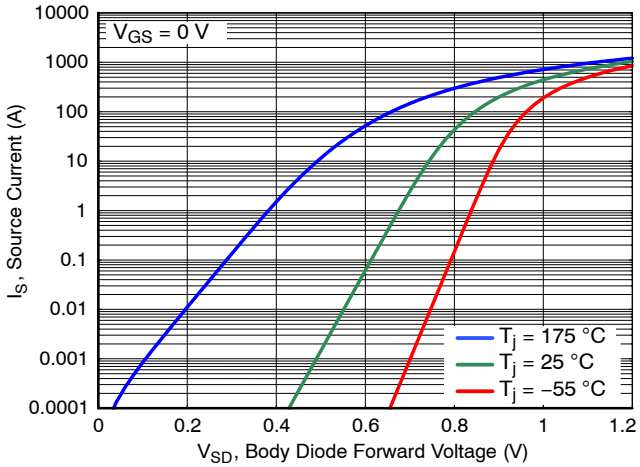


Figure 10. Diode Forward Characteristics

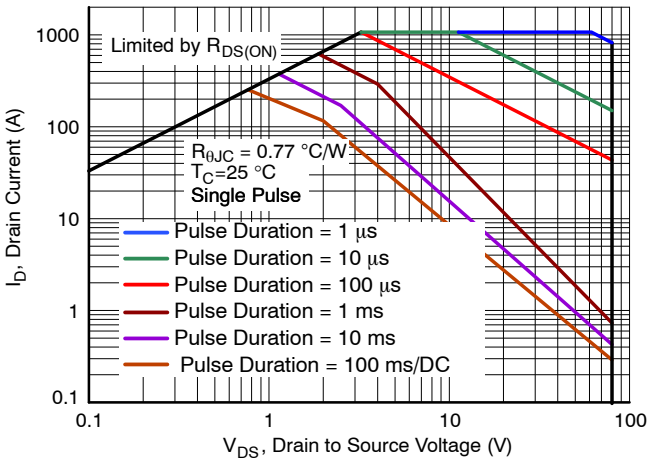


Figure 11. Safe Operating Area (SOA)

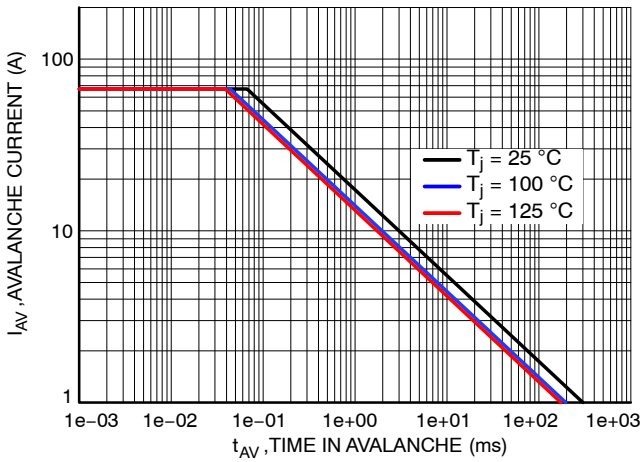


Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS

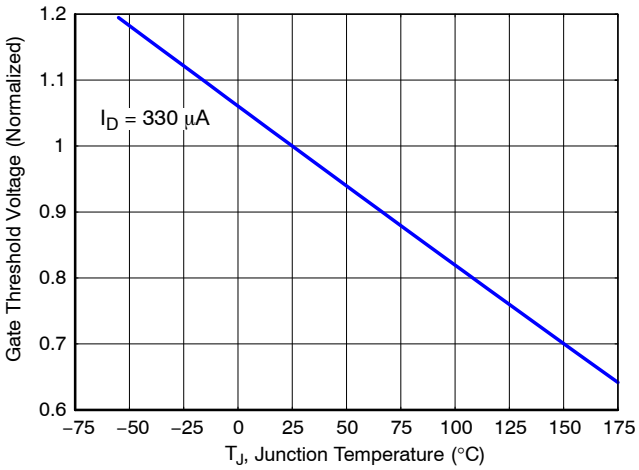


Figure 13. Gate Threshold Voltage vs. Junction Temperature

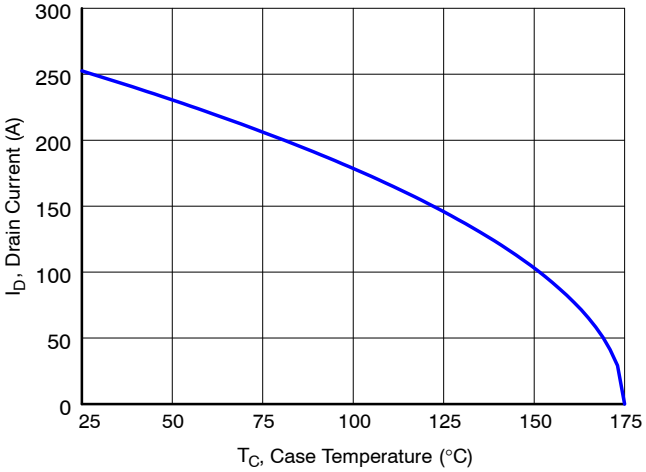


Figure 14. Maximum Current vs. Case Temperature

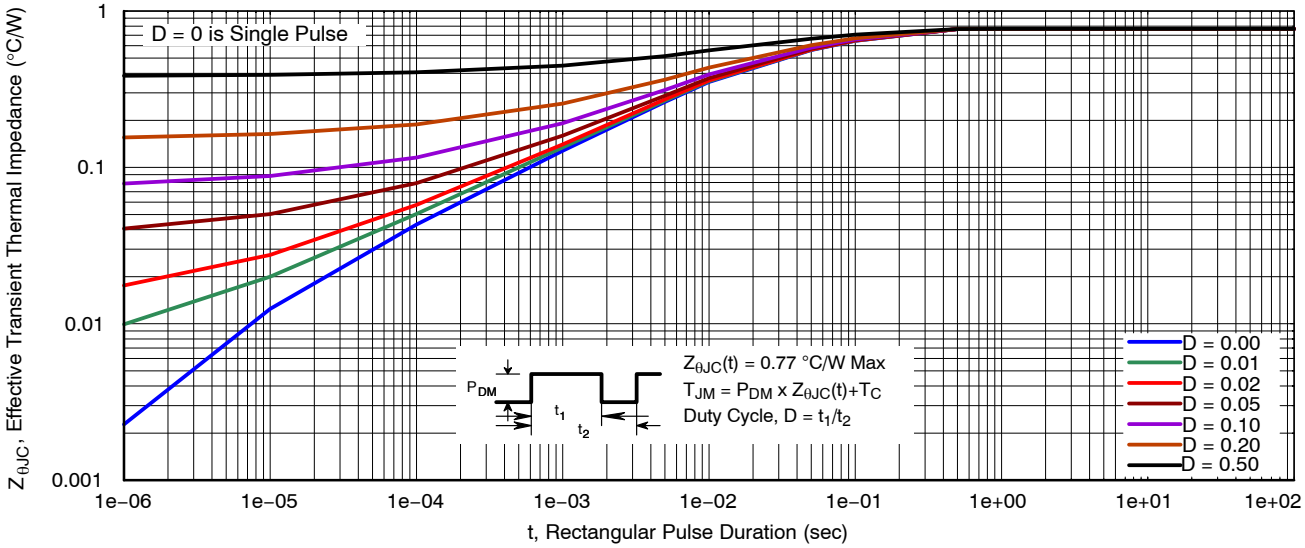


Figure 15. Transient Thermal Response

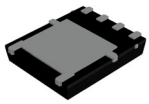
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFWS1D5N08XT1G	1D5N08	DFNW5 (Pb-Free)	1,500 / Tape & Reel
NVMFWS1D5N08XET1G	1D5N08	DFNW5 (Pb-Free)	1,500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

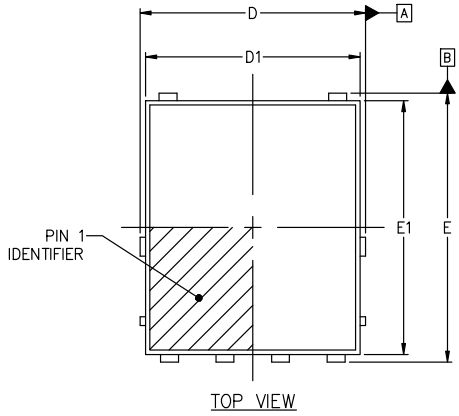
REVISION HISTORY

Revision	Description of Changes	Date
0	Would like to request to reuse back the industrial part version of NTMFWS1D5N08XT1G Datasheet attached here with just revising the OPN, switching part value using 80% of VDS (already Strikethrough) and its curve (Figure 9) generated from Fit request#18313 particularly for Auto version one NVMFWS1D5N08XT1G. Based off of the NTMFWS1D5N08X/D.	4/21/2023
1	Addition of NVMFWS1D5N08XET1G OPN in the data sheet.	3/3/2026



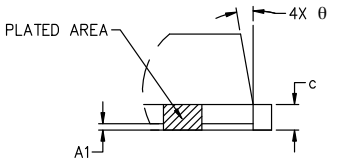
DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BA
ISSUE C

DATE 19 SEP 2024

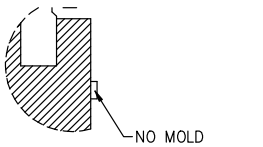


NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M−2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

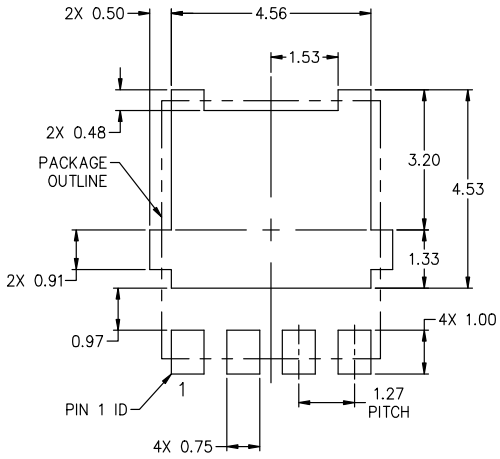


DETAIL "A"
SCALE 2:1



DETAIL "B"
SCALE 2:1

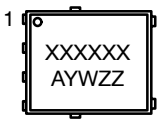
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
θ	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON26450H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DFNW5 4.90x5.90x1.00, 1.27P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales