

# MOSFET - Power, Single N-Channel, STD Gate, SO8-FL

40 V, 0.52 mΩ, 414 A

## NVMFWS0D5N04XM

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Small Footprint (5 x 6 mm) with Compact Design
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

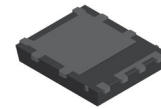
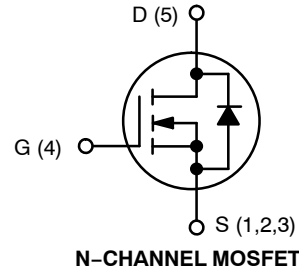
- Motor Drive
- Battery Protection
- Synchronous Rectification

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	40	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_C = 25^\circ\text{C}$	414
		$T_C = 100^\circ\text{C}$	293
Power Dissipation	$P_D$	163	W
Pulsed Drain Current	$I_{DM}$	$T_C = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	900
Pulsed Source Current (Body Diode)			$I_{SM}$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	251	A
Single Pulse Avalanche Energy	$I_{PK} = 28.2 \text{ A}$	$E_{AS}$	1434 mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

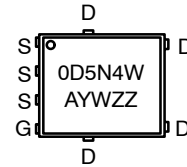
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$V_{(BR)DSS}$	$R_{DS(on) MAX}$	$I_D MAX$
40 V	0.52 mΩ @ 10 V	414 A



DFNW5 (SO-8FL WF)  
CASE 507BD

### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVMFWS0D5N04XM

## THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	0.92	°C/W
Thermal Resistance, Junction-to-Ambient (Notes 1, 2)	$R_{\theta JA}$	38.9	

- Surface-mounted on FR4 board using 650 mm<sup>2</sup> pad, 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$ , Referenced to $25^\circ\text{C}$		15		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40\text{ V}, T_J = 25^\circ\text{C}$			1	μA
		$V_{DS} = 40\text{ V}, T_J = 125^\circ\text{C}$			60	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

### ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}, T_J = 25^\circ\text{C}$		0.43	0.52	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 240\text{ }\mu\text{A}, T_J = 25^\circ\text{C}$	2.5	3.0	3.5	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 240\text{ }\mu\text{A}$		-7.21		mV/°C
Forward Trans-conductance	$g_{FS}$	$V_{DS} = 5\text{ V}, I_D = 50\text{ A}$		267		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		6232		pF	
Output Capacitance	$C_{OSS}$			3987			
Reverse Transfer Capacitance	$C_{RSS}$			53.9			
Total Gate Charge	$Q_G(TOT)$	$V_{DD} = 32\text{ V}, I_D = 50\text{ A}, V_{GS} = 6\text{ V}$		60.5		nC	
Total Gate Charge	$Q_G(TOT)$		$V_{DD} = 32\text{ V}, I_D = 50\text{ A}, V_{GS} = 10\text{ V}$		97.9		
Threshold Gate Charge	$Q_G(TH)$				18.2		
Gate-to-Source Charge	$Q_{GS}$				27.4		
Gate-to-Drain Charge	$Q_{GD}$				18.5		
Gate Resistance	$R_G$			$f = 1\text{ MHz}$			0.47

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}$ , $V_{DD} = 32\text{ V}, I_D = 50\text{ A}, R_G = 0\text{ }\Omega$		8.64		ns
Rise Time	$t_r$			7.02		
Turn-Off Delay Time	$t_{d(OFF)}$			13.7		
Fall Time	$t_f$			6.85		

### SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$I_S = 50\text{ A}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$		0.8	1.2	V
		$I_S = 50\text{ A}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$		0.65		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 32\text{ V}$		101		ns
Charge Time	$t_a$			56.9		
Discharge Time	$t_b$			44.8		
Reverse Recovery Charge	$Q_{RR}$			286		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

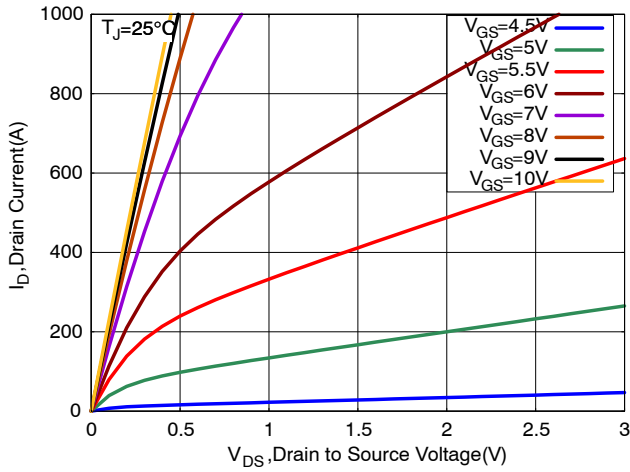


Figure 1. On-Region Characteristics

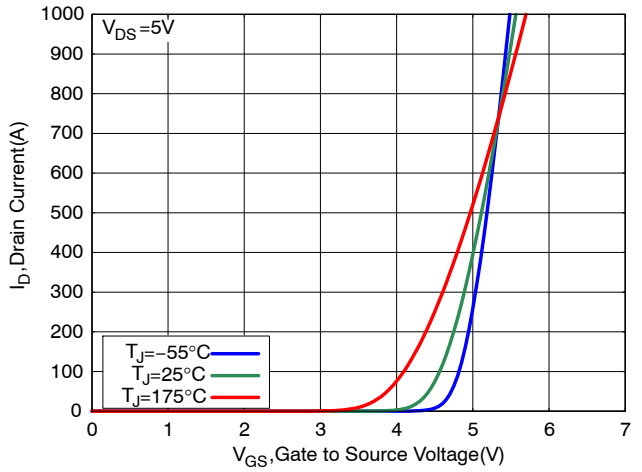


Figure 2. Transfer Characteristics

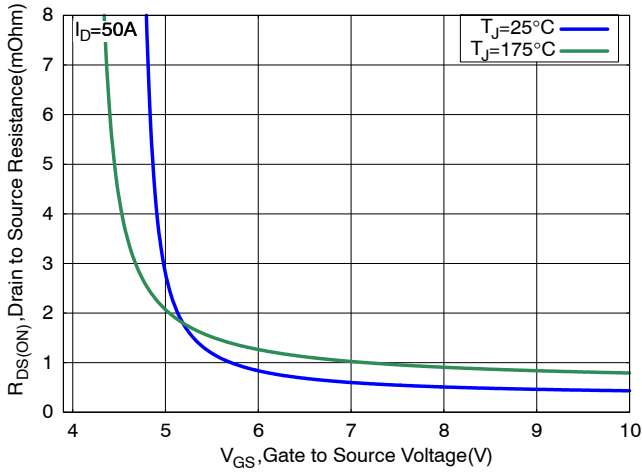


Figure 3. On-Resistance vs. Gate Voltage

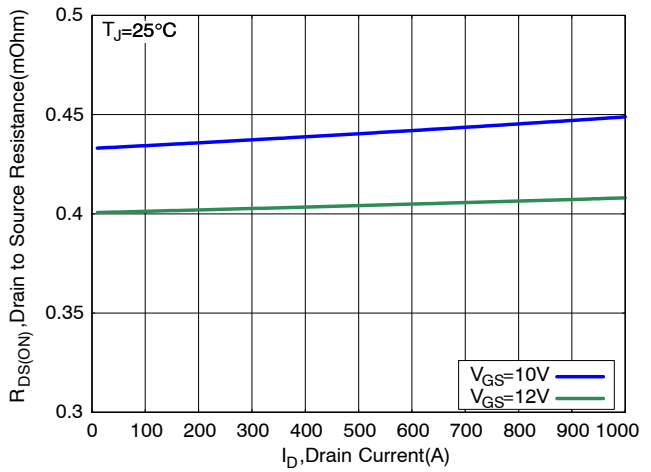


Figure 4. On-Resistance vs. Drain Current

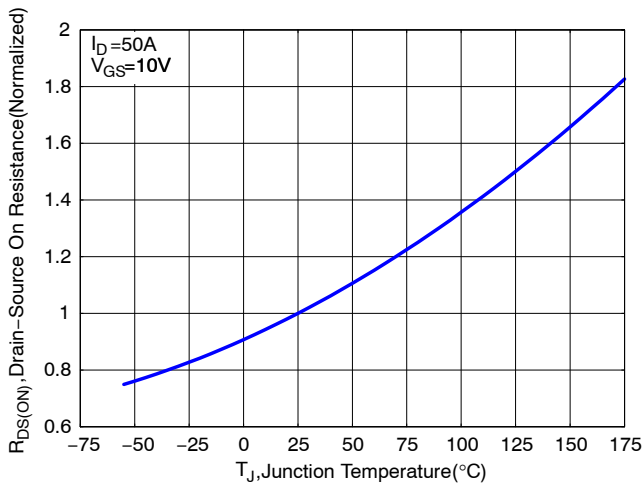


Figure 5. Normalized ON Resistance vs. Junction Temperature

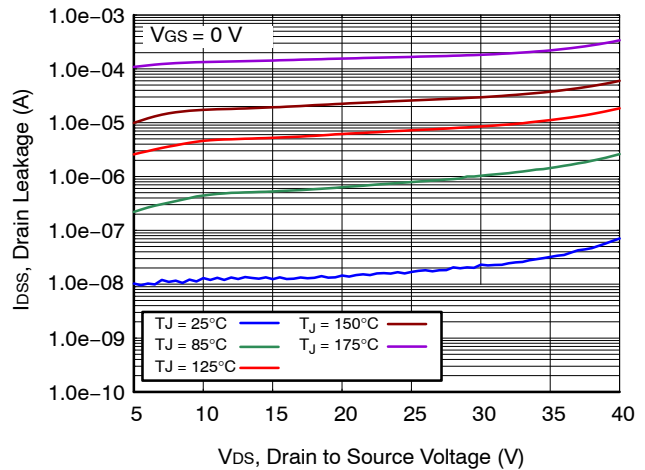


Figure 6. Drain Leakage vs. Drain to Source Voltage

# NVMFWS0D5N04XM

## TYPICAL CHARACTERISTICS (continued)

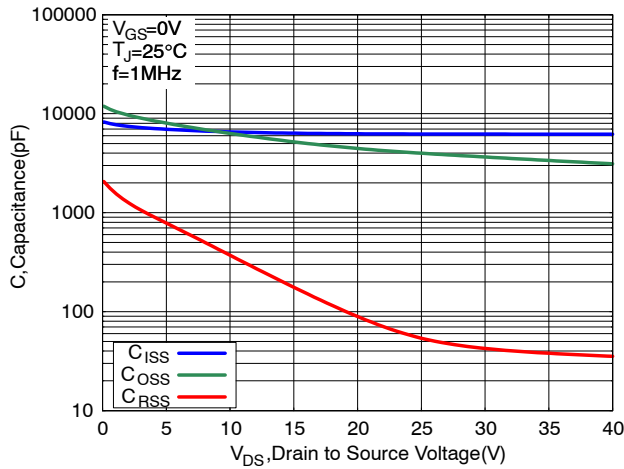


Figure 7. Capacitance Characteristics

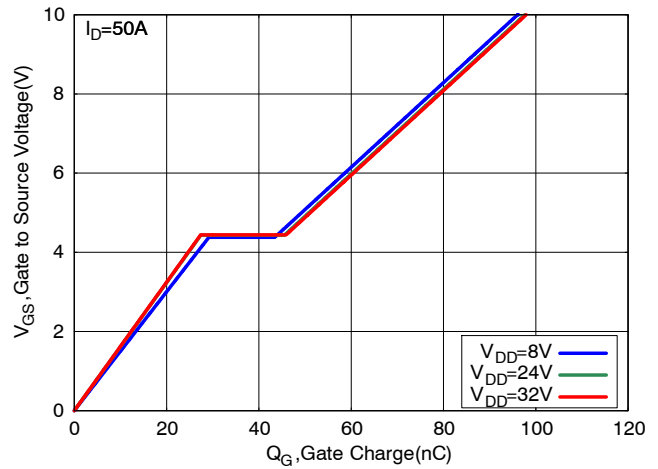


Figure 8. Gate Charge Characteristics

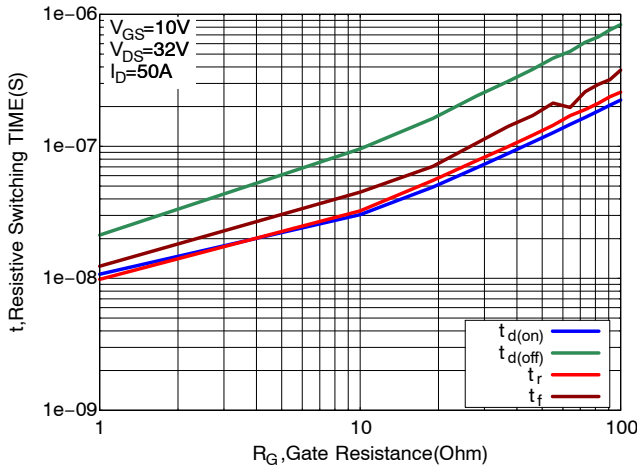


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

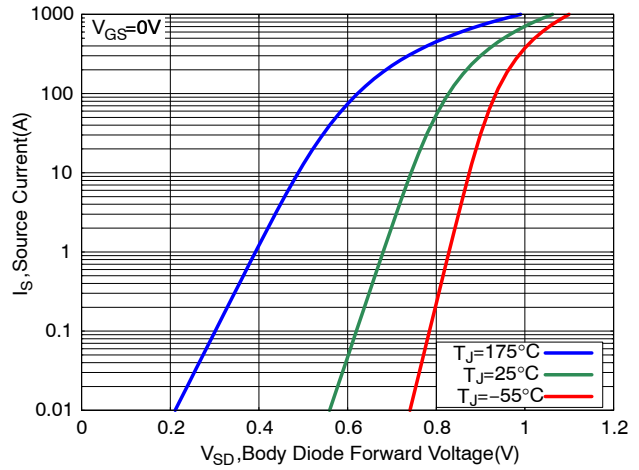


Figure 10. Diode Forward Characteristics

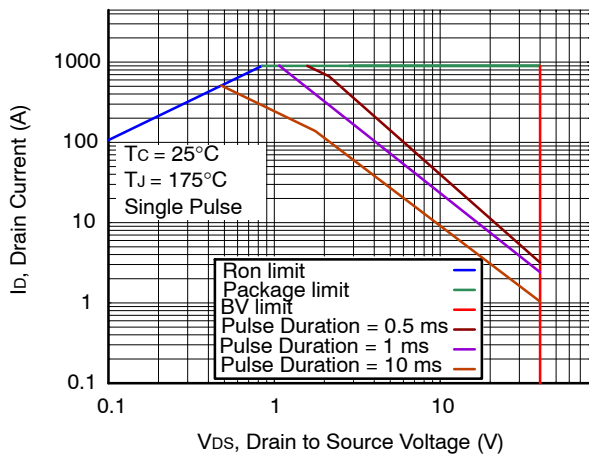


Figure 11. Maximum Rated Forward Biased Safe Operating Area

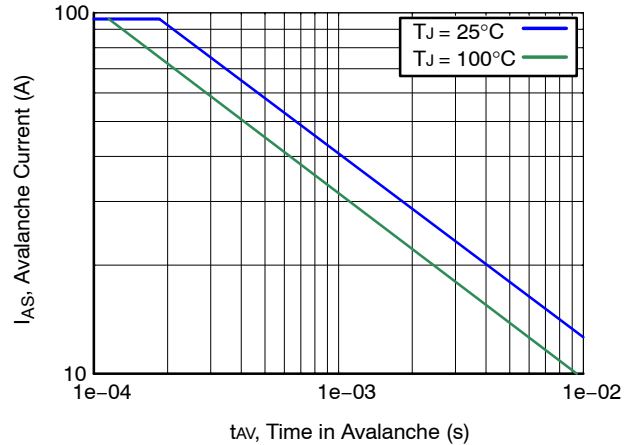


Figure 12.  $I_{peak}$  vs. Time in Avalanche

# NVMFWS0D5N04XM

## TYPICAL CHARACTERISTICS (continued)

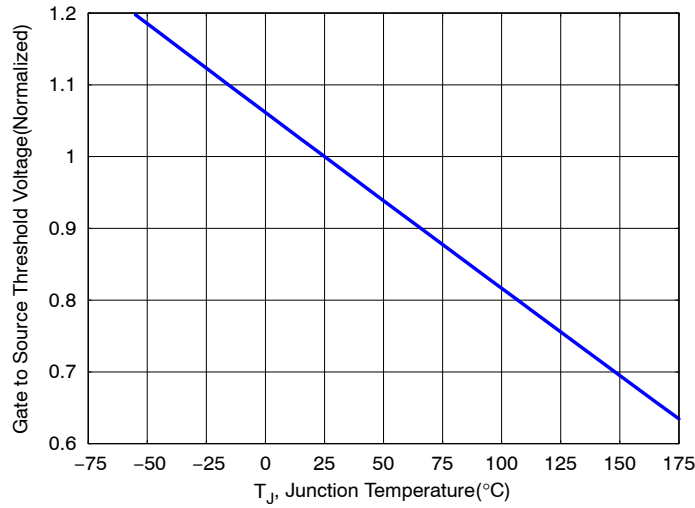


Figure 13. Gate Threshold Voltage vs. Junction Temperature

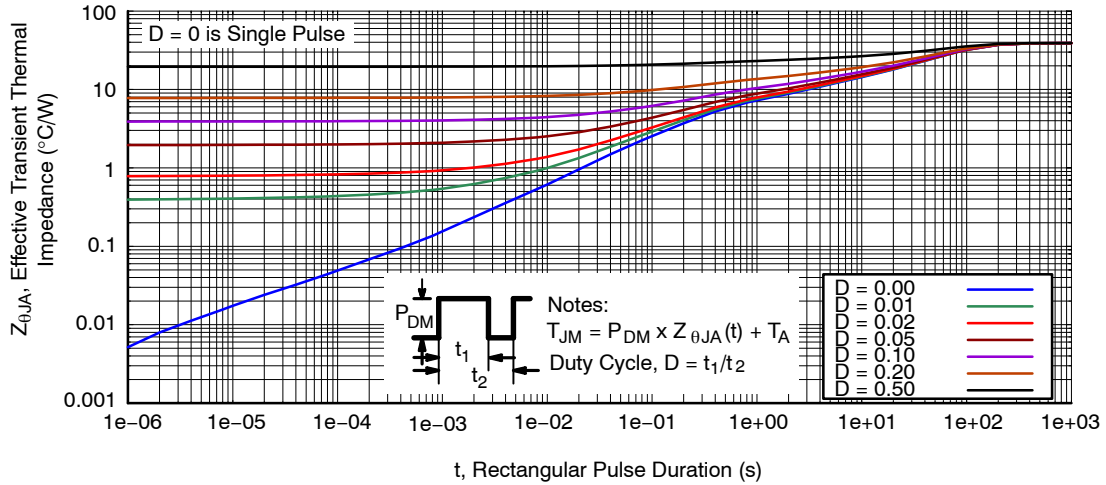


Figure 14. Thermal Characteristics

### DEVICE ORDERING INFORMATION

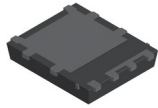
Device	Marking	Package	Shipping <sup>†</sup>
NVMFWS0D5N04XMT1G	0D5N4W	DFNW5 (Pb-Free)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

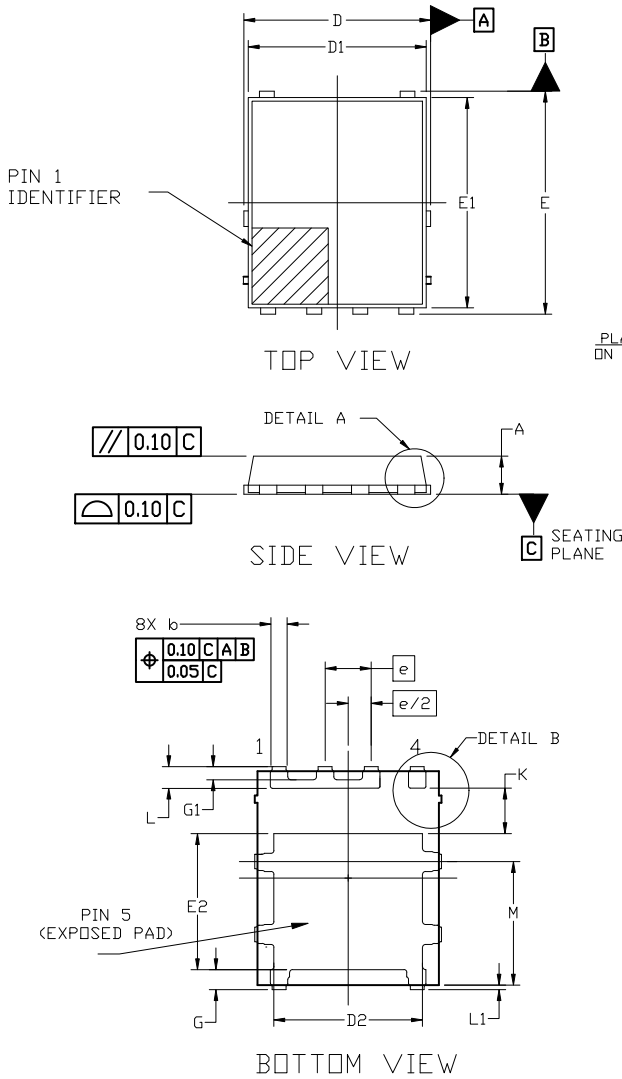
## PACKAGE DIMENSIONS

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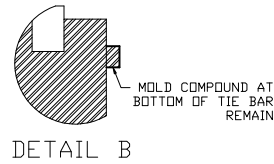
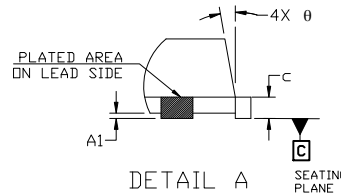
### DFNW5 5x6, FULL-CUT SO8FL WF CASE 507BD ISSUE O

DATE 13 APR 2021

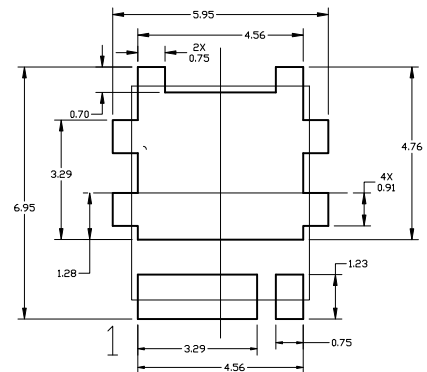


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.



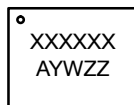
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.80	5.00	5.20
D2	3.90	4.10	4.30
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.55	3.75	3.95
e	1.27 BSC		
G	0.50	0.55	0.70
G1	0.26	0.36	0.46
k	1.10	1.25	1.40
L	0.50	0.60	0.70
L1	0.150 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



**RECOMMENDED MOUNTING FOOTPRINT**

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

**GENERIC MARKING DIAGRAM\***



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Assembly Lot

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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