MOSFET - Power, Single P-Channel

-40 V, 9.5 mΩ, -77 A

NVMFS9D6P04M8L

V$_{(BR)DSS}$	R$_{DS(on)}$ MAX	I$_D$ MAX
−40 V	9.5 mΩ @ −10 V	−77 A
	13.8 mΩ @ −4.5 V	

Features

- Small Footprint for Compact Design
- Low R$_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFWS9D6P04M8L − Wettable Flanks Product
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR−Free and are RoHS Compliant

P−Channel MOSFET

D (5−8)

G (4)

S (1,2,3)

**DFN5 (SO−8FL)
STYLE 1
CASE 488AA**

MARKING DIAGRAM

1

XXXXXX
AYWZZ

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

MAXIMUM RATINGS (T$_J$ = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V$_{DSS}$	−40	V
Gate−to−Source Voltage			V$_{GS}$	±20	V
Continuous Drain Current R$_{θJC}$ (Notes 1, 2, 4)	Steady State	T$_C$ = 25°C	I$_D$	−77.0	A
		T$_C$ = 100°C		−54.4	
Power Dissipation R$_{θJC}$ (Notes 1, 2)		T$_C$ = 25°C	P$_D$	75	W
		T$_C$ = 100°C		38	
Continuous Drain Current R$_{θJA}$ (Notes 1, 3, 4)	Steady State	T$_A$ = 25°C	I$_D$	−17.1	A
		T$_A$ = 100°C		−12.1	
Power Dissipation R$_{θJA}$ (Notes 1, 3)		T$_A$ = 25°C	P$_D$	3.7	W
		T$_A$ = 100°C		1.8	
Pulsed Drain Current	T$_A$ = 25°C, t$_p$ = 10 μs		I$_{DM}$	450	A
Operating Junction and Storage Temperature Range			T$_J$, T$_{stg}$	−55 to +175	°C
Source Current (Body Diode)			I$_S$	−62	A
Single Pulse Drain−to−Source Avalanche Energy (I$_{L(pk)}$ = −8.5 A)			E$_{AS}$	259	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T$_L$	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
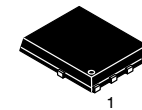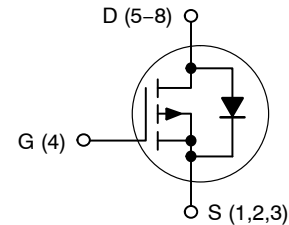
THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction−to−Case – Steady State (Drain) (Notes 1, 2, 4)	R$_{θJC}$	2	°C/W
Junction−to−Ambient – Steady State (Note 3)	R$_{θJA}$	40.7	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Assumes heat−sink sufficiently large to maintain constant case temperature independent of device power.
3. Surface−mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

December, 2024 – Rev. 1

Publication Order Number:
NVMFS9D6P04M8L/D

NVMFS9D6P04M8L

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				21		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −40 V	T_J = 25°C			−1.0	μA
			T_J = 125°C			−1000	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −580 μA		−1.0		−2.4	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−5.1		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −10 V, I_D = −20 A			7.15	9.5	mΩ
		V_{GS} = −4.5 V, I_D = −10 A			10.4	13.8	
Forward Transconductance	g_{FS}	V_{DS} = −1.5 V, I_D = −15 A			36		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −20 V			2002		pF
Output Capacitance	C_{oss}				935		
Reverse Transfer Capacitance	C_{rss}				43		
Total Gate Charge	$Q_{G(TOT)}$	V_{DS} = −20 V, I_D = −20 A	V_{GS} = −4.5 V		15.04		nC
			V_{GS} = −10 V		14.47		
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = −10 V, V_{DS} = −20 V, I_D = −20 A			4.27		nC
Gate−to−Source Charge	Q_{GS}				11.94		
Gate−to−Drain Charge	Q_{GD}				12.83		
Plateau Voltage	V_{GP}				3.63		V
SWITCHING CHARACTERISTICS, V_{GS} = −4.5 V (Note 6)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −4.5 V, V_{DS} = −20 V, I_D = −20 A, R_G = 2.5 Ω			13.1		ns
Rise Time	t_r				103		
Turn−Off Delay Time	$t_{d(off)}$				83.3		
Fall Time	t_f				63.0		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −20 A	T_J = 25°C		−0.86	−1.25	V
			T_J = 125°C		−0.74		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = −20 A			54.6		ns
Charge Time	t_a				34.9		
Discharge Time	t_b				19.7		
Reverse Recovery Charge	Q_{RR}				97.9		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

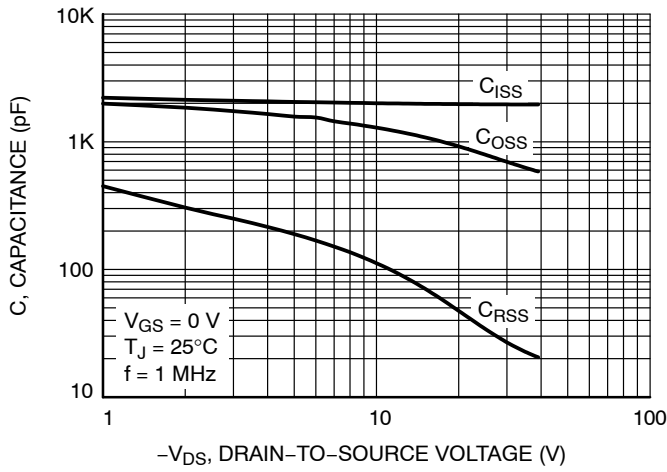Figure 1. On−Region Characteristics

Figure 2. Transfer Characteristics

Figure 3. On−Resistance vs. Gate−to−Source
Voltage

Figure 4. On−Resistance vs. Drain Current and
Gate Voltage

Figure 5. On−Resistance Variation with
Temperature

Figure 6. Drain−to−Source Leakage Current
vs. Voltage

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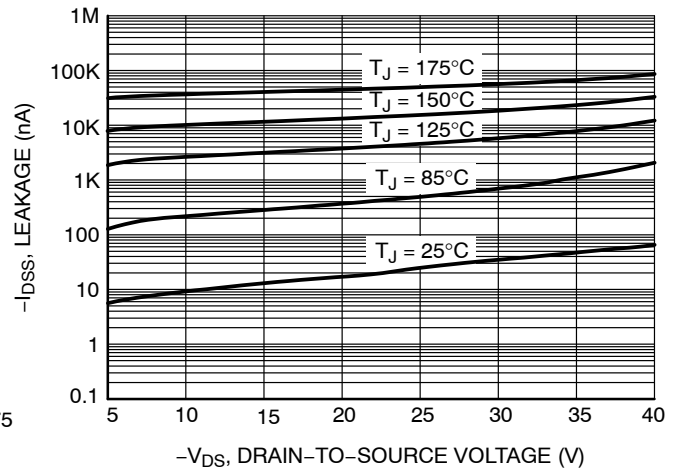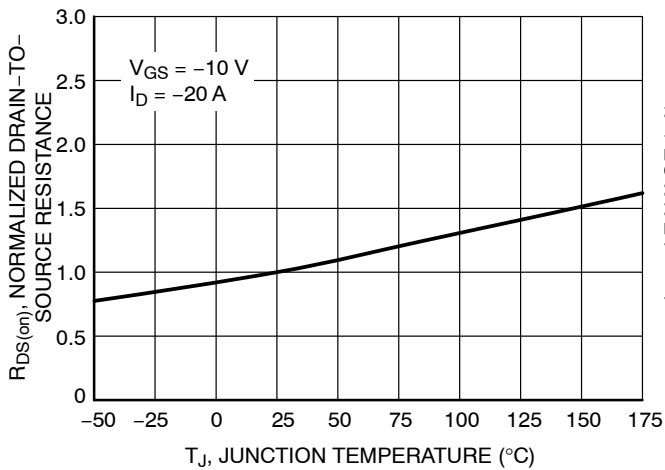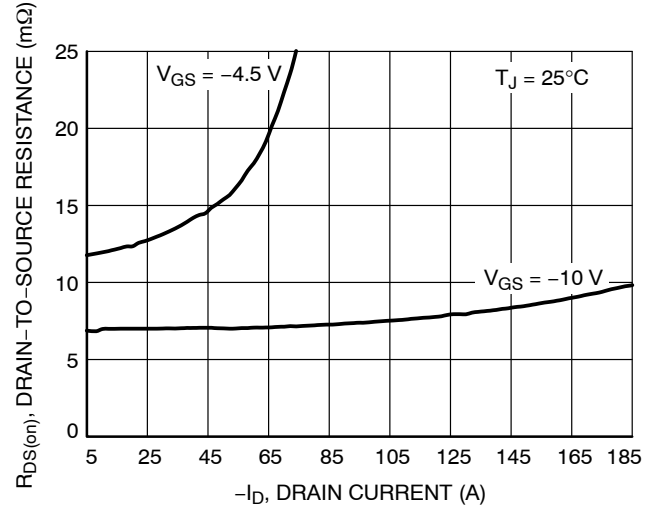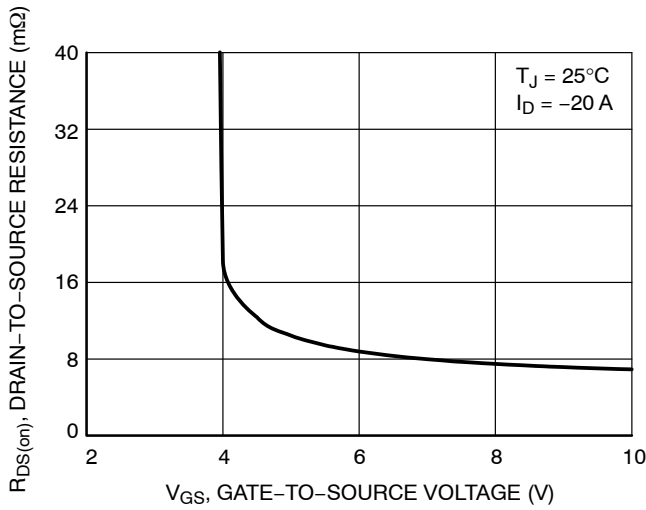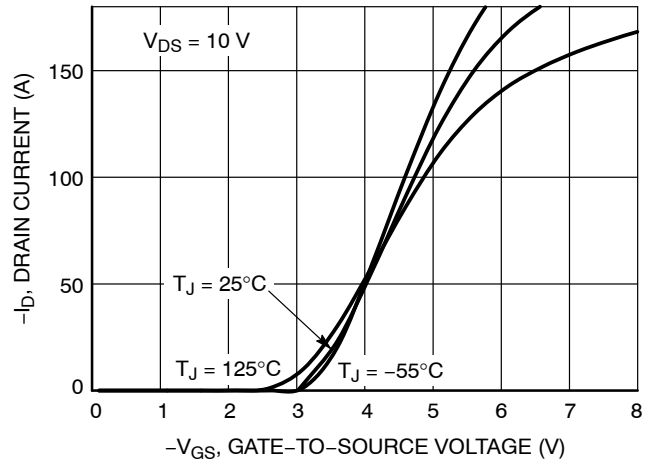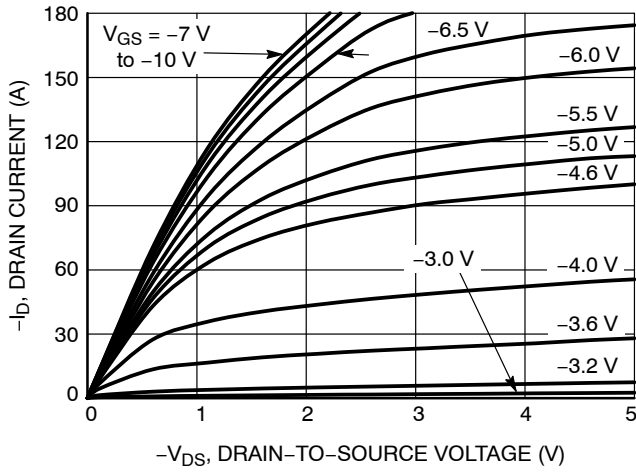
Figure 7. Capacitance Variation
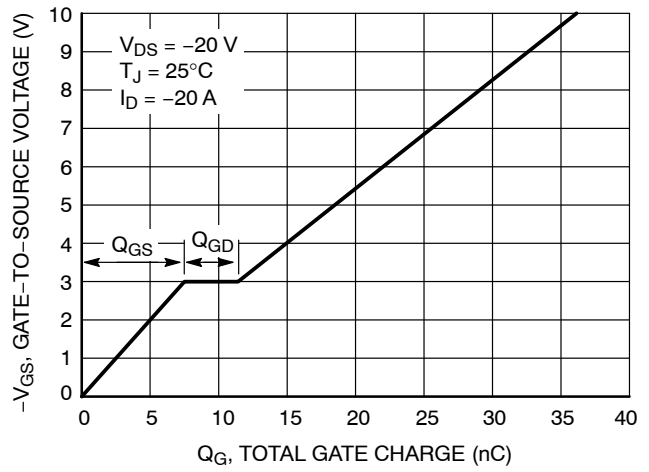
Figure 8. Gate−to−Source vs. Total Charge
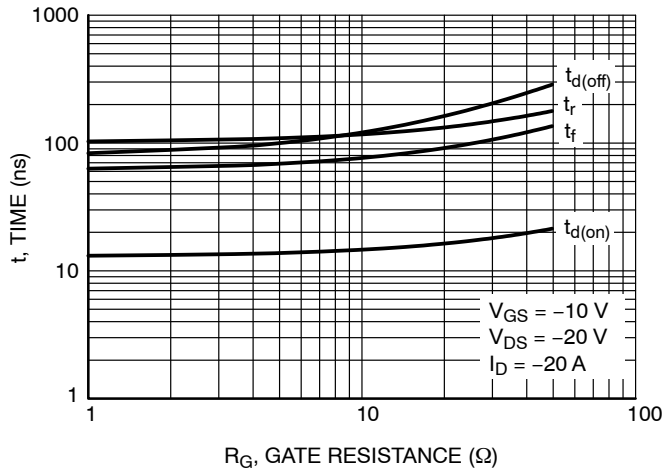
Figure 9. Resistive Switching Time Variation vs. Gate Resistance
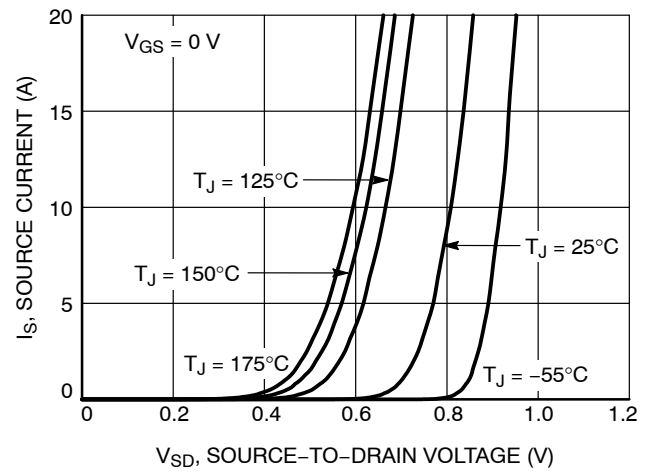
Figure 10. Diode Forward Voltage vs. Current
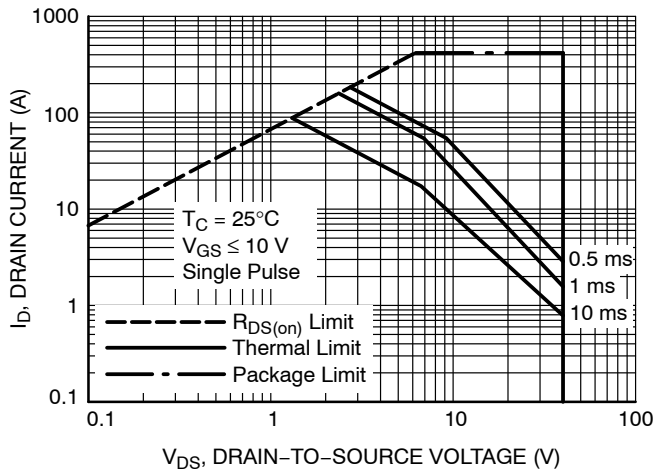
Figure 11. Maximum Rated Forward Biased Safe Operating Area
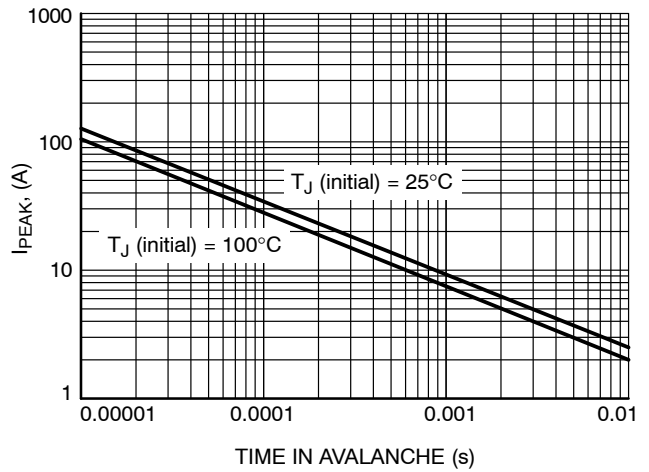
Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS
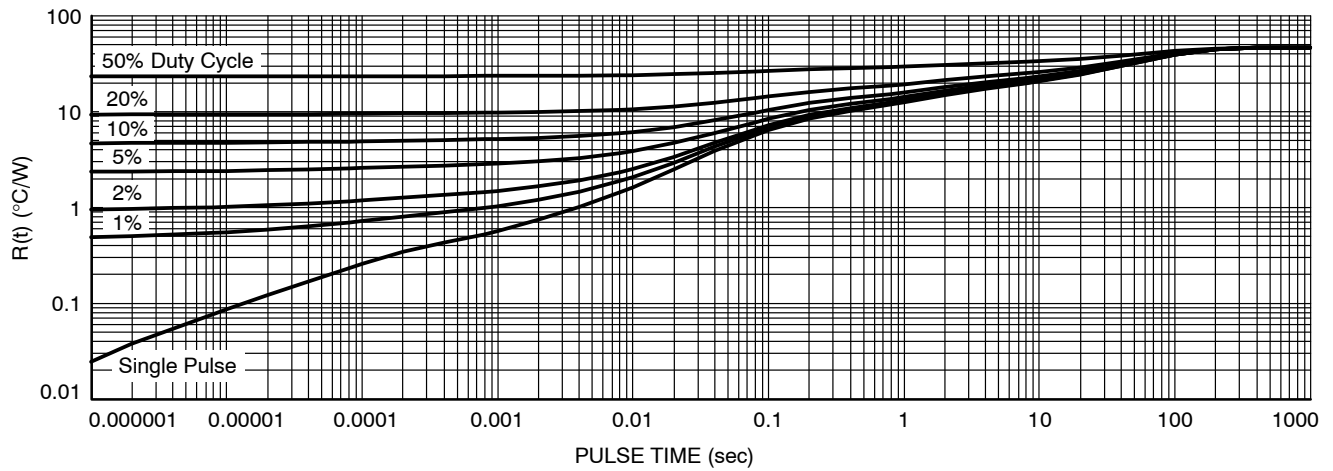
Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping[†]
NVMFS9D6P04M8LT1G	V9D6PL	DFNW5 (Pb–Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE N

TOP VIEW

SIDE VIEW

DETAIL A

DETAIL A

SEATING PLANE

BOTTOM VIEW
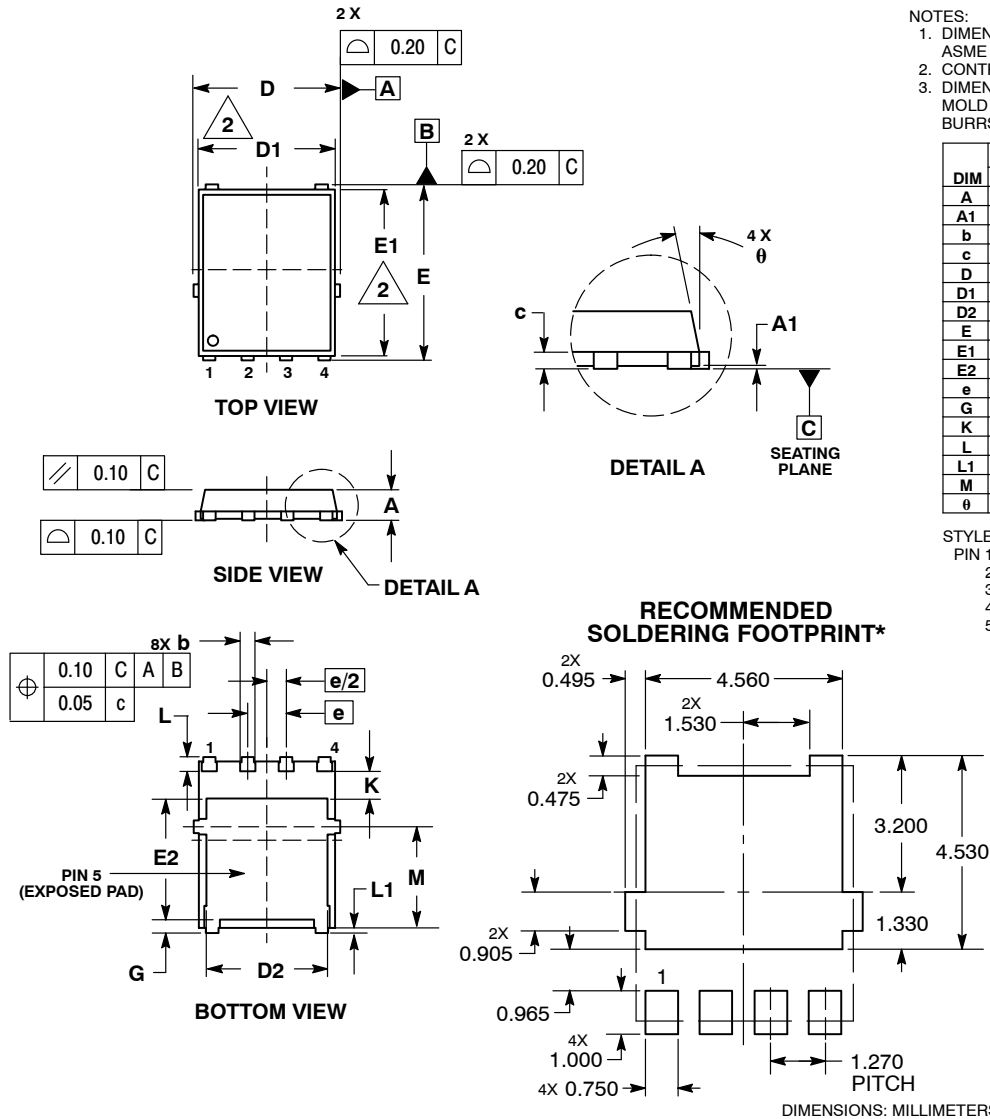
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–––	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	–––	12 °

STYLE 1:
PIN 1. SOURCE
    2. SOURCE
    3. SOURCE
    4. GATE
    5. DRAIN

RECOMMENDED SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ADDITIONAL INFORMATION

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