

# MOSFET – Power, Single N-Channel, DFN5/DFNW5

60 V, 71 A, 6.1 mΩ

## NVMFS5C670NL

### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- NVMFS5C670NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-to-Source Voltage	60	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$ 71 A
			$T_C = 100^\circ\text{C}$ 50
			$T_C = 25^\circ\text{C}$ 61 W
$P_D$	Power Dissipation $R_{\theta JC}$ (Note 1)		$T_C = 100^\circ\text{C}$ 31
$I_D$	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$ 17 A
			$T_A = 100^\circ\text{C}$ 12
			$T_A = 25^\circ\text{C}$ 3.6 W
$P_D$	Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)		$T_A = 100^\circ\text{C}$ 1.8
$I_{DM}$	Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	440 A
$T_J, T_{stg}$	Operating Junction and Storage Temperature	-55 to +175	$^\circ\text{C}$
$I_S$	Source Current (Body Diode)	68	A
$E_{AS}$	Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 3.6 \text{ A}$ )	166	mJ
$T_L$	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	260	$^\circ\text{C}$

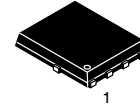
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

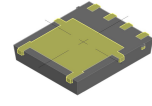
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State	2.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	41	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

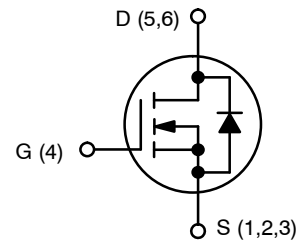
$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
60 V	6.1 mΩ @ 10 V	71 A
	8.8 mΩ @ 4.5 V	



DFN5 (SO-8FL)  
CASE 488AA

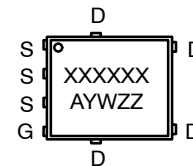


DFNW5  
CASE 507BE



N-CHANNEL MOSFET

### MARKING DIAGRAM



XXXXXX = 5C670L  
(NVMFS5C670NL) or  
670LWF  
(NVMFS5C670NLWF)

A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

# NVMFS5C670NL

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient			27		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		250	
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

## ON CHARACTERISTICS (Note 4)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 53\ \mu\text{A}$	1.2		2.0	V
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient			-4.7		mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}$	$I_D = 35\text{ A}$	5.1	6.1	m $\Omega$
		$V_{GS} = 4.5\text{ V}$	$I_D = 35\text{ A}$	7.0	8.8	
$g_{FS}$	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 35\text{ A}$		82		S

## CHARGES AND CAPACITANCES

$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$		1400		pF
$C_{OSS}$	Output Capacitance			690		
$C_{RSS}$	Reverse Transfer Capacitance			15		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}; I_D = 35\text{ A}$		9.0		nC
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}; I_D = 35\text{ A}$		20		nC
$Q_{G(TH)}$	Threshold Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}; I_D = 35\text{ A}$		2.5		nC
$Q_{GS}$	Gate-to-Source Charge			4.5		
$Q_{GD}$	Gate-to-Drain Charge			2.0		
$V_{GP}$	Plateau Voltage			3.1		

## SWITCHING CHARACTERISTICS (Note 5)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}, I_D = 35\text{ A}, R_G = 2.5\ \Omega$		11		ns
$t_r$	Rise Time			60		
$t_{d(OFF)}$	Turn-Off Delay Time			15		
$t_f$	Fall Time			4		

## DRAIN-SOURCE DIODE CHARACTERISTICS

$V_{SD}$	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 35\text{ A}$	$T_J = 25^\circ\text{C}$		0.9	1.2	V
			$T_J = 125^\circ\text{C}$		0.8		
$t_{RR}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 35\text{ A}$		34		ns	
$t_a$	Charge Time			17			
$t_b$	Discharge Time			17			
$Q_{RR}$	Reverse Recovery Charge			19			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

# NVMFS5C670NL

## TYPICAL CHARACTERISTICS

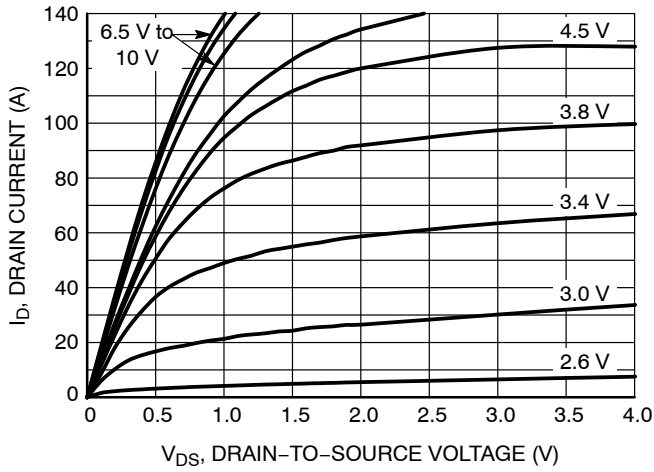


Figure 1. On-Region Characteristics

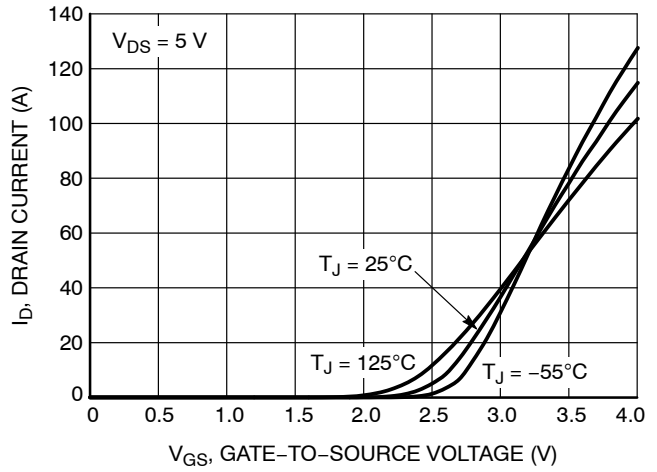


Figure 2. Transfer Characteristics

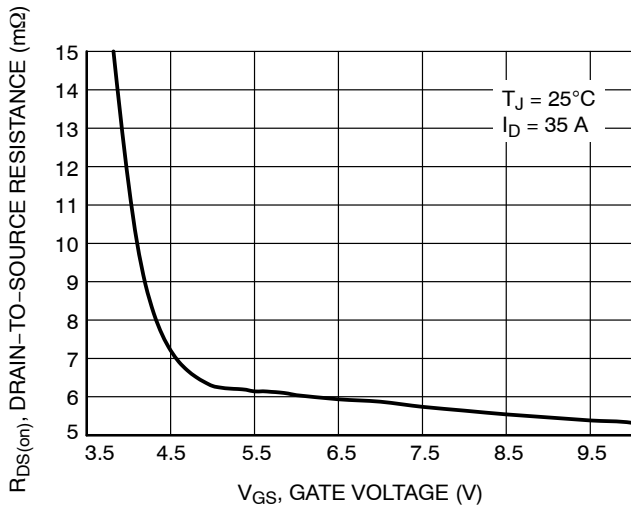


Figure 3. On-Resistance vs. Gate-to-Source Voltage

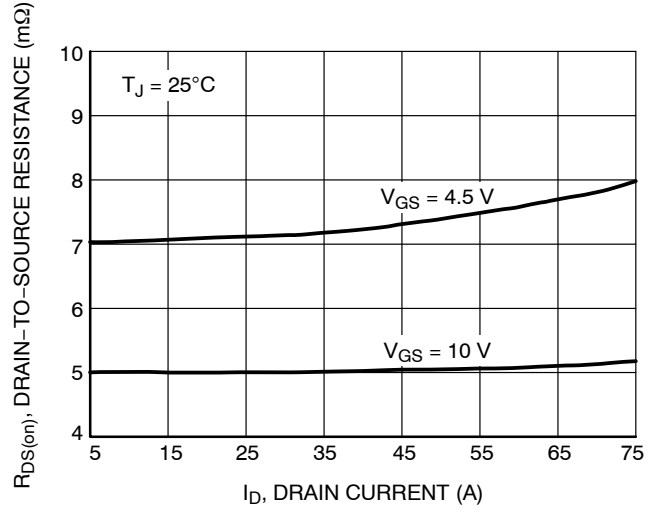


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

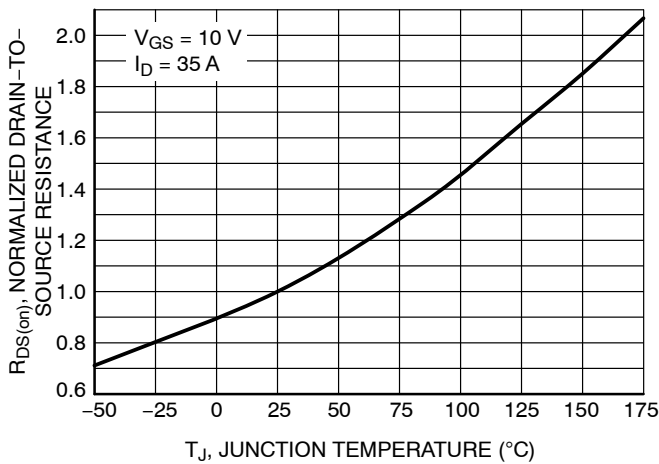


Figure 5. On-Resistance Variation with Temperature

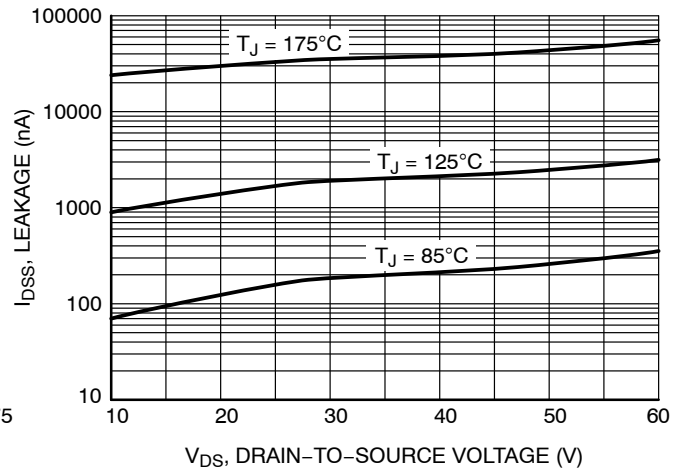
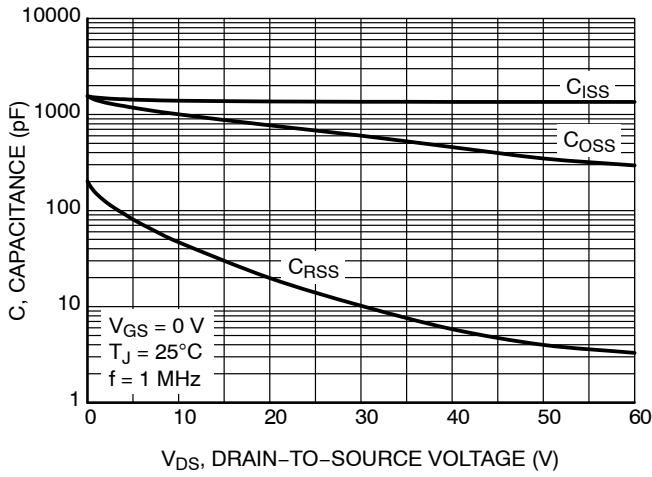


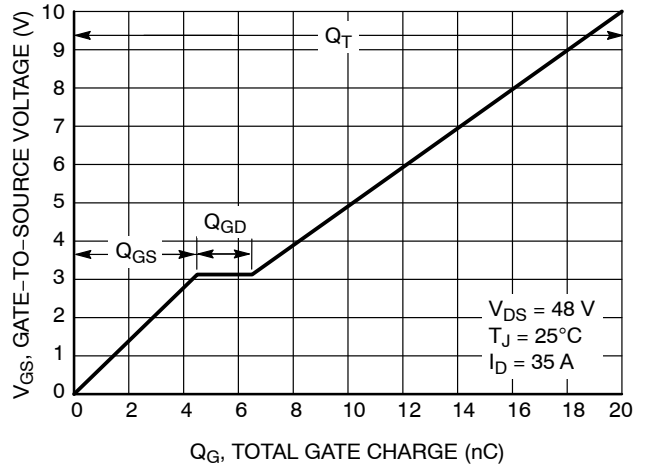
Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NVMFS5C670NL

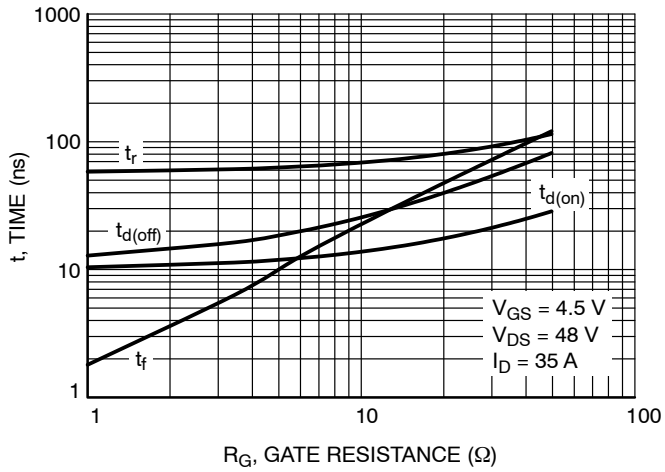
## TYPICAL CHARACTERISTICS (continued)



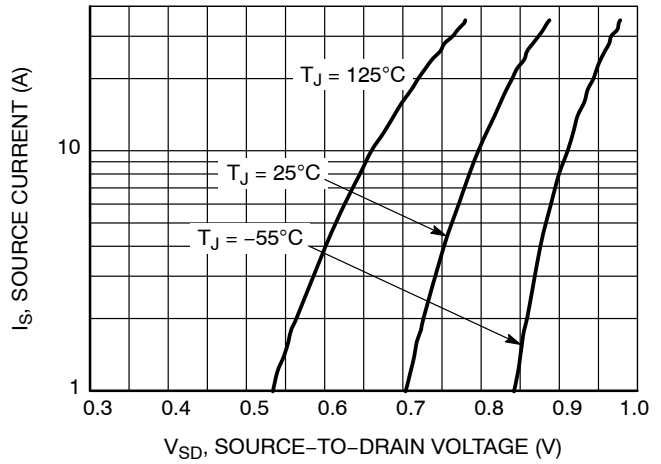
**Figure 7. Capacitance Variation**



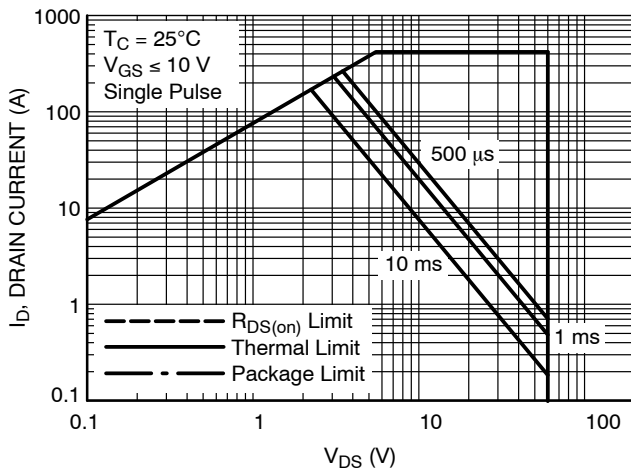
**Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



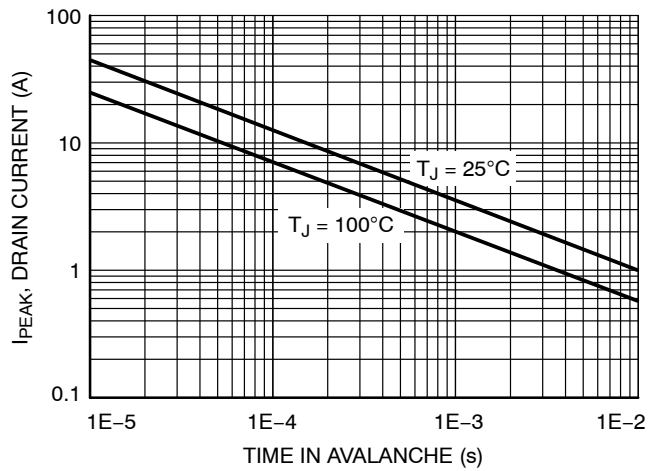
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Diode Forward Voltage vs. Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Drain Current vs. Time in Avalanche**

# NVMFS5C670NL

## TYPICAL CHARACTERISTICS (continued)

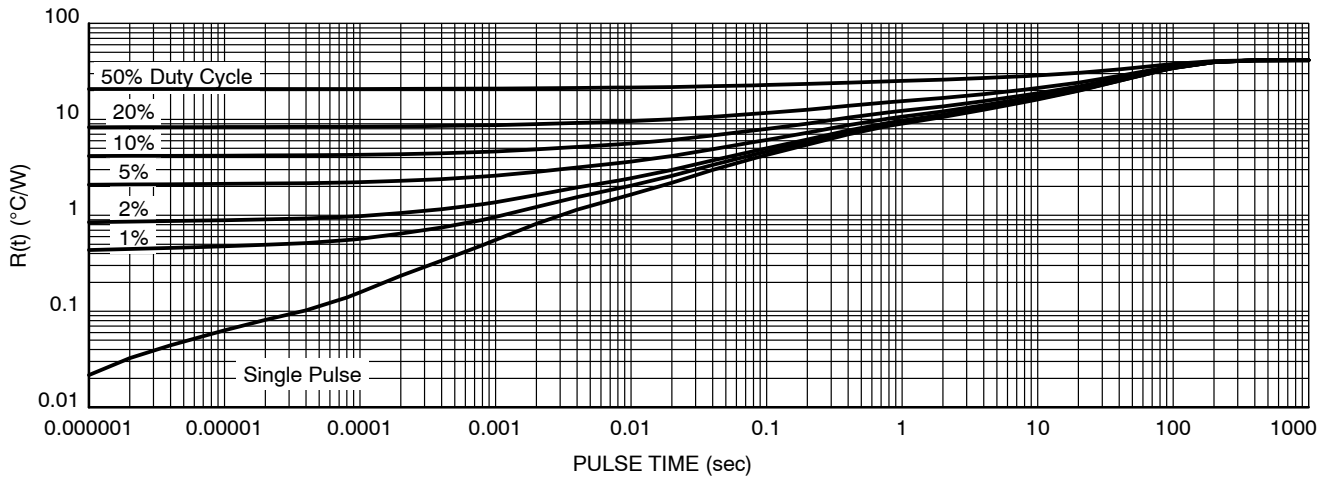


Figure 13. Thermal Characteristics

### DEVICE ORDERING INFORMATION

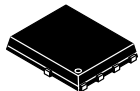
Device	Marking	Package	Shipping <sup>†</sup>
NVMFS5C670NLT1G	5C670L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C670NLAFT1G	5C670L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C670NLAFT1G-YE	5C670L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C670NLWFAFT1G	670LWF	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C670NLWFAFT3G	670LWF	DFNW5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel

### DISCONTINUED (Note 6)

NVMFS5C670NLWFT3G	670LWF	DFNW5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel
NVMFS5C670NLWFT1G	670LWF	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C670NLT3G	5C670L	DFN5 (Pb-Free)	5000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

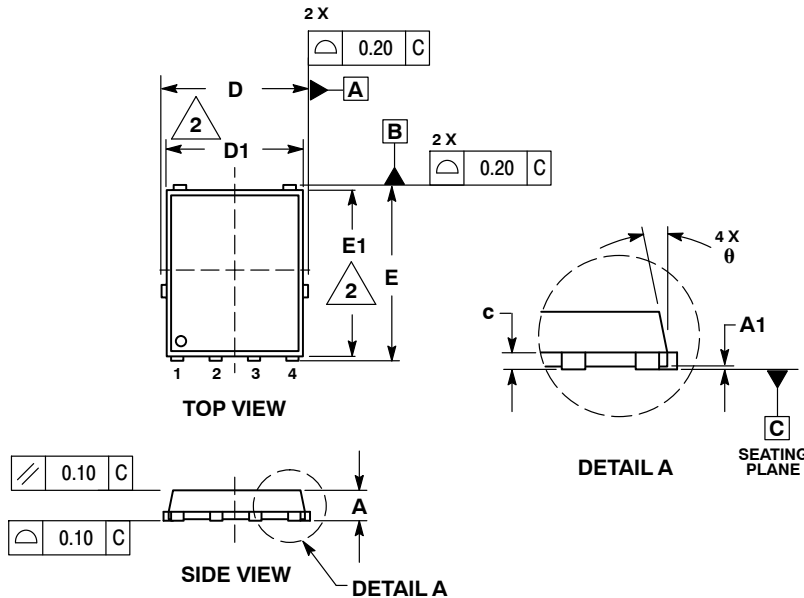
6. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on [www.onsemi.com](http://www.onsemi.com).



1  
SCALE 2:1

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE N

DATE 25 JUN 2018

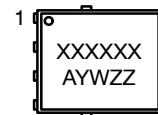


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

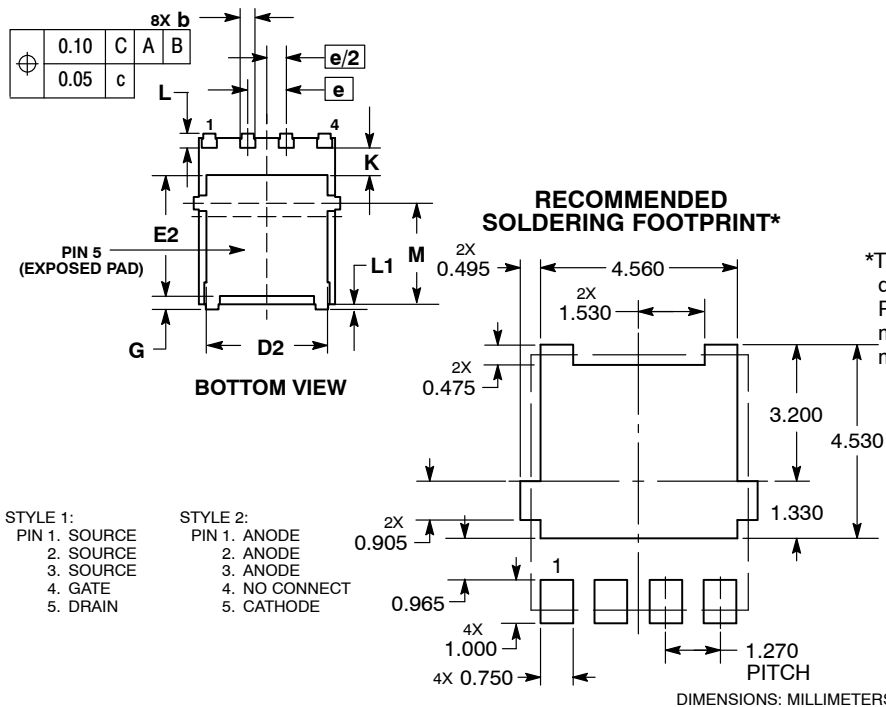
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



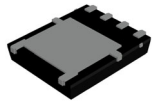
- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN

- STYLE 2:  
PIN 1. ANODE  
2. ANODE  
3. ANODE  
4. NO CONNECT  
5. CATHODE

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

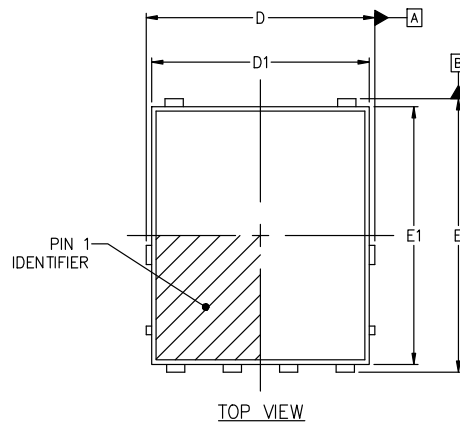
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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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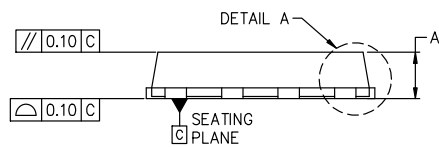


**DFNW5 4.90x5.90x1.00, 1.27P**  
**CASE 507BE**  
**ISSUE B**

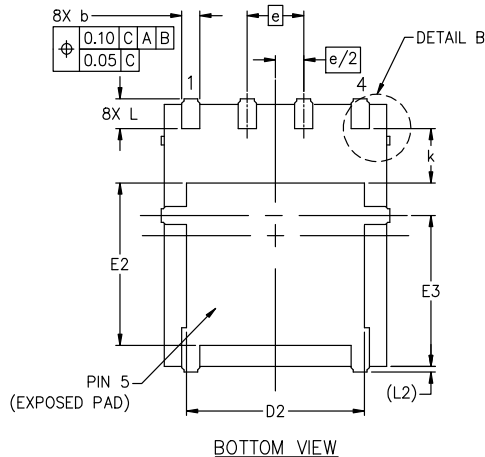
DATE 19 SEP 2024



TOP VIEW

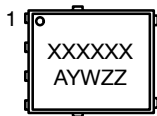


SIDE VIEW



BOTTOM VIEW

**GENERIC MARKING DIAGRAM\***

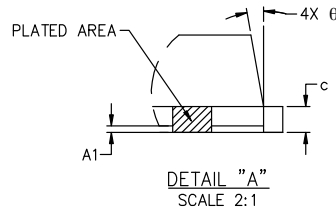


XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 W = Work Week  
 ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

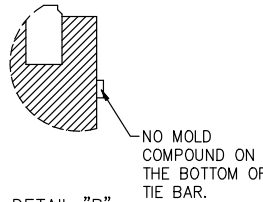
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.



DETAIL "A"  
SCALE 2:1

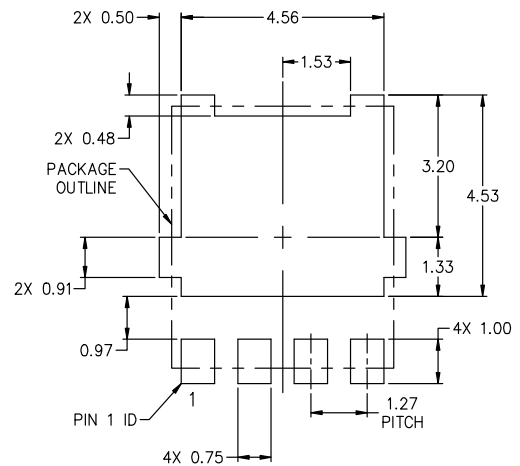


ALTERNATE CONSTRUCTION



DETAIL "B"  
SCALE 2:1

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
theta	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT\*  
 \*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON33319H</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>DFNW5 4.90x5.90x1.00, 1.27P</b>	<b>PAGE 1 OF 1</b>

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onsemi Website: [www.onsemi.com](http://www.onsemi.com)

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