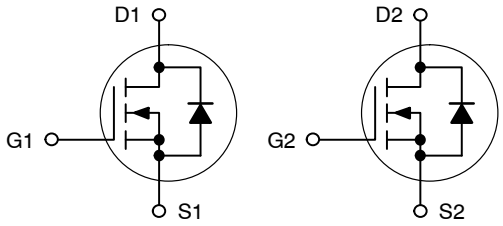
MOSFET - Power, Dual N-Channel, Logic Level, Dual SO8FL
60 V, 39 mΩ, 17 A

NVMFD5877NL

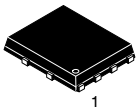
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
60 V	39 mΩ @ 10 V	17 A
	60 mΩ @ 4.5 V	

Dual N-Channel



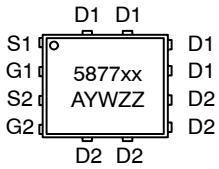
Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFD5877NLWF – Wettable Flanks Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



DFN8 5x6
(SO8FL)
CASE 506BT

MARKING DIAGRAM



5877NL = Specific Device Code for NVMFD5877NL
5877LW = Specific Device Code for NVMFD5877NLWF
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	60	V
Gate-to-Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4)	Steady State	T_{mb} = 25 °C	I_D	17	A
		T_{mb} = 100 °C		12	
Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3)		T_{mb} = 25 °C	P_D	23	W
		T_{mb} = 100 °C		12	
Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 3, 4)	Steady State	T_A = 25 °C	I_D	6	A
		T_A = 100 °C		5	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		T_A = 25 °C	P_D	3.2	W
		T_A = 100°C		1.6	
Pulsed Drain Current	T_A = 25 °C, t_p = 10 μs		I_{DM}	74	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	19	A
Single Pulse Drain-to-Source Avalanche Energy (T_J = 25°C, V_{DD} = 24 V, V_{GS} = 10 V, R_G = 25 Ω)	($I_{L(pk)}$ = 14.5 A, L = 0.1 mH)		E_{AS}	10.5	mJ
	($I_{L(pk)}$ = 6.3 A, L = 2 mH)			40	
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Mounting Board (top) – Steady State (Note 2, 3)	$R_{\Psi J-mb}$	6.5	°C/W
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	47	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				53		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25 °C			1.0	μA
			T_J = 125 °C			10	
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0		3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				3.5		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 7.5 A		31	39	mΩ
		V_{GS} = 4.5 V	I_D = 7.5 A		42	60	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 5.0 A			7.0		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			540		pF
Output Capacitance	C_{oss}				55		
Reverse Transfer Capacitance	C_{rss}				36		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 5.0 A			5.9		nC
Threshold Gate Charge	$Q_{G(TH)}$				0.62		
Gate-to-Source Charge	Q_{GS}				1.64		
Gate-to-Drain Charge	Q_{GD}				2.80		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 48V, I_D = 5.0A			11	20	nC
SWITCHING CHARACTERISTICS (Note 6)							
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 5.0 A, R_G = 2.5 Ω			8.1		ns
Rise Time	t_r				15.8		
Turn-Off Delay Time	$t_{d(off)}$				11.8		
Fall Time	t_f				3.9		
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 5.0 A, R_G = 2.5 Ω			4.9		ns
Rise Time	t_r				6.4		
Turn-Off Delay Time	$t_{d(off)}$				14.5		
Fall Time	t_f				2.4		

5. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 5.0 A	T_J = 25°C		0.8	1.2	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 5.0 A			14.5		ns
Charge Time	t_a				11.5		
Discharge Time	t_b				3.1		
Reverse Recovery Charge	Q_{RR}				11		nC
PACKAGE PARASITIC VALUES							
Source Inductance	L_S	T_A = 25 °C			0.93		nH
Drain Inductance	L_D				0.005		
Gate Inductance	L_G				1.84		
Gate Resistance	R_G				1.5		Ω

5. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

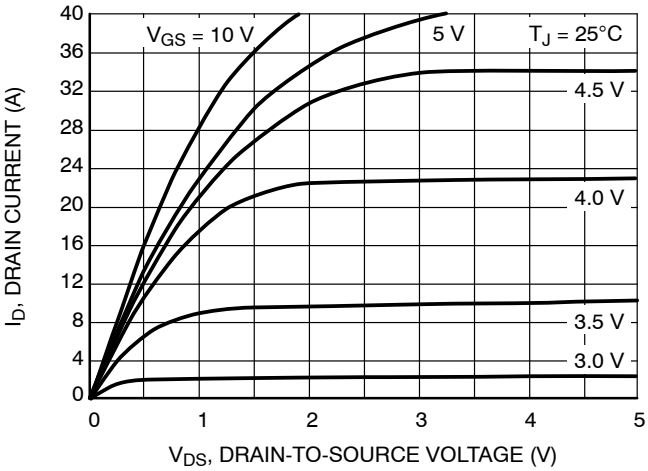


Figure 1. On-Region Characteristics

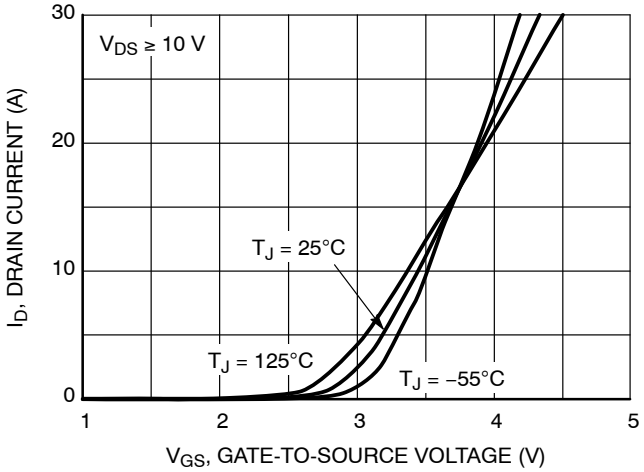


Figure 2. Transfer Characteristics

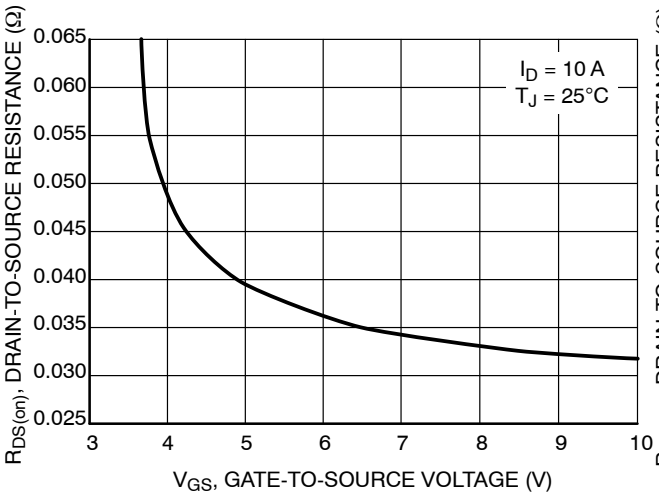


Figure 3. On-Resistance vs. Gate-to-Source Voltage

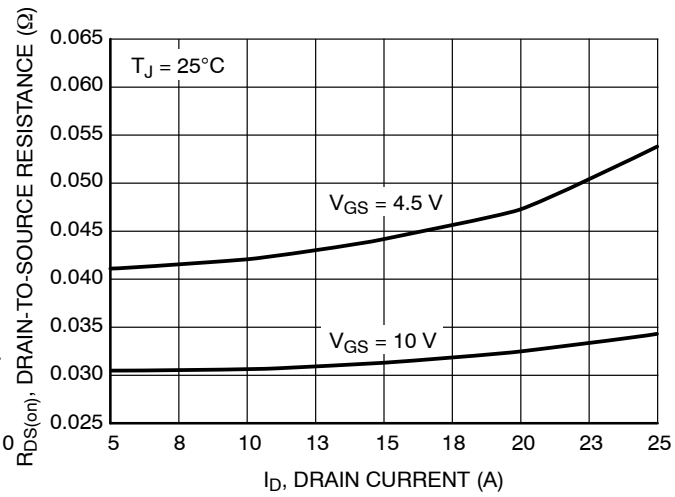


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

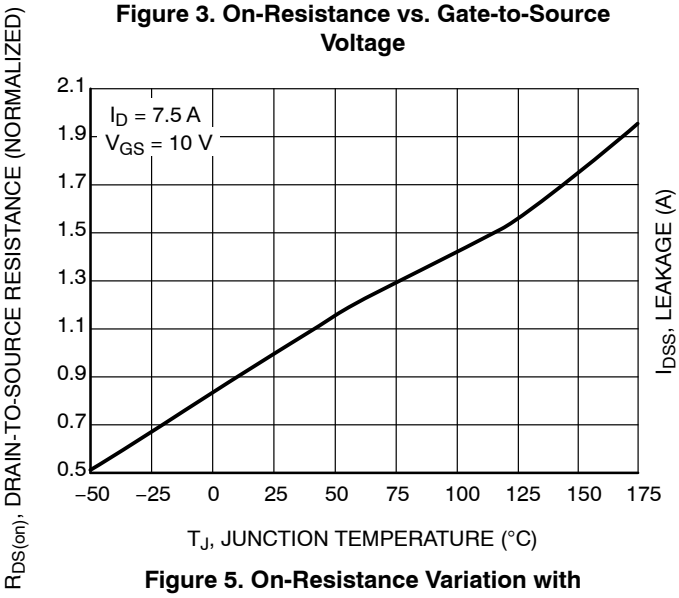


Figure 5. On-Resistance Variation with Temperature

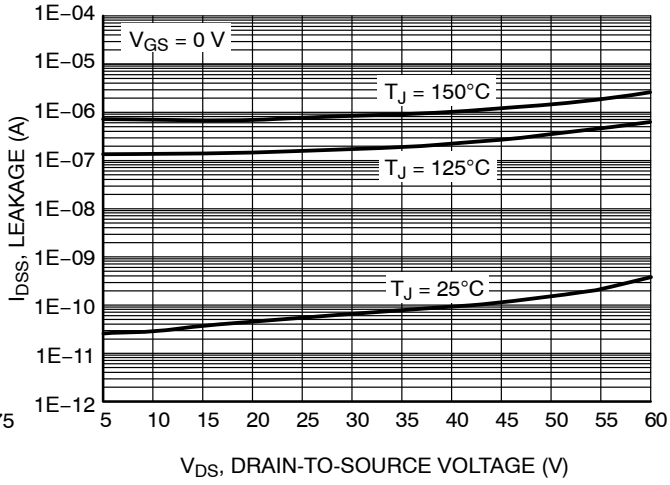


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

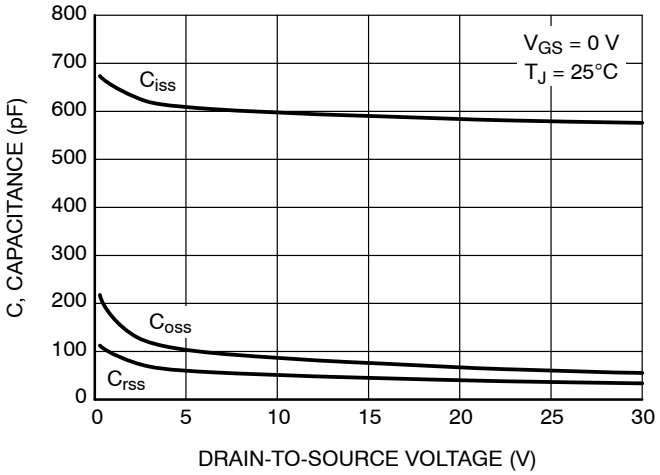


Figure 7. Capacitance Variation

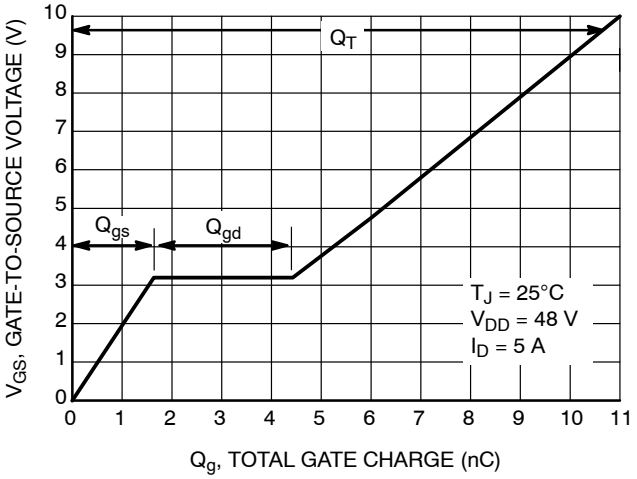


Figure 8. Gate-to-Source vs. Gate Charge

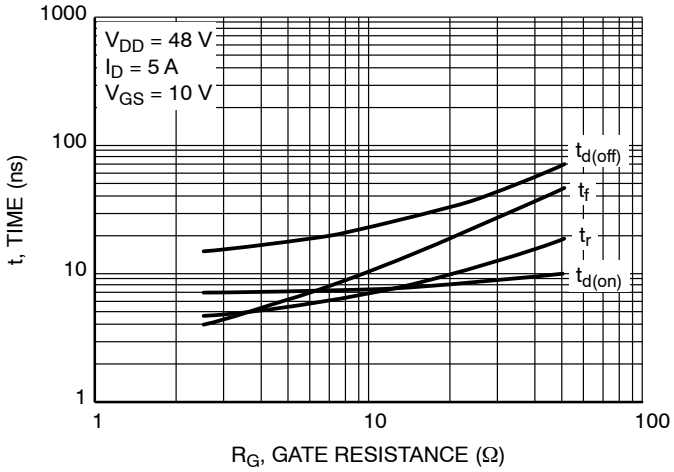


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

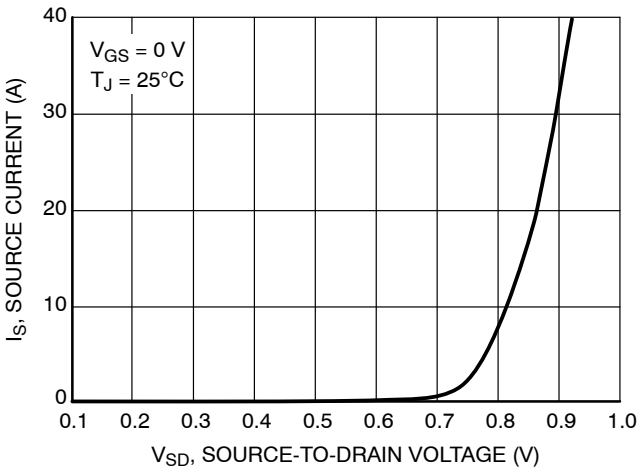


Figure 10. Diode Forward Voltage

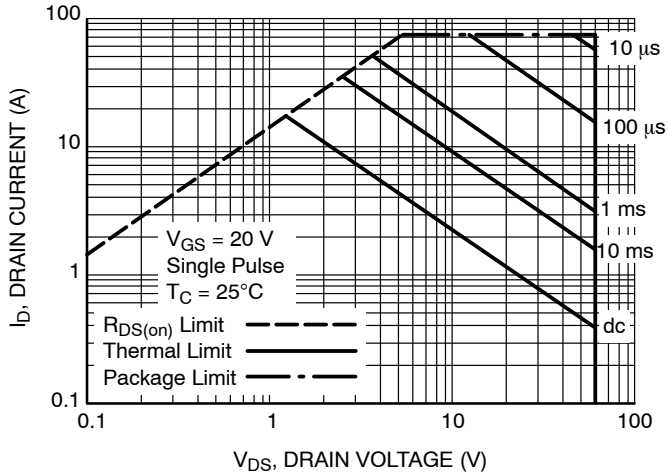


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

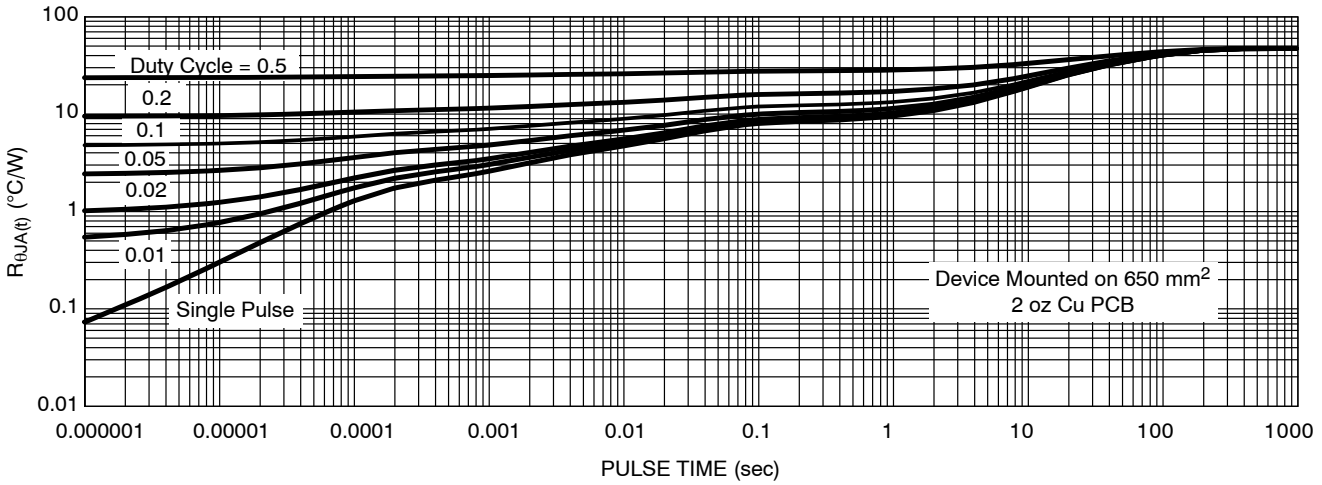


Figure 12. Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFD5877NLWFT1G-UM	5877LW	DFN8 (Pb-Free)	1500 / Tape & Reel

DISCONTINUED (Note 7)

NVMFD5877NLT1G	5877NL	DFN8 (Pb-Free)	1500 / Tape & Reel
NVMFD5877NLWFT1G	5877LW	DFN8 (Pb-Free)	1500 / Tape & Reel
NVMFD5877NLT3G	5877NL	DFN8 (Pb-Free)	5000 / Tape & Reel
NVMFD5877NLWFT3G	5877LW	DFN8 (Pb-Free)	5000 / Tape & Reel

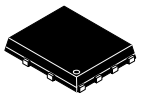
† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

7. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

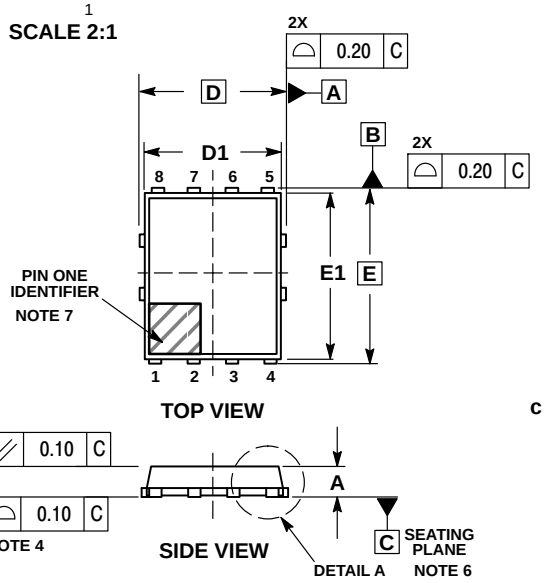
DFN8 5x6, 1.27P Dual Flag (SO8FL−Dual)

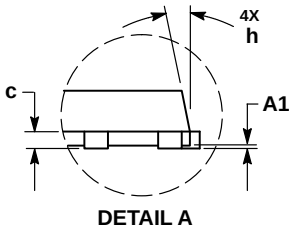
CASE 506BT
ISSUE F

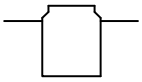
DATE 23 NOV 2021



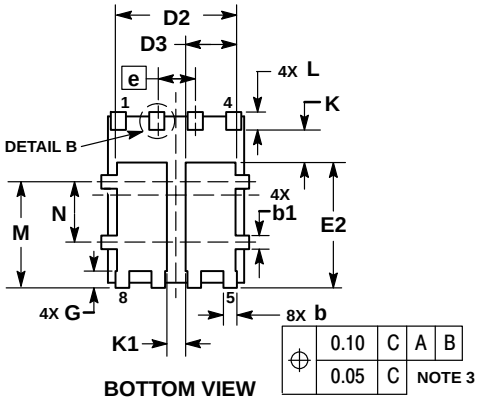
SCALE 2:1







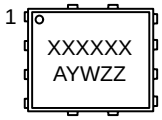
DETAIL B
ALTERNATE CONSTRUCTION



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	–––	1.10
A1	–––	–––	0.05
b	0.33	0.42	0.51
b1	0.33	0.42	0.51
c	0.20	–––	0.33
D		5.15 BSC	
D1	4.70	4.90	5.10
D2	3.90	4.10	4.30
D3	1.50	1.70	1.90
E		6.15 BSC	
E1	5.70	5.90	6.10
E2	3.90	4.15	4.40
e		1.27 BSC	
G	0.45	0.55	0.65
h	–––	–––	12 °
K	0.51	–––	–––
K1	0.56	–––	–––
L	0.48	0.61	0.71
M	3.25	3.50	3.75
N	1.80	2.00	2.20

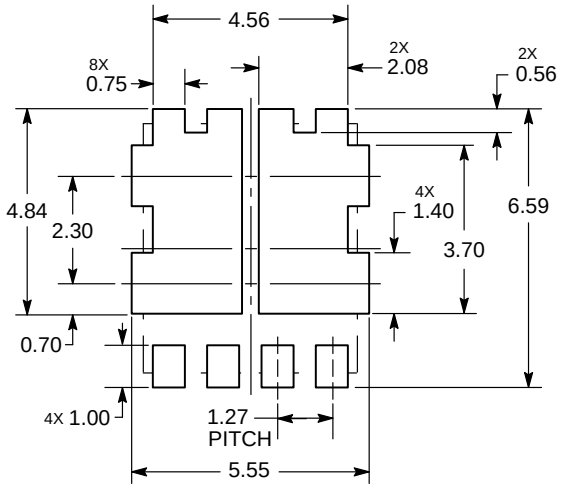
GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON50417E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**DFN8 5X6, 1.27P DUAL FLAG (SO8FL−DUAL)**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales