

MOSFET - Power, Dual N-Channel

100 V, 10.4 mΩ, 61 A

NVMFD010N10MCL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- NVMFD010N10MCL – Wettable Flank Products
- These Devices are Pb-Free, Halogen Free/BFR Free, Beryllium Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	100	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Current R _{θJC} (Note 1)	Steady State	T _C = 25°C	I _D	61	A
		T _C = 100°C		43	
Power Dissipation R _{θJC} (Note 1)	Steady State	T _C = 25°C	P _D	84	W
		T _C = 100°C		42	
Continuous Drain Current R _{θJA} (Notes 1, 2)	Steady State	T _A = 25°C	I _D	11.6	A
		T _A = 100°C		8.2	
Power Dissipation R _{θJA} (Notes 1, 2)	Steady State	T _A = 25°C	P _D	3.1	W
		T _A = 100°C		1.5	
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs		I _{DM}	270	A
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +175	°C
Source Current (Body Diode)			I _S	65	A
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 3.3 A)			E _{AS}	485	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

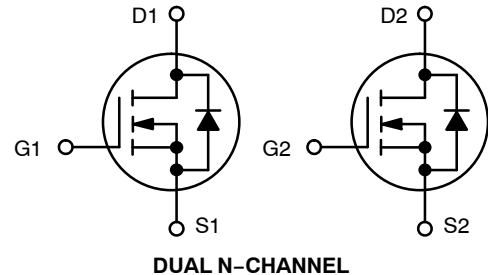
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

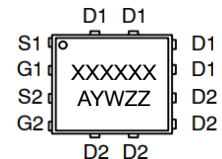
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 1)	$R_{\theta JC}$	1.79	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	49	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using 1 in² pad size, 2 oz. Cu pad.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	10.4 mΩ @ 10 V	61 A
	14.6 mΩ @ 4.5 V	



MARKING DIAGRAM



XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NVMFD010N10MCLT1G	DFN8 (Pb-Free)	1500 / Tape & Reel
NVMFWD010N10MCLT1G (Wettable Flanks)		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NVMFD010N10MCL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C		50.2		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 97\text{ }\mu\text{A}$	1		3	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-5.6		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 17\text{ A}$		8.7	10.4	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 14\text{ A}$		11.7	14.6	
Forward Transconductance	g_{FS}	$V_{DS} = 10\text{ V}, I_D = 17\text{ A}$		60		S

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 50\text{ V}$		1800		pF
Output Capacitance	C_{OSS}			700		
Reverse Transfer Capacitance	C_{RSS}			9.5		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 50\text{ V}, I_D = 14\text{ A}$		12		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 17\text{ A}$		26		
Threshold Gate Charge	$Q_{G(TH)}$			2.4		
Gate-to-Source Charge	Q_{GS}			4.9		
Gate-to-Drain Charge	Q_{GD}			2.7		
Plateau Voltage	V_{GP}			2.7		V

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 17\text{ A}, R_G = 6\text{ }\Omega$		11		ns
Rise Time	t_r			4.2		
Turn-Off Delay Time	$t_{d(OFF)}$			32		
Fall Time	t_f			5.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 17\text{ A}$	$T_J = 25^\circ\text{C}$		0.85	1.3	V
			$T_J = 125^\circ\text{C}$		0.74		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 9\text{ A}$		40			ns
Reverse Recovery Charge	Q_{RR}			31			nC
Charge Time	t_a			19			ns
Discharge Time	t_b			21			nS

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

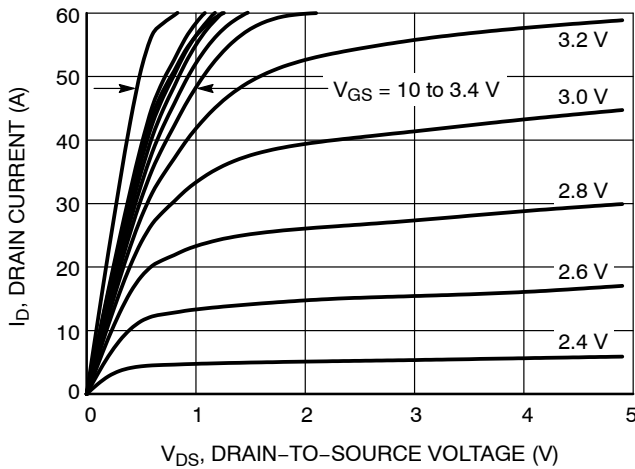


Figure 1. On-Region Characteristics

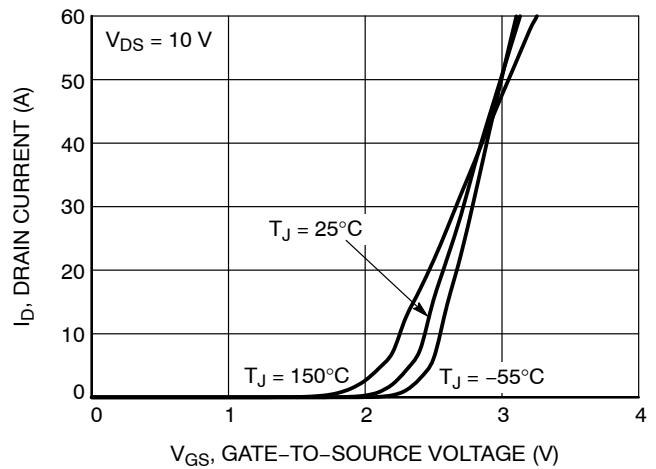


Figure 2. Transfer Characteristics

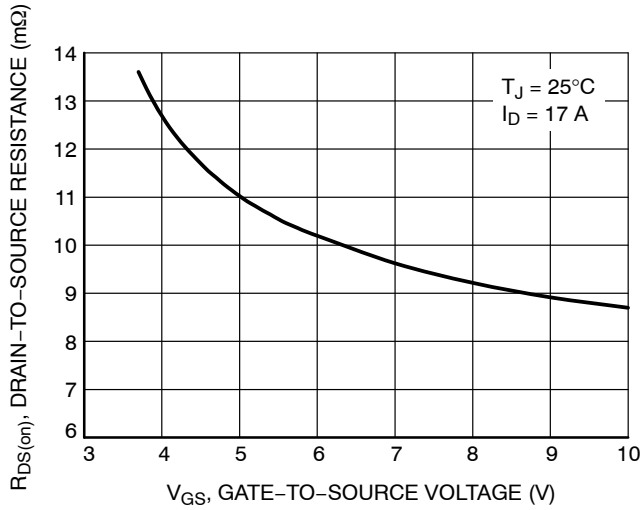


Figure 3. On-Resistance vs. Gate-to-Source Voltage

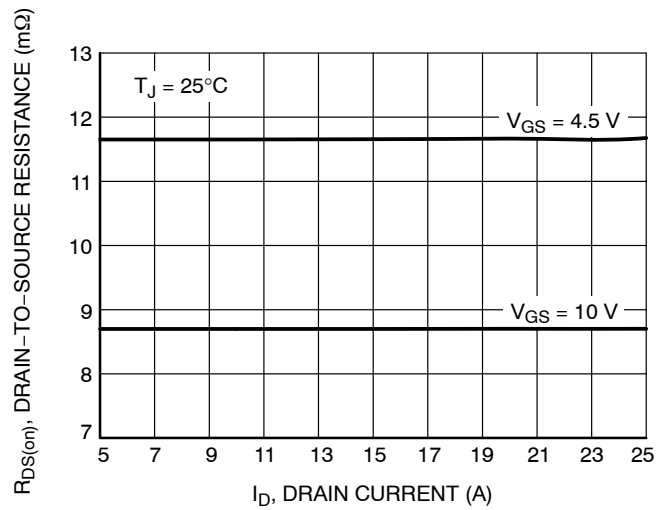


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

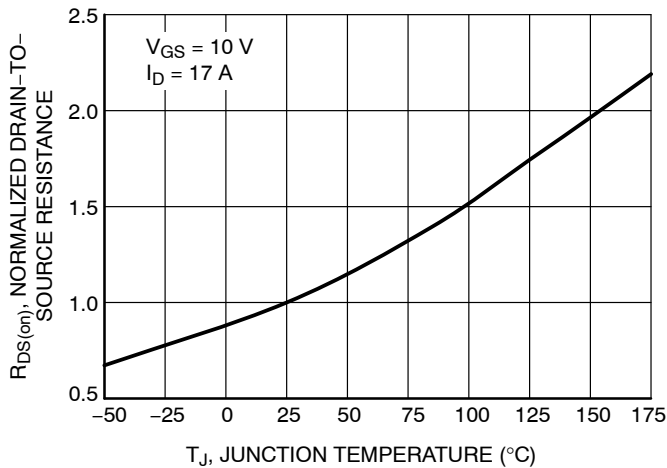


Figure 5. On-Resistance Variation with Temperature

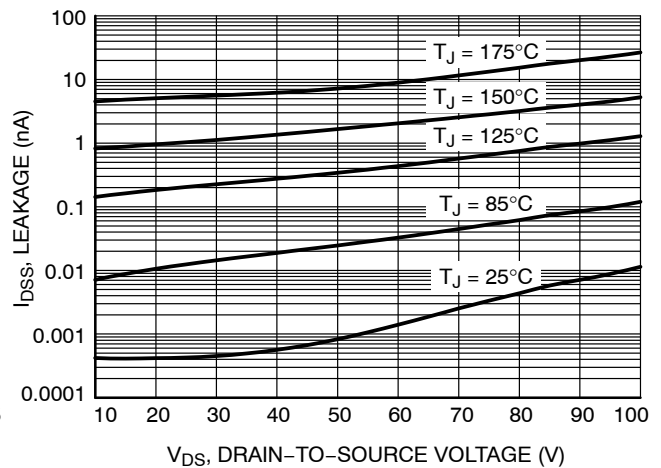


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

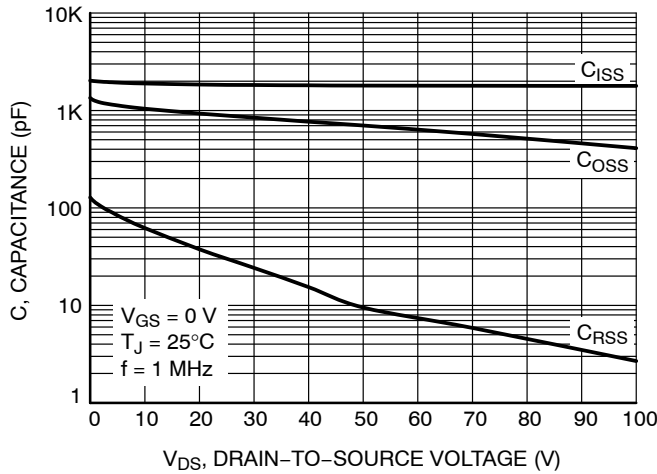


Figure 7. Capacitance Variation

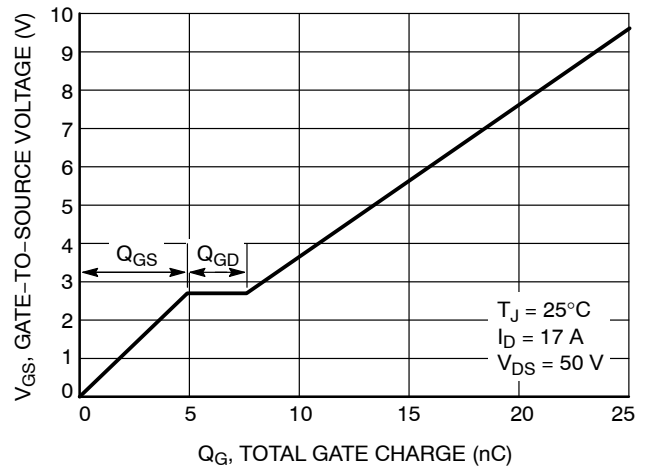


Figure 8. Gate-to-Source Voltage vs. Total Charge

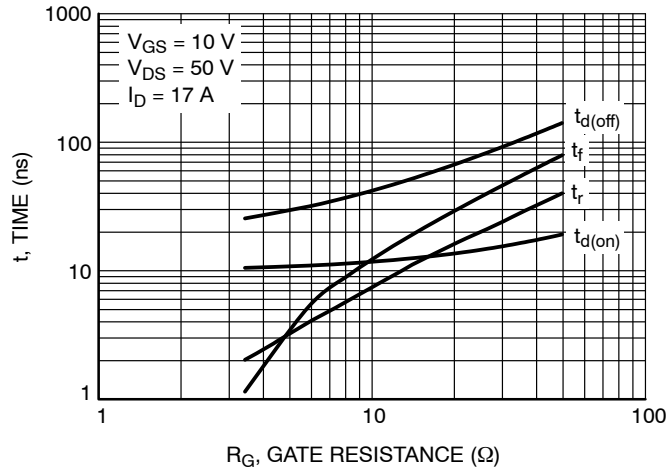


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

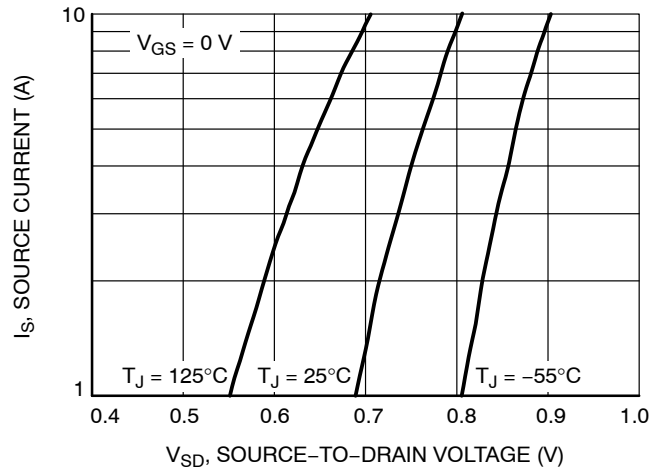


Figure 10. Diode Forward Voltage vs. Current

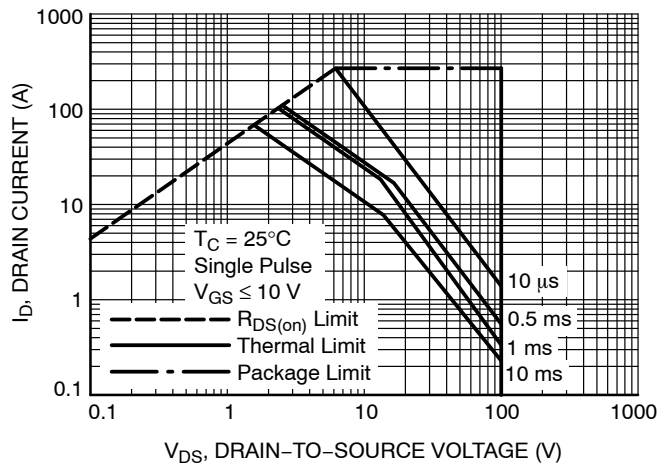


Figure 11. Maximum Rated Forward Biased Safe Operating Area

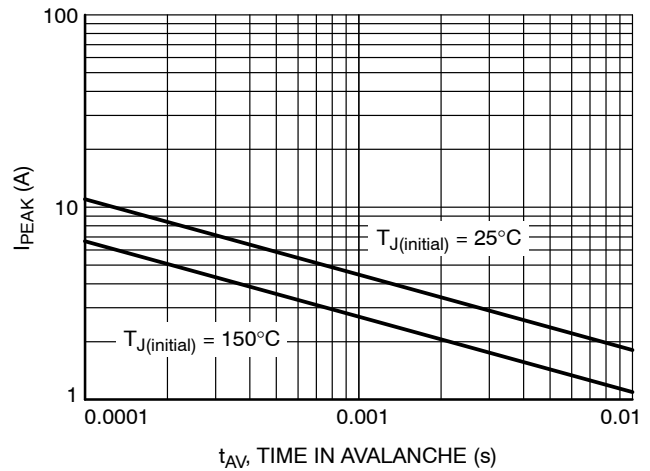


Figure 12. Maximum Drain Current vs. Time in Avalanche

NVMFD010N10MCL

TYPICAL CHARACTERISTICS

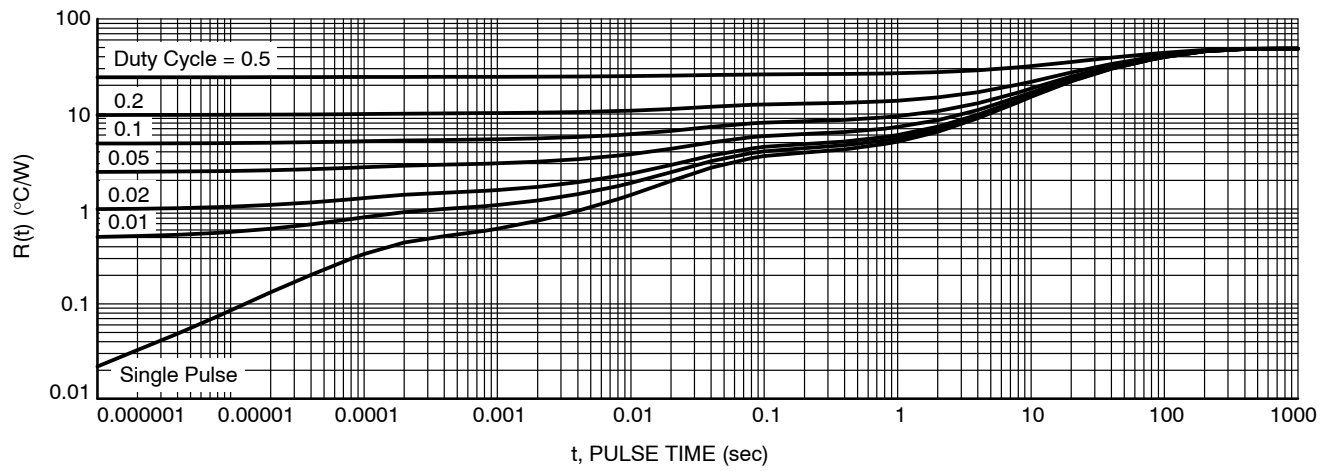


Figure 13. Transient Thermal Impedance

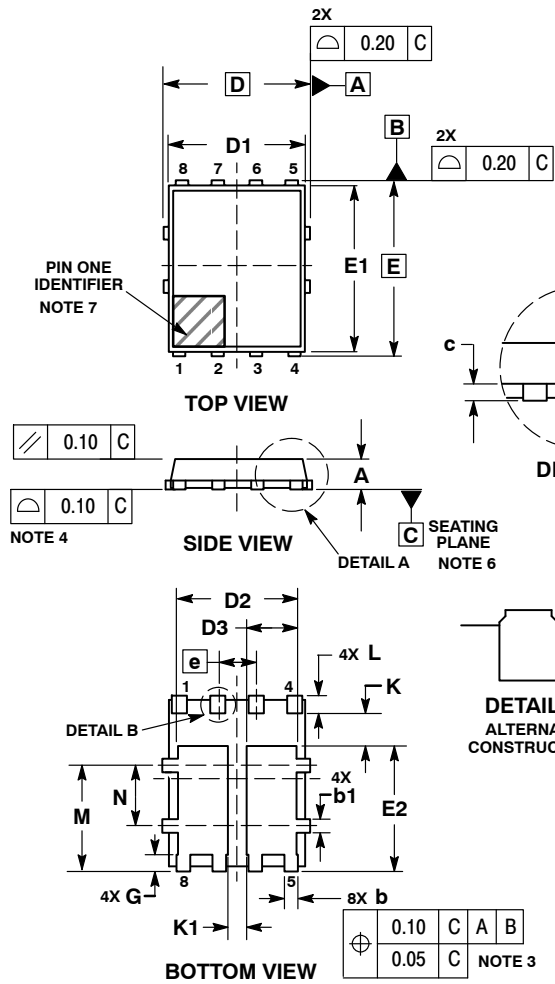
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PACKAGE DIMENSIONS

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)

CASE 506BT

ISSUE E

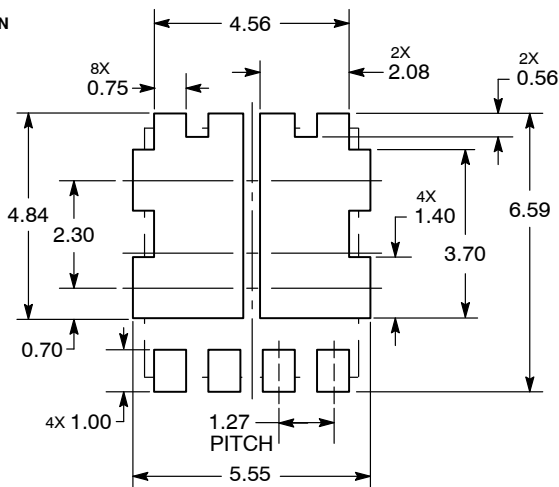


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

DIM	MILLIMETERS		
	MIN	MAX	MAX
A	0.90	---	1.10
A1	---	---	0.05
b	0.33	0.42	0.51
b1	0.33	0.42	0.51
c	0.20	---	0.33
D	5.15 BSC		
D1	4.70	4.90	5.10
D2	3.90	4.10	4.30
D3	1.50	1.70	1.90
E	6.15 BSC		
E1	5.70	5.90	6.10
E2	3.90	4.15	4.40
e	1.27 BSC		
G	0.45	0.55	0.65
h	---	---	12 °
K	0.51	---	---
K1	0.56	---	---
L	0.48	0.61	0.71
M	3.25	3.50	3.75
N	1.80	2.00	2.20

SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NVMFD010N10MCL

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