

# MOSFET – Power, Single N-Channel, SUPERFET® V, FRFET®, TO247-3L 600 V, 55 m $\Omega$ , 45 A NVHL055N60S5F

#### Description

The SUPERFET V MOSFET FRFET series has optimized body diode performance characteristics. This can allow for the removal of components in the application and improve application performance and reliability, particularly when soft switching topologies are used.

#### **Features**

- 650 V @  $T_J = 150^{\circ}$ C / Typ.  $R_{DS(on)} = 44 \text{ m}\Omega$
- 100% Avalanche Tested
- Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### **Applications**

- Electric Vehicle On Board Chargers
- EV Main Battery DC/DC Converters

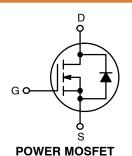
#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

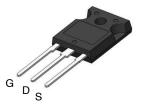
Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	600	٧
Gate-to-Source Voltage	DC	V <sub>GS</sub>	±30	V
	AC (f > 1 Hz)		±30	
Continuous Drain Current	T <sub>C</sub> = 25°C	I <sub>D</sub>	45	Α
	T <sub>C</sub> = 100°C		28	
Power Dissipation	T <sub>C</sub> = 25°C	$P_{D}$	278	W
Pulsed Drain Current	T 05°C	I <sub>DM</sub>	159	Α
Pulsed Source Current (Body Diode)	T <sub>C</sub> = 25°C, t <sub>P</sub> = 10 μs	I <sub>SM</sub>	159	
Operating Junction and Storage Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Source Current (Body Diode)		I <sub>S</sub>	45	Α
Single Pulse Avalanche Energy	$(I_L = 7 A, R_G = 25 \Omega)$	E <sub>AS</sub>	417	mJ
Avalanche Current		I <sub>AS</sub>	7	Α
Repetitive Avalanche Energy (Note 1)		E <sub>AR</sub>	2.78	mJ
MOSFET dv/dt		dvdt	120	V/ns
Peak Diode Recovery dv/dt (Note 2)			70	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T <sub>L</sub>	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2.  $I_{SD} \le 22.5 \text{ A}$ , di/dt  $\le 200 \text{ A/}\mu\text{s}$ ,  $V_{DD} \le 400 \text{ V}$ , starting  $T_J = 25^{\circ}\text{C}$ .

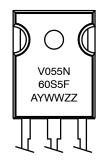
V <sub>DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
600 V	55 mΩ @ 10 V	45 A





TO-247 Long Leads CASE 340CX

#### **MARKING DIAGRAM**



V055N60S5F = Specific Device Code
A = Assembly Location
YWW = Data Code (Year & Week)

ZZ = Assembly Lot

#### **ORDERING INFORMATION**

Device	Package	Shipping
NVHL055N60S5F	TO-247	30 Units / Tube

#### THERMAL RESISTANCE

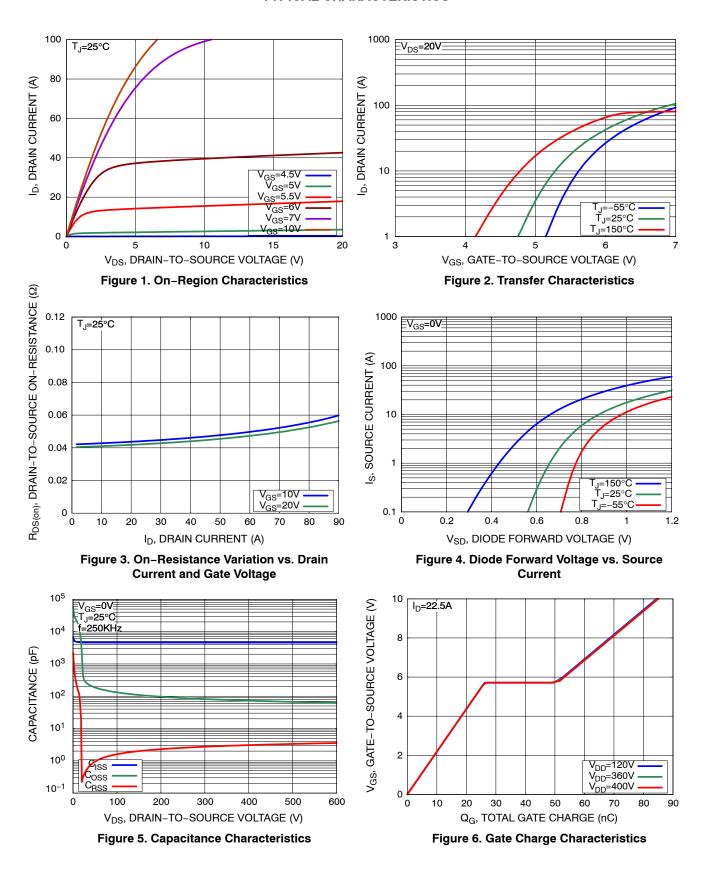
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Max.	$R_{ heta JC}$	0.45	°C/W
Thermal Resistance, Junction-to-Ambient, Max.	$R_{ heta JA}$	40	

# **ELECTRICAL CHARACTERISTICS** (T<sub>1</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V, } I_D = 1 \text{ mA, } T_J = 25^{\circ}\text{C}$	600	-	-	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/$ $\Delta T_J$	I <sub>D</sub> = 10 mA, Referenced to 25°C	-	581	-	mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 600 V, T <sub>J</sub> = 25°C	-	_	10	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V	ı	_	±100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 22.5 A, T <sub>J</sub> = 25°C	-	44	55	mΩ
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{GS} = V_{DS}, I_D = 5.2 \text{ mA}, T_J = 25^{\circ}\text{C}$	3.2	_	4.8	V
Forward Trans-conductance	9FS	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 22.5 A	-	44.8	-	S
CHARGES, CAPACITANCES & GATE	RESISTANCE					
Input Capacitance	C <sub>ISS</sub>	$V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V}, f = 250 \text{ kHz}$	-	4603	-	pF
Output Capacitance	C <sub>OSS</sub>		-	72.9	-	
Time Related Output Capacitance	C <sub>OSS(tr.)</sub>	$I_D$ = Constant, $V_{DS}$ = 0 V to 400 V, $V_{GS}$ = 0 V	-	1114	-	
Energy Related Output Capacitance	C <sub>OSS(er.)</sub>	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	-	125	-	
Total Gate Charge	Q <sub>G(tot)</sub>	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 22.5 A, V <sub>GS</sub> = 10 V	-	85.2	-	nC
Gate-to-Source Charge	$Q_{GS}$		-	26.2	-	
Gate-to-Drain Charge	$Q_{GD}$		-	24.9	-	
Gate Resistance	$R_{G}$	f = 1 MHz	-	4.32	-	Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{GS} = 0/10 \text{ V}, V_{DD} = 400 \text{ V},$	-	44	_	ns
Rise Time	t <sub>r</sub>	$I_D = 22.5 \text{ A}, R_G = 4.7 \Omega$	-	26.2	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	108	-	
Fall Time	t <sub>f</sub>		-	2.6	_	
SOURCE-TO-DRAIN DIODE CHARAC	TERISTICS					
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0 \text{ V}, I_{SD} = 22.5 \text{ A}, T_J = 25^{\circ}\text{C}$	-	_	1.2	V
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 22.5 A,	_	128	_	ns
Reverse Recovery Charge	Q <sub>RR</sub>	dI/dt = 100 A/μs, V <sub>DD</sub> = 400 V	_	758	_	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### **TYPICAL CHARACTERISTICS**



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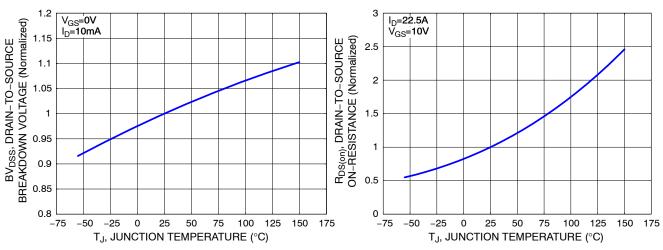


Figure 7. Breakdown Voltage Variation vs. Temperature

Figure 8. On–Resistance Variation vs.
Temperature

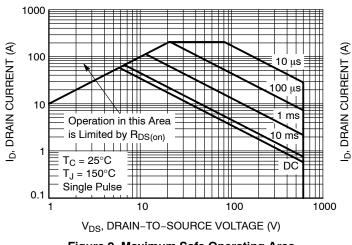


Figure 9. Maximum Safe Operating Area

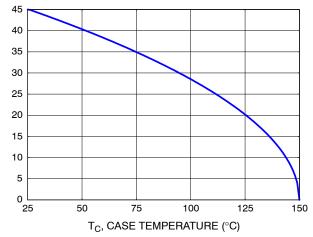


Figure 10. Maximum Drain Current vs. Case Temperature

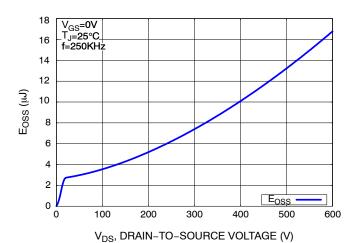


Figure 11. E<sub>OSS</sub> vs. Drain-to-Source Voltage

## **TYPICAL CHARACTERISTICS**

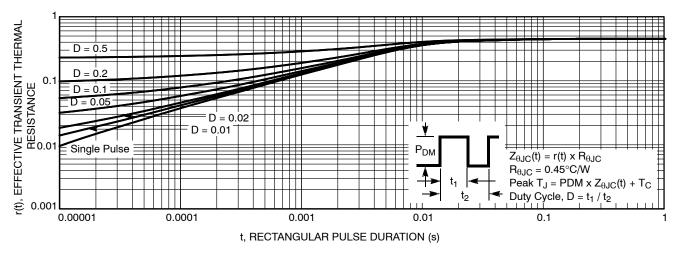


Figure 12. Transient Thermal Impedance

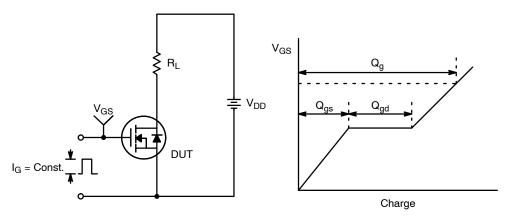


Figure 13. Gate Charge Test Circuit & Waveform

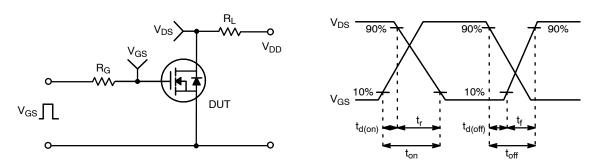


Figure 14. Resistive Switching Test Circuit & Waveforms

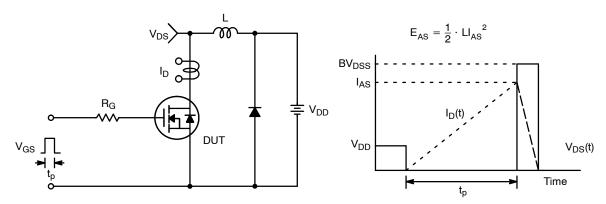


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

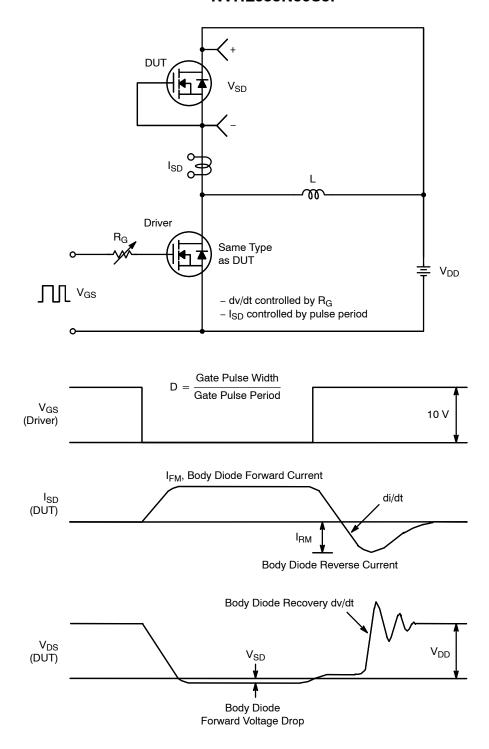
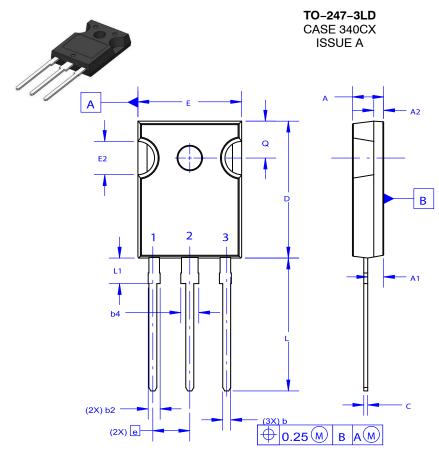


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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**DATE 06 JUL 2020** 





NOTES: UNLESS OTHERWISE SPECIFIED.

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- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

# GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code A = Assembly Location

Y = Year
WW = Work Week

WW = Work Week
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " •", may or may not be present. Some products may not follow the Generic Marking.

Ø <sub>P</sub> —		Φ <sub>P1</sub> D2
E1 —	2	D1

DIM	MILLIMETERS		
DIM	MIN	NOM	MAX
Α	4.58	4.70	4.82
<b>A</b> 1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
Е	15.37	15.62	15.87
E2	4.96	5.08	5.20
е	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
ØΡ	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
С	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
ØP1	6.60	6.80	7.00

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