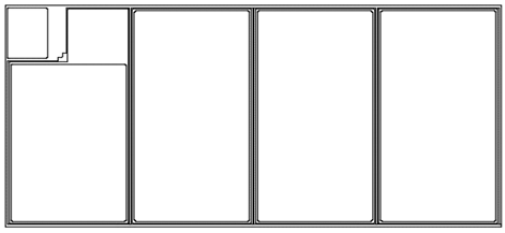
MOSFET – Power, N-Channel

100 V, 4.0 mΩ

NVCR4LS004N10MCA



Features

- Typical $R_{DS(on)}$ = 3.2 mΩ at V_{GS} = 10 V
- Typical $Q_{g(tot)}$ = 47 nC at V_{GS} = 10 V
- AEC−Q101 Qualified
- RoHS Compliant

DIMENSION (μm)

Die Size	4953 × 2413
Die Size (Sawn)	4933 ±15 × 2393 ±15
Source Attach Area	1114.8 × 1648.9, (1114.8 × 2205.8) × 3
Gate Attach Area	385 × 535
Die Thickness	101.6 ±19.1

Gate and Source: AlSiCu
Drain: Ti−NiV−Ag (back side of die)
Passivation: Polyimide
Wafer Diameter: 8 inch
Wafer Sawn on UV Tape
Bad Dice Identified in Inking
Gross Die Counts: 2113

ORDERING INFORMATION

Device	Package
NVCR4LS004N10MCA	Wafer Sawn on Foil

RECOMMENDED STORAGE CONDITIONS

Temperature	22 to 28°C
RH	40 to 66%

The Chip is 100% Probed to Meet the Conditions and Limits Specified at T_J = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} = 100 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	–	4.0	V
*$R_{DS(on)}$	Bare Die Drain to Source On Resistance	I_D = 5 A, V_{GS} = 10 V	–	3.2	4.0	mΩ
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 5 A, V_{GS} = 0 V	–	–	1.2	V
E_{AS}	Single Pulse Drain−to−Source Avalanche Energy	L = 30 μH, I_{AS} = 79 A	93.6	–	–	mJ

*Accurate $R_{DS(on)}$ test at die level is not feasible for this thin die as limited by the test contact precision attainable in a die form. The max $R_{DS(on)}$ specification is defined from the historical performance of the die in package but is not guaranteed by test in production. The die $R_{DS(on)}$ performance depends on the Source wire/ribbon bonding layout.

MOSFET MAXIMUM RATINGS in Reference to the FDBL86066−F085 electrical data in TOLL
(T_J = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (V_{GS} = 10) (Note 1) T_C = 25°C T_C = 100°C	 184 130	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	93.6	mJ
P_D	Power Dissipation $R_{\theta JC}$	300	W
	Derate Above 25°C	2	W/°C
T_J, T_{STG}	Operating and Storage Temperature	−55 to +175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.5	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by silicon.
2. Starting T_J = 25°C, L = 30 μH, I_{AS} = 79 A, V_{DD} = 100 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

ELECTRICAL CHARACTERISTICS in Reference to the FDBL86066−F085 electrical data in TOLL
(T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		100	–	–	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} = 100 V, V_{GS} = 0 V	T_J = 25°C	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		2.0	–	4.0	V
$R_{DS(on)}$	Drain to Source on Resistance	I_D = 80 A, V_{GS} = 10 V	T_J = 25°C	–	3.3	4.1	mΩ
			T_J = 175°C (Note 4)	–	7.3	8.8	mΩ
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		–	3240	–	pF
C_{oss}	Output Capacitance			–	1950	–	pF
C_{rss}	Reverse Transfer Capacitance			–	26	–	pF
R_g	Gate Resistance	f = 1 MHz		–	0.5	–	Ω
$Q_{g(ToT)}$	Total Gate Charge	V_{GS} = 0 to 10 V, V_{DD} = 50 V, I_D = 80 A		–	47	–	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2 V, V_{DD} = 50 V, I_D = 80 A		–	6	–	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 50 V, I_D = 80 A		–	15	–	nC
Q_{gd}	Gate to Drain “Miller” Charge			–	10	–	nC
SWITCHING CHARACTERISTICS							
$t_{d(on)}$	Turn−On Delay	V_{DD} = 50 V, I_D = 80 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		–	18	–	ns
t_r	Rise Time			–	9	–	ns
$t_{d(off)}$	Turn−Off Delay			–	36	–	ns
t_f	Fall Time			–	13	–	ns
DRAIN−SOURCE DIODE CHARACTERISTIC							
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 80 A, V_{GS} = 0 V		–	–	1.25	V
		I_{SD} = 40 A, V_{GS} = 0 V		–	–	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 80 A, dI_{SD}/dt = 1000 A/μs		–	32	–	ns
Q_{rr}	Reverse Recovery Charge			–	243	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

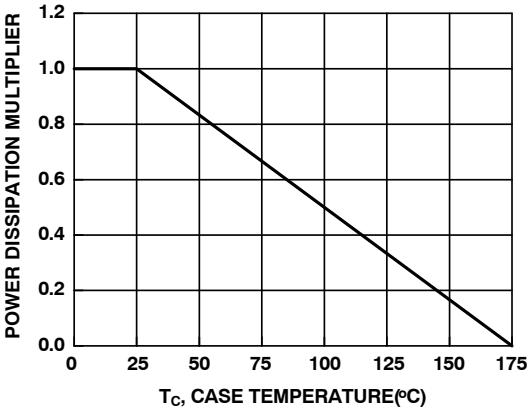


Figure 1. Normalized Power Dissipation vs. Case Temperature

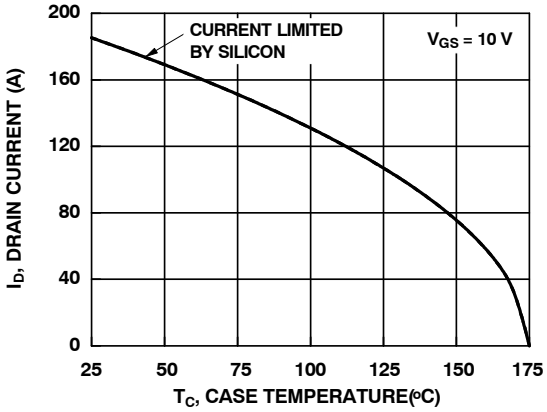


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

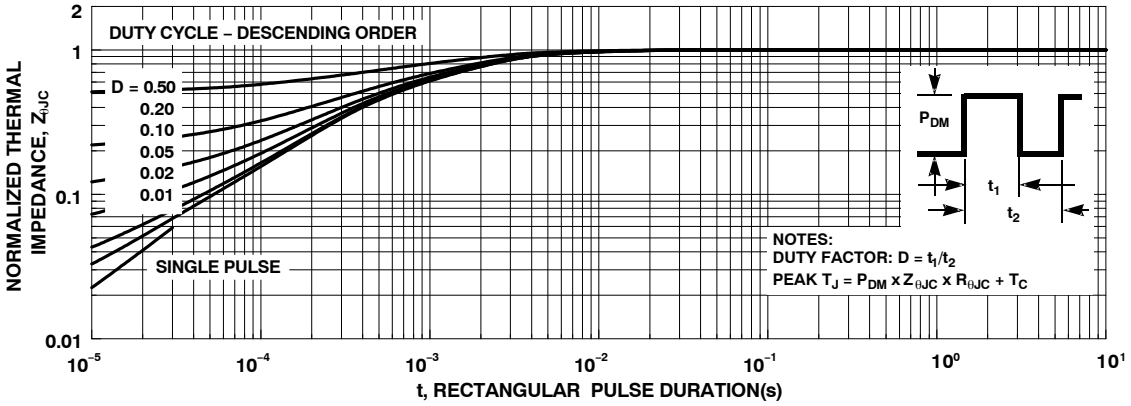


Figure 3. Normalized Maximum Transient Thermal Impedance

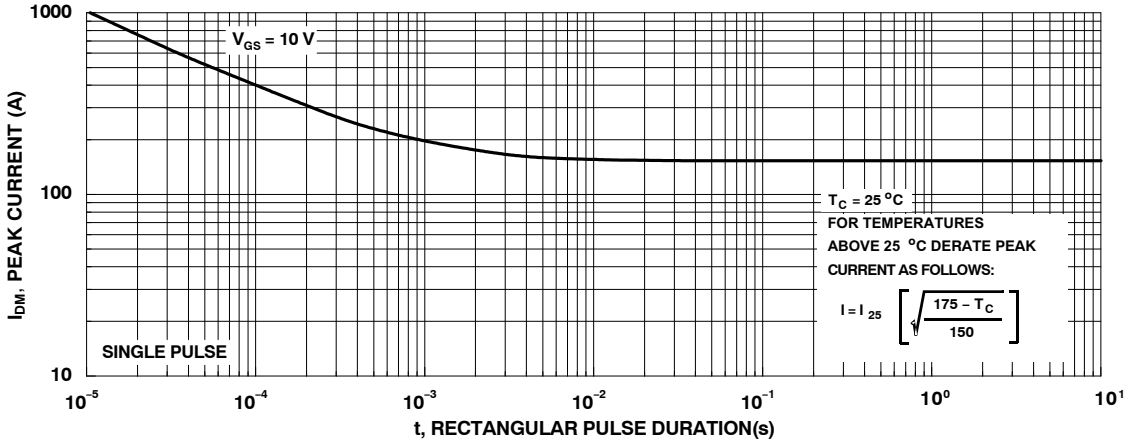


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

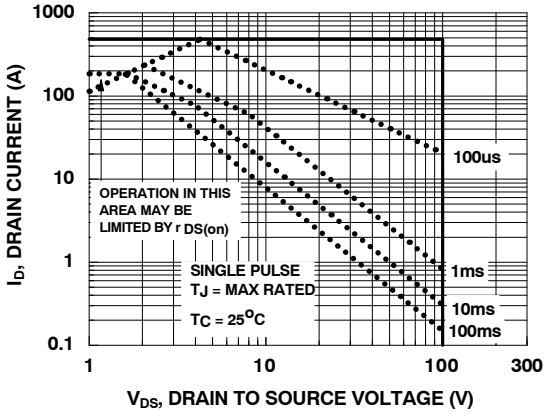


Figure 5. Forward Bias Safe Operating Area

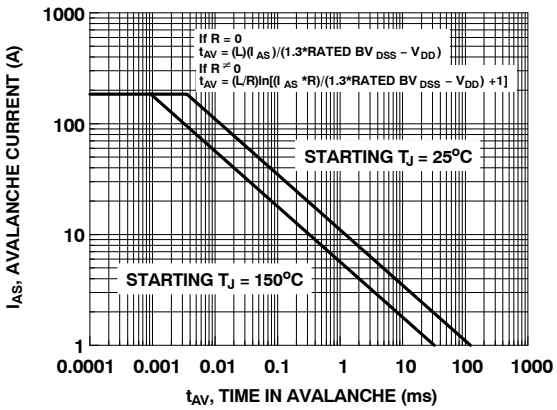


Figure 6. Unclamped Inductive Switching Capability

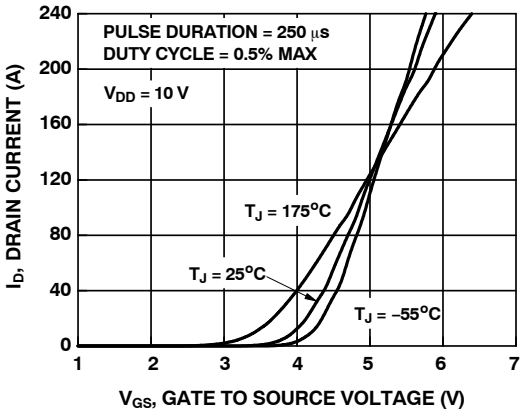


Figure 7. Transfer Characteristics

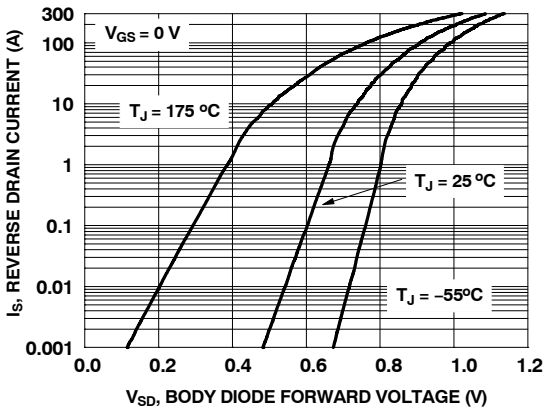


Figure 8. Forward Diode Characteristics

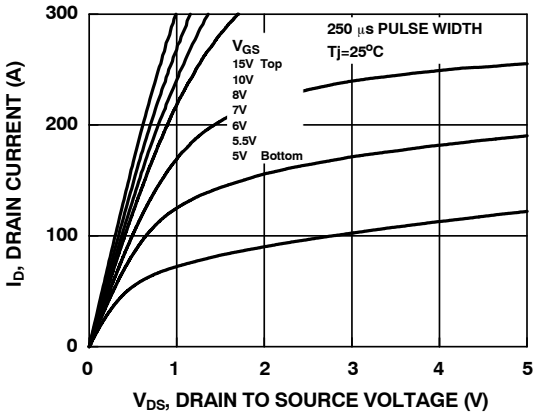


Figure 9. Saturation Characteristics

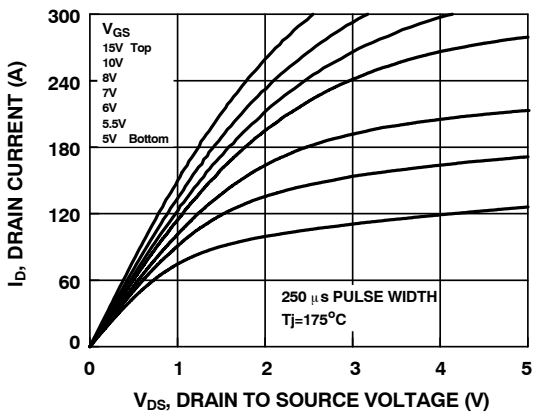


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

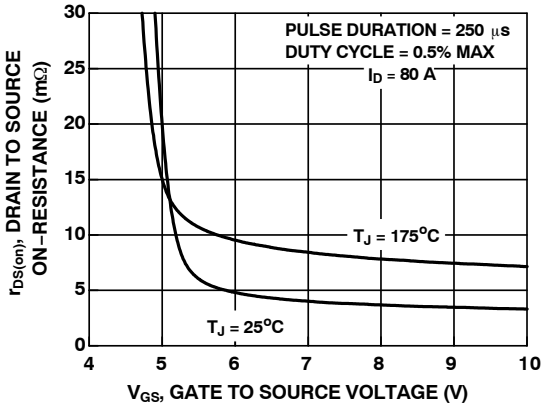


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

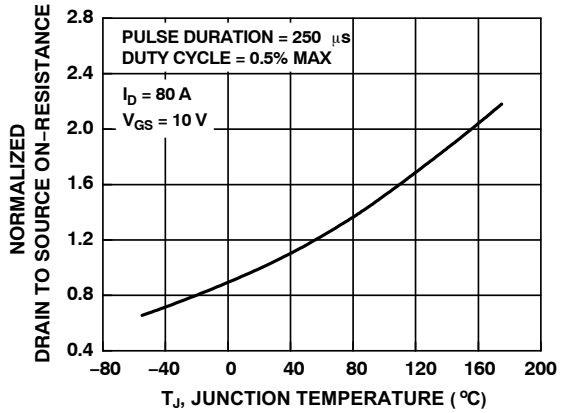


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

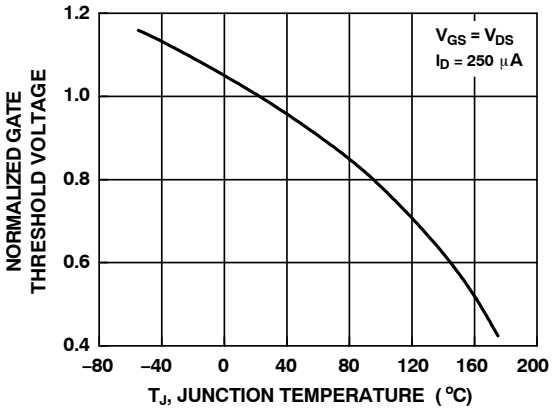


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

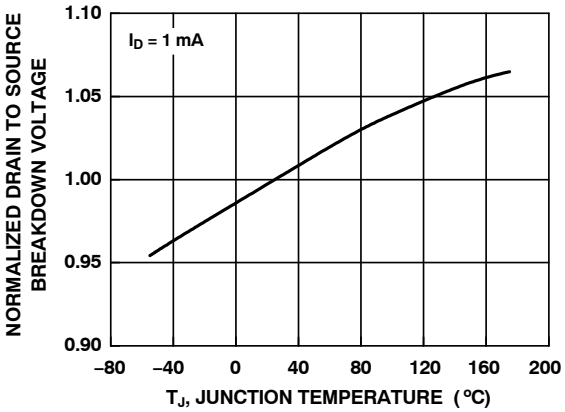


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

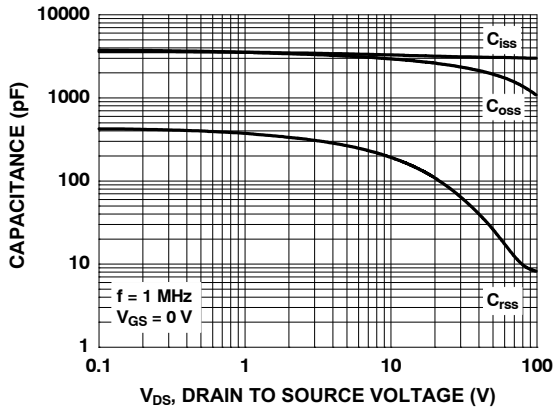


Figure 15. Capacitance vs. Drain to Source Voltage

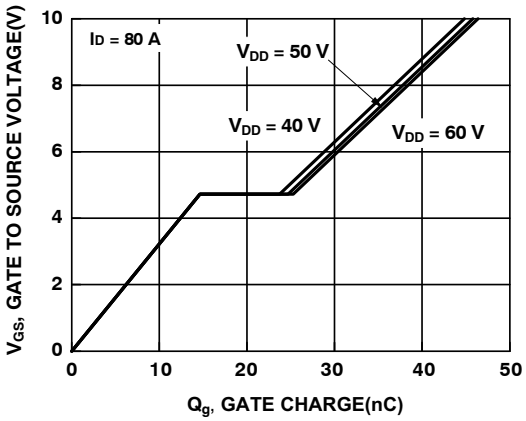


Figure 16. Gate Charge vs. Gate to Source Voltage

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales