Onsemi

MOSFET - Power, Single N-Channel, D2PAK-7L 650 V, 95 mΩ, 36 A

NVBG095N65S3F

Description

SUPERFET[®] III MOSFET is onsemi's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency. SUPERFET III FRFET® MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

In addition, the D2PAK 7 lead package offers Kelvin sense. This allows higher switching speeds and gives designers the ability to reduce the overall application footprint.

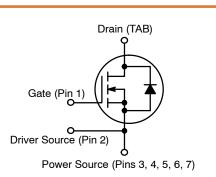
Features

- 700 V @ $T_J = 150^{\circ}C$
- Typ. $R_{DS(on)} = 78 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 66 \text{ nC}$)
- Low Effective Output Capacitance (Typ. Coss(eff.) = 597 pF)
- 100% Avalanche Tested
- AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Automotive On Board Charger
- Automotive DC/DC Converter for BEV

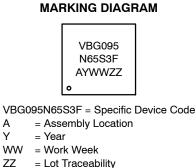
V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
650 V	95 mΩ @ 10 V	36 A



N-CHANNEL MOSFET



D2PAK-7L CASE 418BJ



ORDERING INFORMATION

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See detailed ordering and shipping information on page 6 of this data sheet

Symbol	Parameter		Value	Unit
V _{DSS}	Drain-to-Source Voltage		650	V
V _{GSS}	Gate-to-Source Voltage	– DC	±30	V
		– AC (f > 1 Hz)	±30	
ID	Drain Current	– Continuous (T _C = 25°C)	36	А
		– Continuous (T _C = 100°C)	22.8	
I _{DM}	Drain Current	– Pulsed (Note 1)	90	А
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		440	mJ
I _{AS}	Avalanche Current (Note 2)		4.6	A
E _{AR}	Repetitive Avalanche Energy (Note 1)		2.72	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
PD	Power Dissipation	(T _C = 25°C)	272	W
		- Derate Above 25°C	2.176	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
ΤL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	°C

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality shows be assumed, damage may occur and reliability may be affected. 1. Repetitive rating: pulse-width limited by maximum junction temperature. 2. $I_{AS} = 4.6 \text{ A}, R_G = 25 \Omega$, starting $T_J = 25^{\circ}\text{C}$. 3. $I_{SD} \le 18 \text{ A}, \text{ di/dt} \le 200 \text{ A/}\mu\text{s}, \text{ V}_{DD} \le 400 \text{ V}, \text{ starting } T_J = 25^{\circ}\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{ extsf{ heta}JC}$	Thermal Resistance, Junction-to-Case, Max.	0.46	°C/W
$R_{ heta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	

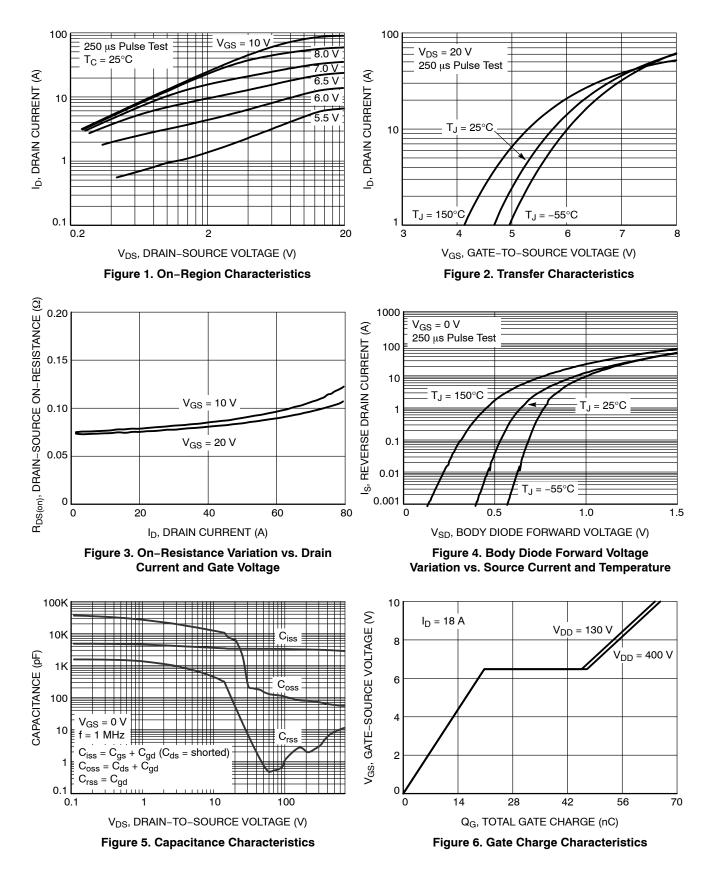
ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
OFF CHARAC	TERISTICS			•		
BV _{DSS}	Drain-to-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650			V
		V_{GS} = 0 V, I_D = 10 mA, T_J = 150°C	700			V
$\Delta \text{BV}_{\text{DSS}} / \Delta \text{T}_{\text{J}}$	Breakdown Voltage Temperature Coefficient	I_D = 15 mA, Referenced to 25°C		640		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V			10	μΑ
		V_{DS} = 520 V, T_C = 125°C		12		
I _{GSS}	Gate-to-Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACT	ERISTICS					
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 0.86$ mA	3.0		5.0	V
R _{DS(on)}	Static Drain-to-Source On Resistance	V_{GS} = 10 V, I _D = 18 A		78	95	mΩ
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 18 A		19		S
DYNAMIC CHA	ARACTERISTICS			1	1	
C _{iss}	Input Capacitance			3020		pF
C _{oss}	Output Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz		61		
C _{oss(eff.)}	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		597		pF
C _{oss(er.)}	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		107		pF
Q _{g(tot)}	Total Gate Charge at 10 V			66		nC
Q _{gs}	Gate-to-Source Gate Charge	$V_{GS} = 10 \text{ V}, V_{DS} = 400 \text{ V}, I_{D} = 18 \text{ A}$		22		
Q _{gd}	Gate-to-Drain "Miller" Charge	(Note 4)		26		-
ESR	Equivalent Series Resistance	f = 1 MHz		2.4		Ω
SWITCHING C	HARACTERISTICS					
t _{d(on)}	Turn-On Delay Time			29.2		ns
t _r	Turn-On Rise Time	V _{GS} = 10 V, V _{DD} = 400 V,	-	23.8		ns
t _{d(off)}	Turn-Off Delay Time	I _D = 18 Å, R _g = 2.2 Ω (Note 4)		69.6		ns
t _f	Turn-Off Fall Time			4.2		ns
SOURCE-DRA	IN DIODE CHARACTERISTICS		I	1	1	1
١ _S	Maximum Continuous Source-to- Drain Diode Forward Current	V _{GS} = 0 V			36	A
I _{SM}	Maximum Pulsed Source-to-Drain Diode Forward Current	V _{GS} = 0 V			90	A
V _{SD}	Source-to-Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 18 A			1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, dI _F /dt = 100 A/µs,		100		ns
Q _{rr}	Reverse Recovery Charge	$I_{SD} = 18 \text{ A}$		372		nC

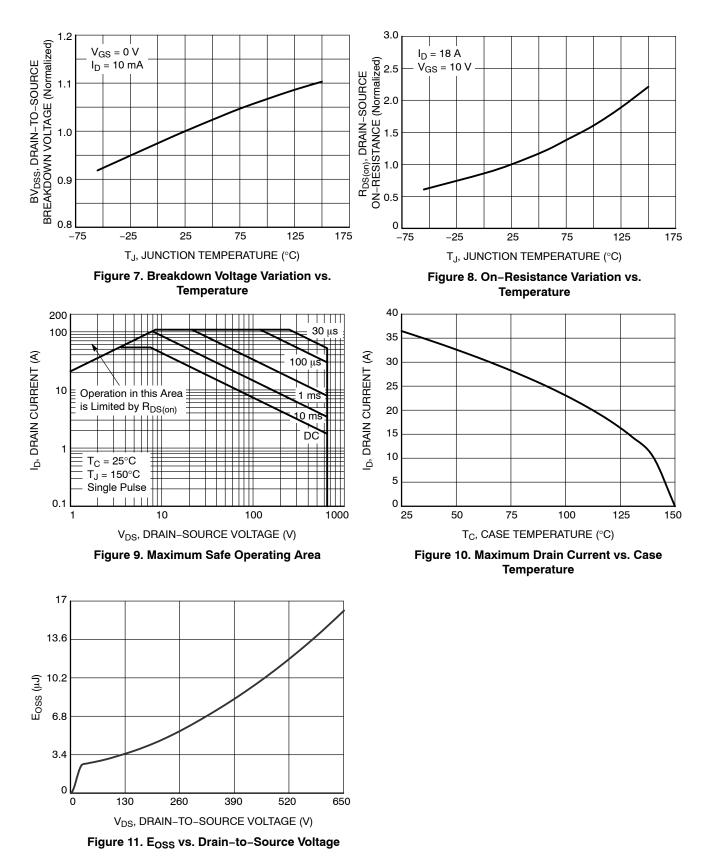
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

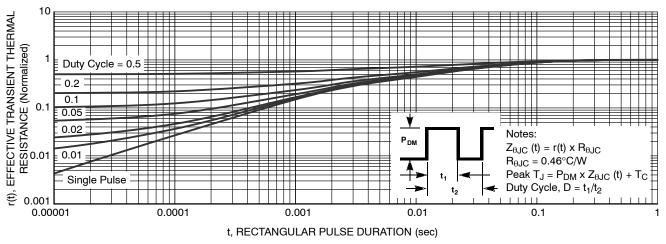


Figure 12. Transient Thermal Response

DEVICE ORDERING INFORMATION

Device	Package	Shipping [†]
NVBG095N65S3F	D2PAK-7L	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

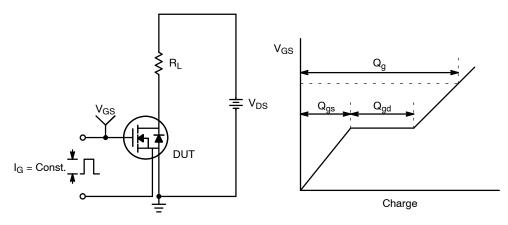


Figure 13. Gate Charge Test Circuit & Waveform

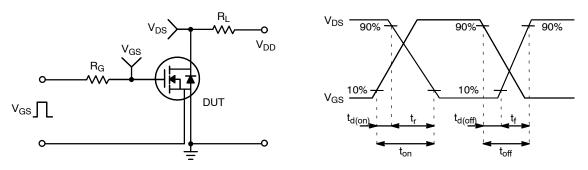
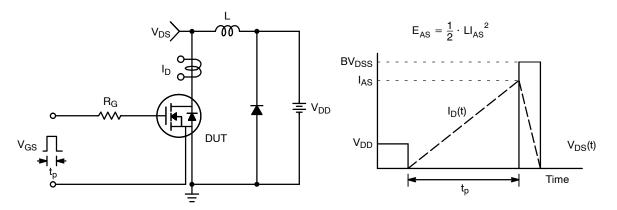


Figure 14. Resistive Switching Test Circuit & Waveforms





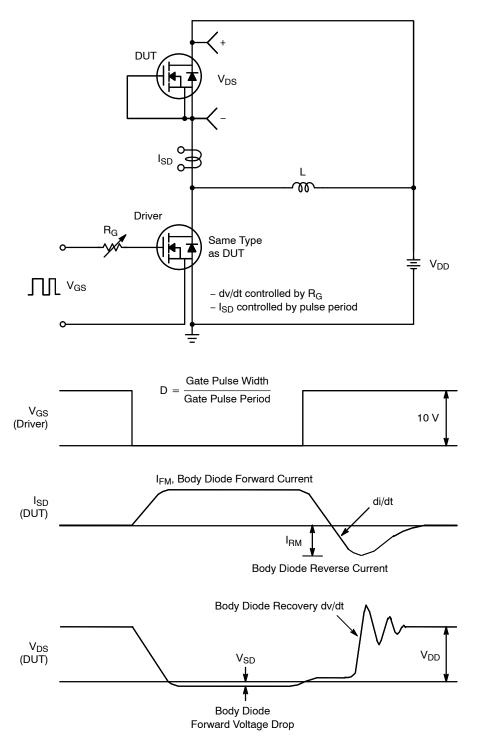


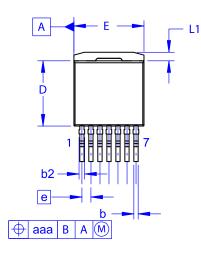
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

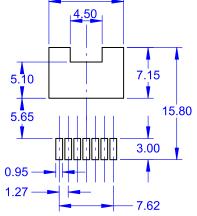
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PACKAGE DIMENSIONS

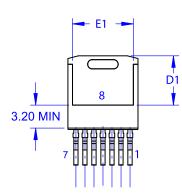
D²PAK7 (TO-263-7L HV) CASE 418BJ ISSUE B

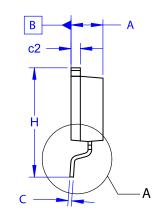






LAND PATTERN RECOMMENDATION



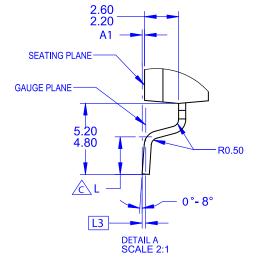


NOTES:

A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED. B. ALL DIMENSIONS ARE IN MILLIMETERS.

OUT OF JEDEC STANDARD VALUE. D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009. E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

DIM	MILLIMETERS			
DIM	MIN	NOM	MAX	
Α	4.30	4.50	4.70	
A1	0.00	0.10	0.20	
b2	0.60	0.70	0.80	
b	0.51	0.60	0.70	
С	0.40	0.50	0.60	
c2	1.20	1.30	1.40	
D	9.00	9.20	9.40	
D1	6.15	6.80	7.15	
E	9.70	9.90	10.20	
E1	7.15	7.65	8.15	
е	~	1.27	~	
Н	15.10	15.40	15.70	
L	2.44	2.64	2.84	
L1	1.00	1.20	1.40	
L3	~	0.25	~	
aaa	~	~	0.25	



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PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

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