

MOSFET - Power, Single N-Channel SuperFET® V, FRFET®, D²PAK 600 V, 55 mΩ, 45 A NVB055N60S5F

Description

The SUPERFET V MOSFET FRFET series has optimized body diode performance characteristics. This can allow for the removal of components in the application and improve application performance and reliability, particularly when soft switching topologies are used.

Features

- 650 V @ $T_J = 150^\circ\text{C}$ / Typ. $R_{DS(on)} = 44\text{ m}\Omega$
- 100% Avalanche Tested
- AEC-Q101 Qualified and PPAP Capable
- Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Electric Vehicle On Board Chargers
- EV Main Battery DC/DC Converters

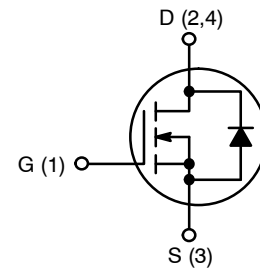
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	600	V
Gate-to-Source Voltage	V_{GS}	DC ± 30	V
		AC ($f > 1\text{ Hz}$) ± 30	
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$ 45	A
		$T_C = 100^\circ\text{C}$ 28	
Power Dissipation	$T_C = 25^\circ\text{C}$ P_D	278	W
Pulsed Drain Current	$T_C = 25^\circ\text{C}$ I_{DM}	159	A
Pulsed Source Current (Body Diode)	$T_C = 25^\circ\text{C}$, $t_p = 10\text{ }\mu\text{s}$ I_{SM}	159	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	45	A
Single Pulse Avalanche Energy	($I_L = 7\text{ A}$, $R_G = 25\text{ }\Omega$) E_{AS}	417	mJ
Avalanche Current	I_{AS}	7	A
Repetitive Avalanche Energy (Note 1)	E_{AR}	2.78	mJ
MOSFET dv/dt	dvdt	120	V/ns
Peak Diode Recovery dv/dt (Note 2)		70	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

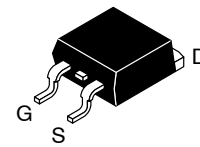
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{SD} \leq 22.5\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq 400\text{ V}$, starting $T_J = 25^\circ\text{C}$.

V_{DSS}	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
600 V	55 mΩ @ 10 V	45 A

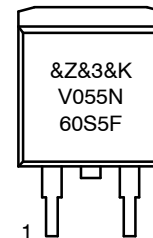


POWER MOSFET



D²PAK
CASE 418AJ

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = Date Code (Year & Week)
&K = Assembly Lot
V055N60S5F = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Max.	$R_{\theta JC}$	0.45	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient, Max.	$R_{\theta JA}$	62.5	

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^{\circ}\text{C}$	600	–	–	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 10\text{ mA}$, Referenced to 25°C	–	581	–	$\text{mV}/^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_J = 25^{\circ}\text{C}$	–	–	10	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	–	–	± 100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 22.5\text{ A}, T_J = 25^{\circ}\text{C}$	–	44	55	$\text{m}\Omega$
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 5.2\text{ mA}, T_J = 25^{\circ}\text{C}$	3.2	–	4.8	V
Forward Trans-conductance	g_{FS}	$V_{DS} = 20\text{ V}, I_D = 22.5\text{ A}$	–	44.8	–	S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 250\text{ kHz}$	–	4603	–	pF
Output Capacitance	C_{OSS}		–	72.9	–	
Time Related Output Capacitance	$C_{OSS(tr.)}$	$I_D = \text{Constant}, V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	–	1114	–	
Energy Related Output Capacitance	$C_{OSS(er.)}$		–	125	–	
Total Gate Charge	$Q_{G(tot)}$	$V_{DD} = 400\text{ V}, I_D = 22.5\text{ A}, V_{GS} = 10\text{ V}$	–	85.2	–	nC
Gate-to-Source Charge	Q_{GS}		–	26.2	–	
Gate-to-Drain Charge	Q_{GD}		–	24.9	–	
Gate Resistance	R_G	$f = 1\text{ MHz}$	–	4.32	–	Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 0/10\text{ V}, V_{DD} = 400\text{ V}, I_D = 22.5\text{ A}, R_G = 4.7\text{ }\Omega$	–	44	–	ns
Rise Time	t_r		–	26.2	–	
Turn-Off Delay Time	$t_{d(off)}$		–	108	–	
Fall Time	t_f		–	2.6	–	

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_{SD} = 22.5\text{ A}, T_J = 25^{\circ}\text{C}$	–	–	1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_{SD} = 22.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 400\text{ V}$	–	128	–	ns
Reverse Recovery Charge	Q_{RR}		–	758	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NVB055N60S5F	V055N60S5F	D ² PAK	Tape & Reel†	330 mm	24 mm	800 Units

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

TYPICAL CHARACTERISTICS

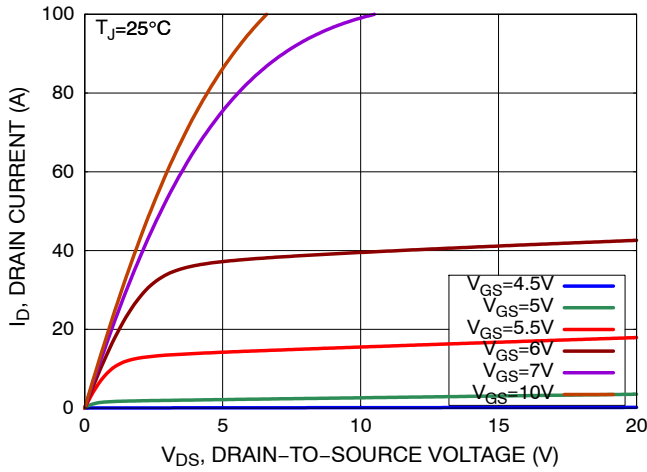


Figure 1. On-Region Characteristics

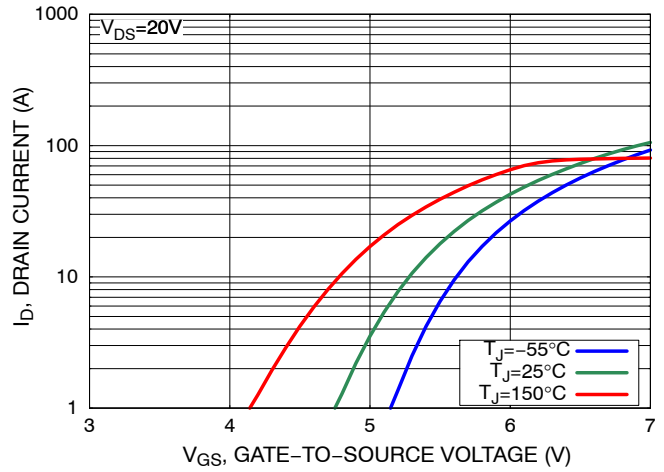


Figure 2. Transfer Characteristics

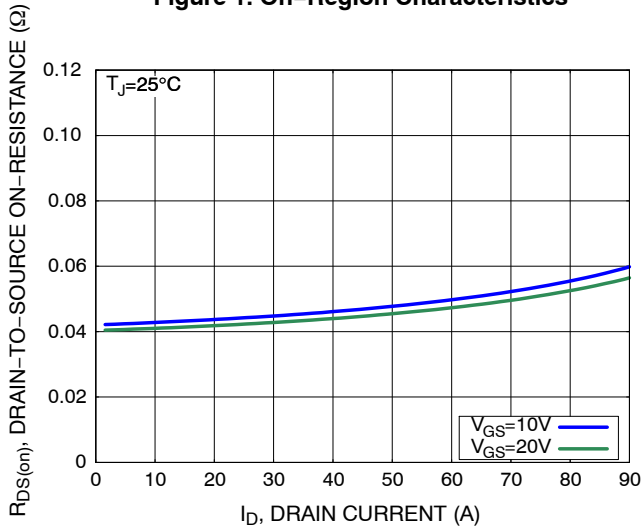


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

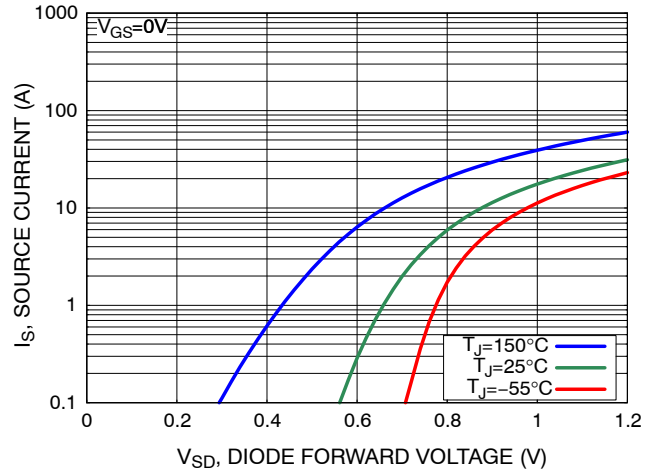


Figure 4. Diode Forward Voltage vs. Source Current

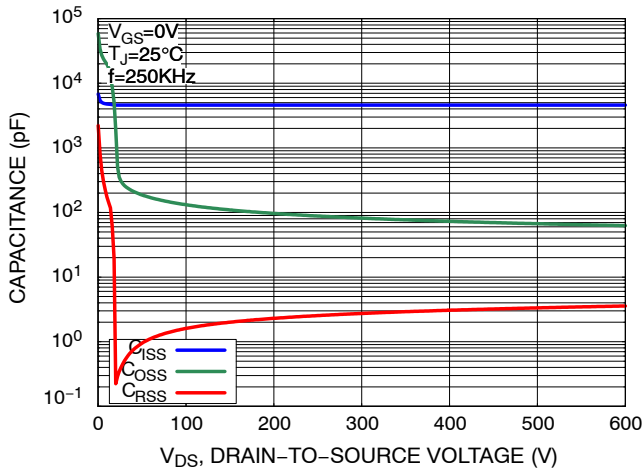


Figure 5. Capacitance Characteristics

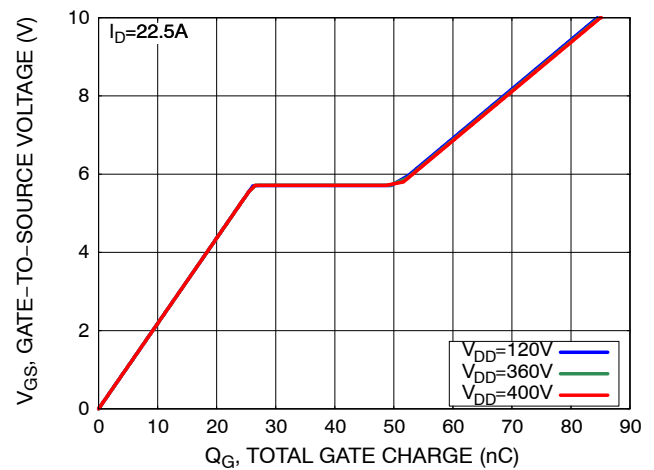


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

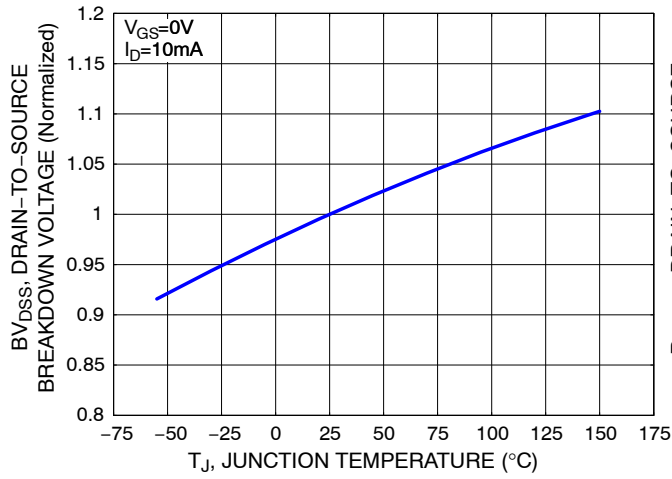


Figure 7. Breakdown Voltage Variation vs. Temperature

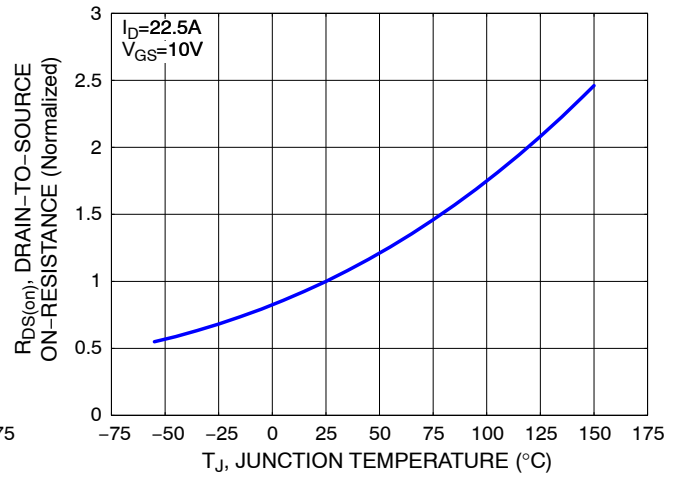


Figure 8. On-Resistance Variation vs. Temperature

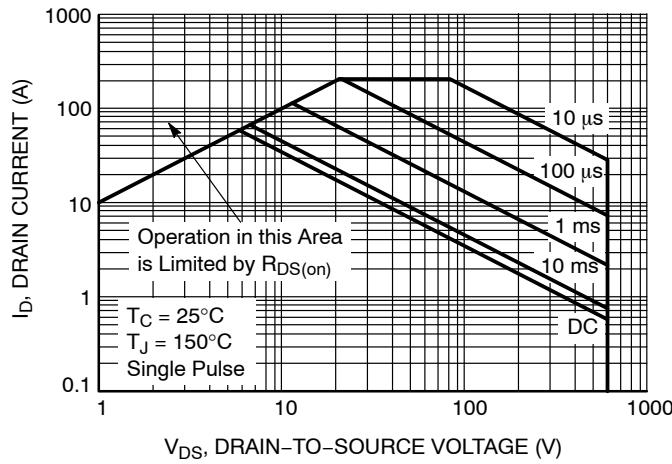


Figure 9. Maximum Safe Operating Area

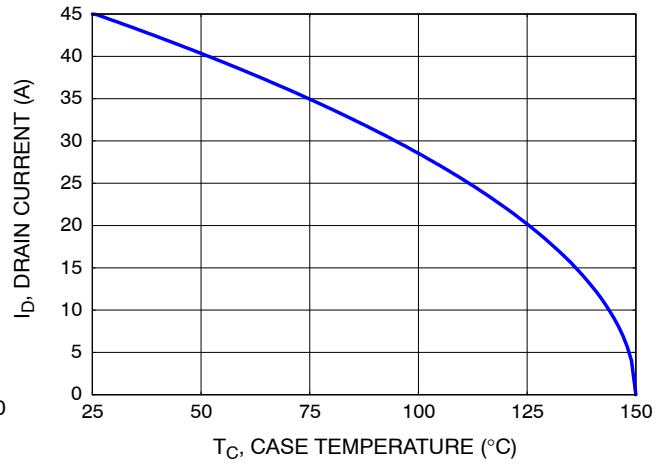


Figure 10. Maximum Drain Current vs. Case Temperature

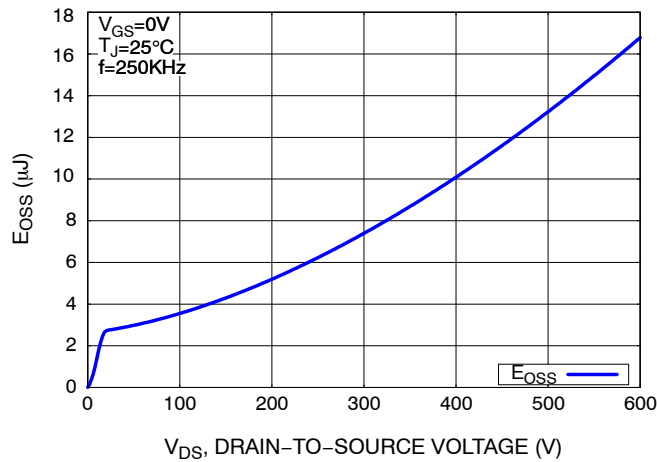


Figure 11. E_{OSS} vs. Drain-to-Source Voltage

TYPICAL CHARACTERISTICS

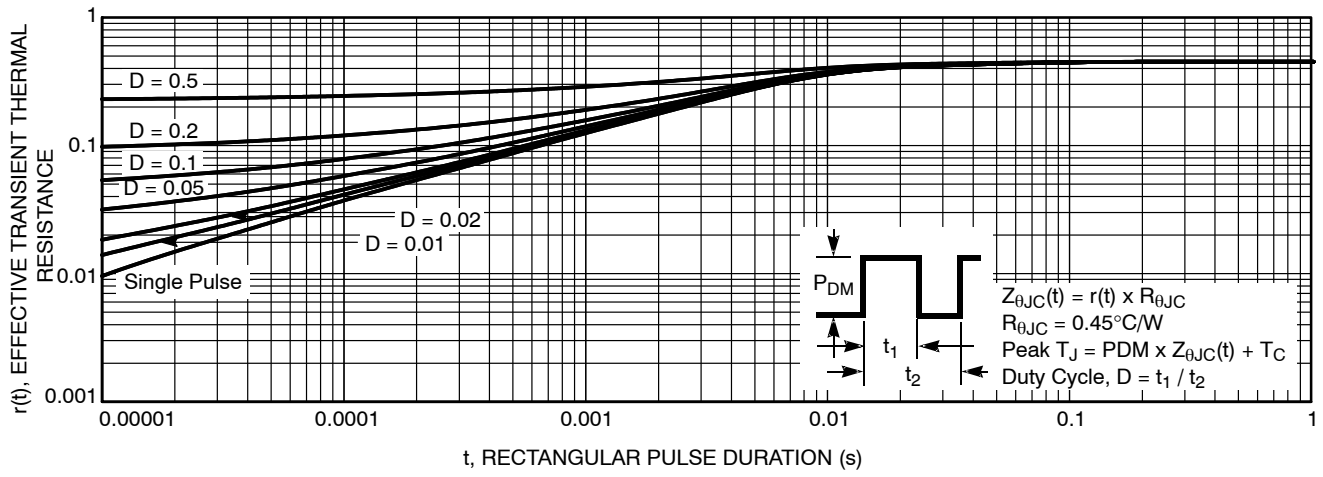


Figure 12. Transient Thermal Impedance

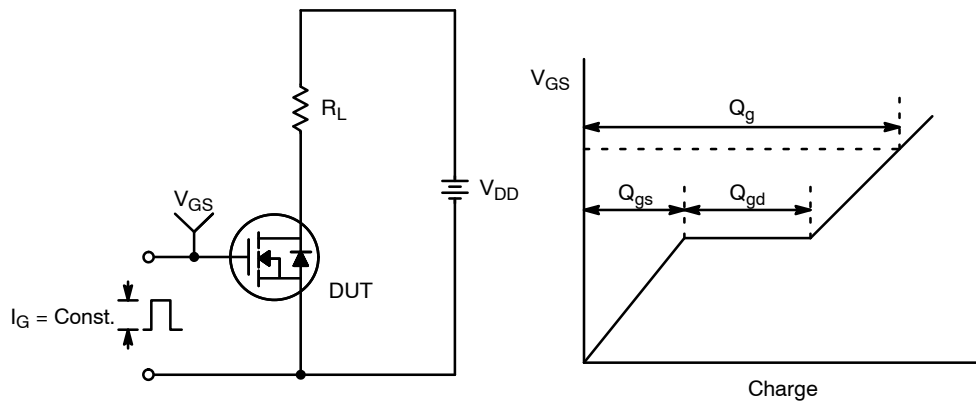


Figure 13. Gate Charge Test Circuit & Waveform

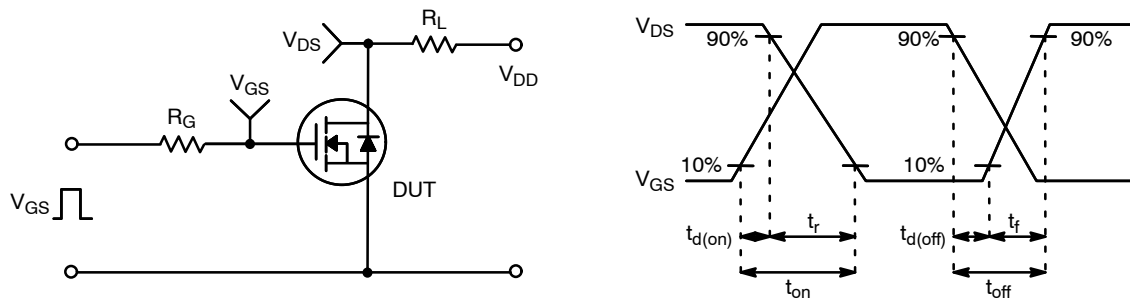


Figure 14. Resistive Switching Test Circuit & Waveforms

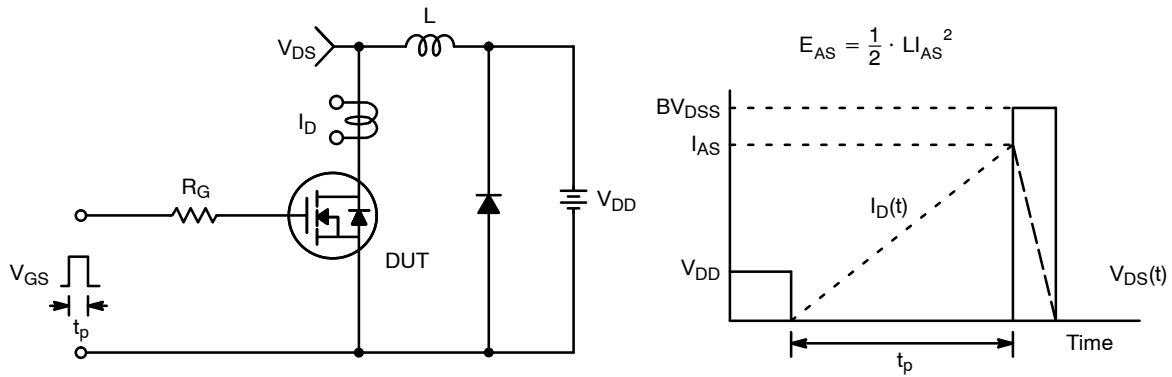


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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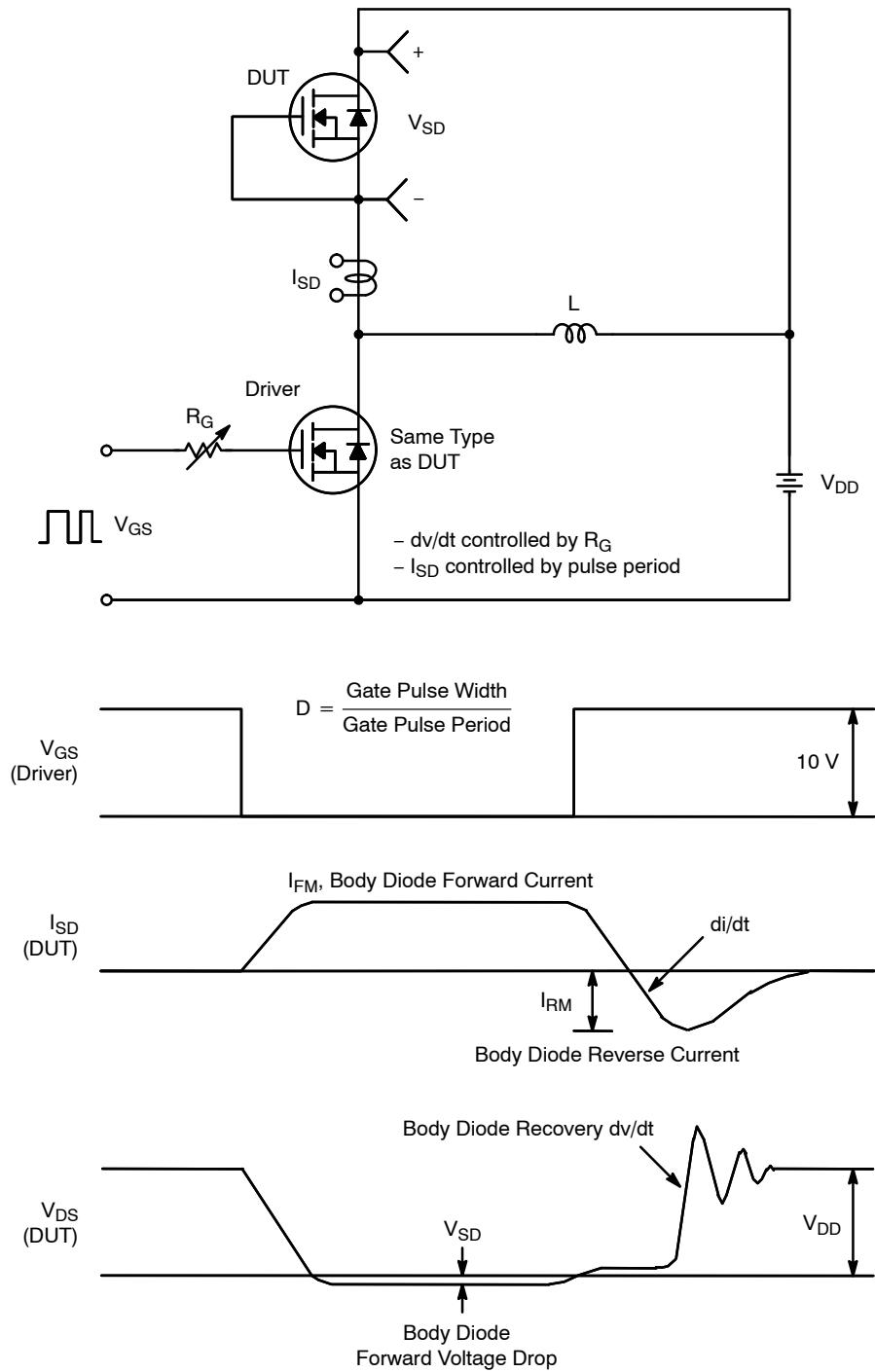
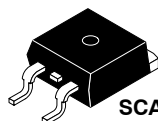


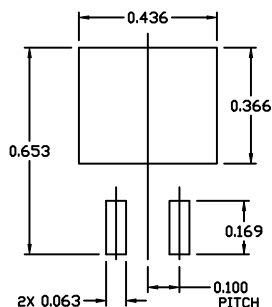
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



SCALE 1:1

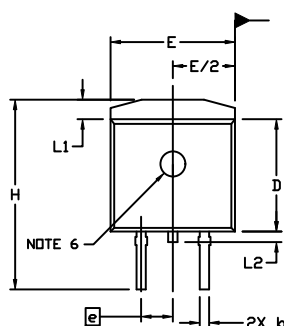
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CASE 418AJ
ISSUE F

DATE 11 MAR 2021

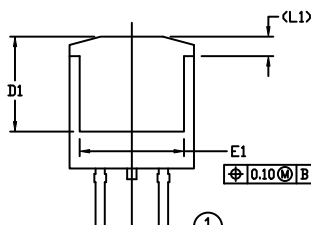


**RECOMMENDED
MOUNTING FOOTPRINT**

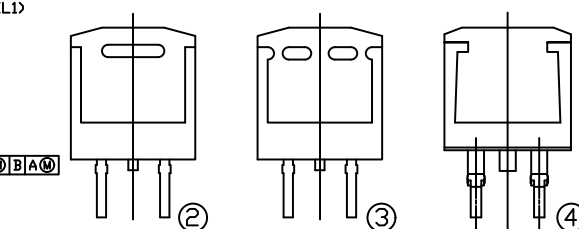
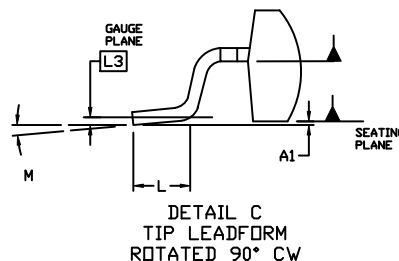
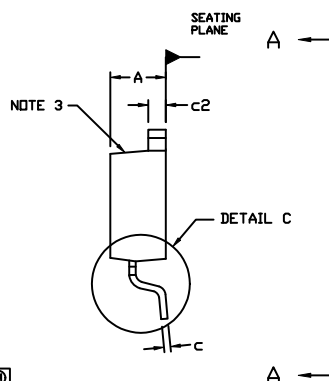
For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM1.



Φ 0.10 @ B/A

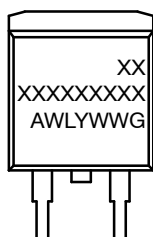


VIEW A-A

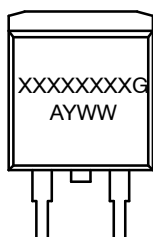


VIEW A-A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



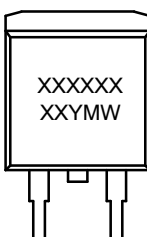
IC



Standard



Rectifier



SSG

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb-Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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