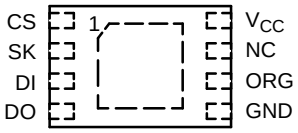
EEPROM Serial 1-Kb Microwire - Automotive Grade 1, Wettable Flank UDFN Package

NV93C46WF

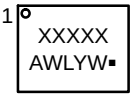
UDFN8
MU SUFFIX
CASE 517DH

PIN CONFIGURATIONS



(Top View)

DEVICE MARKING



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN FUNCTION

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
ORG	Memory Organization
NC	No Connection

Note: When the ORG pin is connected to V_{CC}, the x16 organization is selected. When it is connected to ground, the x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x16 organization.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

Description

The NV93C46WF is an EEPROM Serial 1−Kb Microwire Automotive Grade 1 device which is configured as either 64 registers of 16 bits (ORG pin at V_{CC}) or 128 registers of 8 bits (ORG pin at GND) in a Wettable Flank UDFN Package. Each register can be written (or read) serially by using the DI (or DO) pin. The NV93C46WF features a self−timed internal write with auto−clear. On−chip Power−On Reset circuit protects the internal logic against powering up in the wrong state.

Features

- Automotive AEC−Q100 Grade 1 (−40°C to +125°C) Qualified
- High Speed Operation: 2 MHz
- 2.5 V to 5.5 V Supply Voltage Range
- Selectable x8 or x16 Memory Organization
- Self−Timed Write Cycle with Auto−Clear
- Sequential Read
- Software Write Protection
- Power−up Inadvertant Write Protection
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- UDFN−8 Wettable Flank Package
- This Device is Pb−Free, Halogen Free/BFR Free and RoHS Compliant†

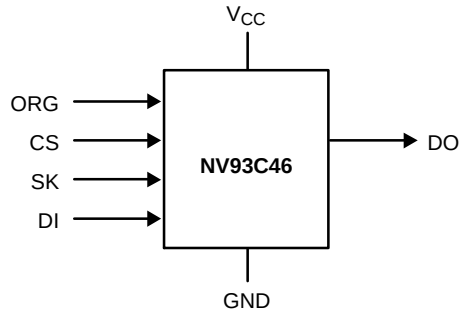


Figure 1. Functional Symbol

†For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Storage Temperature	−65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	−0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Note 3)	Endurance	1,000,000	Program / Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Block Mode, V_{CC} = 5 V, 25°C

Table 3. D.C. OPERATING CHARACTERISTICS
(V_{CC} = +2.5 V to +5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC1}	Supply Current (Write)	Write, V_{CC} = 5.0 V		1	mA
I_{CC2}	Supply Current (Read)	Read, DO open, f_{SK} = 2 MHz, V_{CC} = 5.0 V		500	μA
I_{SB1}	Standby Current (x8 Mode)	V_{IN} = GND or V_{CC} CS = GND, ORG = GND		5	μA
I_{SB2}	Standby Current (x16 Mode)	V_{IN} = GND or V_{CC} CS = GND, ORG = Float or V_{CC}		3	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		2	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC} CS = GND		2	μA
V_{IL1}	Input Low Voltage	4.5 V ≤ V_{CC} < 5.5 V	−0.1	0.8	V
V_{IH1}	Input High Voltage	4.5 V ≤ V_{CC} < 5.5 V	2	V_{CC} + 1	V
V_{IL2}	Input Low Voltage	2.5 V ≤ V_{CC} < 4.5 V	0	V_{CC} x 0.2	V
V_{IH2}	Input High Voltage	2.5 V ≤ V_{CC} < 4.5 V	V_{CC} x 0.7	V_{CC} + 1	V
V_{OL1}	Output Low Voltage	4.5 V ≤ V_{CC} < 5.5 V, I_{OL} = 3 mA		0.4	V
V_{OH1}	Output High Voltage	4.5 V ≤ V_{CC} < 5.5 V, I_{OH} = −400 μA	2.4		V
V_{OL2}	Output Low Voltage	2.5 V ≤ V_{CC} < 4.5 V, I_{OL} = 1 mA		0.2	V
V_{OH2}	Output High Voltage	2.5 V ≤ V_{CC} < 4.5 V, I_{OH} = −100 μA	V_{CC} − 0.2		V

Table 4. PIN CAPACITANCE (T_A = 25°C, f = 1 MHz, V_{CC} = 5 V)

Symbol	Test	Conditions	Min	Typ	Max	Units
C_{OUT} (Note 4)	Output Capacitance (DO)	V_{OUT} = 0 V			5	pF
C_{IN} (Note 4)	Input Capacitance (CS, SK, DI, ORG)	V_{IN} = 0 V			5	pF

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.

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Table 5. A.C. CHARACTERISTICS
(V_{CC} = +2.5 V to +5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Units
t_{CSS}	CS Setup Time	50		ns
t_{CSH}	CS Hold Time	0		ns
t_{DIS}	DI Setup Time	100		ns
t_{DIH}	DI Hold Time	100		ns
t_{PD1}	Output Delay to 1		0.25	μs
t_{PD0}	Output Delay to 0		0.25	μs
t_{HZ} (Note 5)	Output Delay to High−Z		100	ns
t_{EW}	Program/Erase Pulse Width		5	ms
t_{CSMIN}	Minimum CS Low Time	0.25		μs
t_{SKHI}	Minimum SK High Time	0.25		μs
t_{SKLOW}	Minimum SK Low Time	0.25		μs
t_{SV}	Output Delay to Status Valid		0.25	μs
SK_{MAX}	Maximum Clock Frequency	DC	2000	kHz

5. This parameter is tested initially and after a design or process change that affects the parameter.

Table 6. POWER−UP TIMING (Notes 6 and 7)

Symbol	Parameter	Max	Units
t_{PUR}	Power−up to Read Operation	1	ms
t_{PUW}	Power−up to Write Operation	1	ms

6. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
7. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Table 7. A.C. TEST CONDITIONS

Input Rise and Fall Times	≤ 50 ns	
Input Pulse Voltages	0.4 V to 2.4 V	4.5 V ≤ V_{CC} ≤ 5.5 V
Timing Reference Voltages	0.8 V, 2.0 V	4.5 V ≤ V_{CC} ≤ 5.5 V
Input Pulse Voltages	0.2 V_{CC} to 0.7 V_{CC}	2.5 V ≤ V_{CC} ≤ 4.5 V
Timing Reference Voltages	0.5 V_{CC}	2.5 V ≤ V_{CC} ≤ 4.5 V
Output Load	Current Source I_{OLmax}/I_{OHmax}; C_L = 100 pF	

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DEVICE OPERATION

The NV93C46WF is a 1024−bit nonvolatile memory intended for use with industry standard microprocessors. The NV93C46WF can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 9−bit instructions control the reading, writing and erase operations of the device. When organized as X8, seven 10−bit instructions control the reading, writing and erase operations of the device. The NV93C46WF operates on a single power supply and will generate on chip the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status during a write operation. The serial communication protocol follows the timing shown in Figure 2.

The ready/busy status can be determined after the start of internal write cycle by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy “1” into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The Ready/Busy flag can be disabled only in Ready state; no change is allowed in Busy state.

The format for all instructions sent to the device is a logical “1” start bit, a 2−bit (or 4−bit) opcode, 6−bit address (an additional bit when organized X8) and for write operations a 16−bit data field (8−bit for X8 organization).

Read

Upon receiving a READ command (Figure 3) and an address (clocked into the DI pin), the DO pin of the NV93C46WF will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

After the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is proceeded by a dummy zero bit. All sunsequent data words will follow without a dummy zero bit.

Erase/Write Enable and Disable

The NV93C46WF powers up in the write disable state. Any writing after power−up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all NV93C46WF write and erase instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status. The EWEN and EWDS instructions timing is shown in Figure 4.

Table 8. INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A6−A0	A5−A0			Read Address AN–A0
ERASE	1	11	A6−A0	A5−A0			Clear Address AN–A0
WRITE	1	01	A6−A0	A5−A0	D7−D0	D15−D0	Write Address AN–A0
EWEN	1	00	11XXXXX	11XXXX			Write Enable
EWDS	1	00	00XXXXX	00XXXX			Write Disable
ERAL	1	00	10XXXXX	10XXXX			Clear All Addresses
WRAL	1	00	01XXXXX	01XXXX	D7−D0	D15−D0	Write All Addresses

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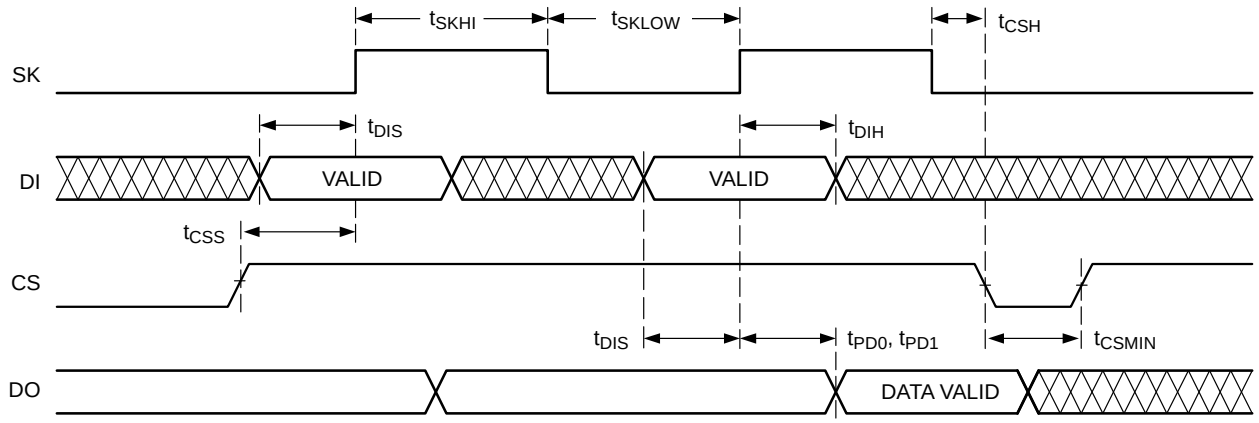

Figure 2. Synchronous Data Timing

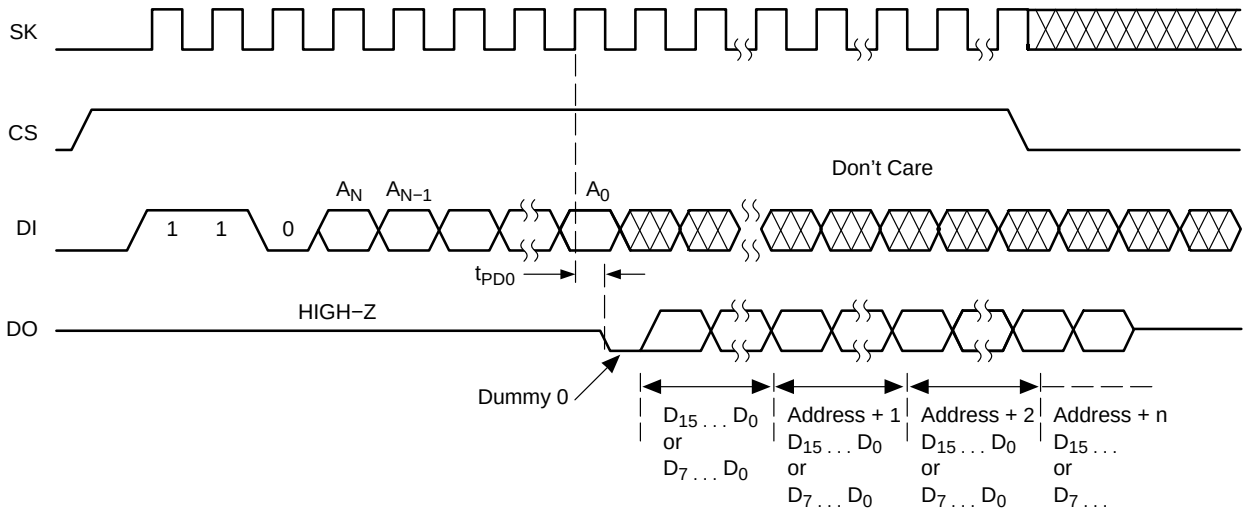

Figure 3. Read Instruction Timing

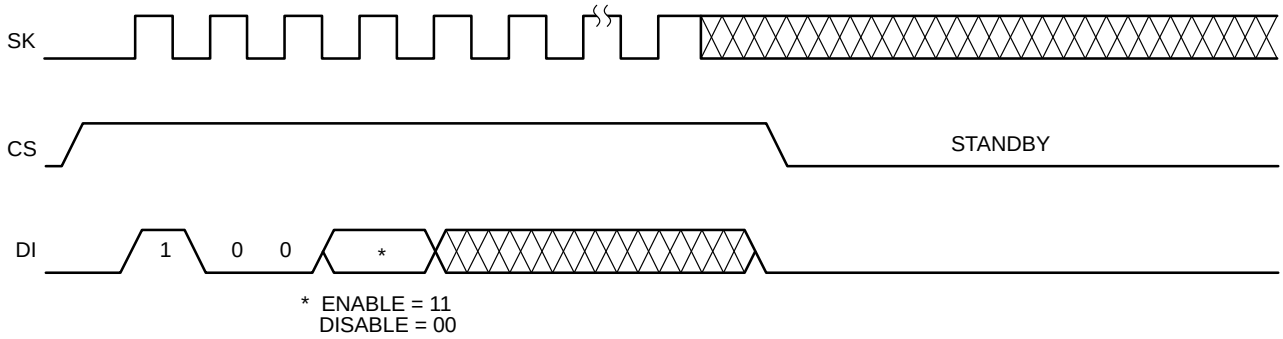

Figure 4. EWEN/EWDS Instruction Timing

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Write

After receiving a WRITE command (Figure 5), address and the data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking for auto−clear and data store cycles on the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the NV93C46WF can be determined by selecting the device and polling the DO pin. Since this device features Auto−Clear before write, it is NOT necessary to erase a memory location before it is written into.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be de−asserted for a minimum of t_{CSMIN} (Figure 6). The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the NV93C46WF can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical “1” state.

Erase All

Upon receiving an ERAL command (Figure 7), the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the NV93C46WF can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical “1” state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} (Figure 8). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the NV93C46WF can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

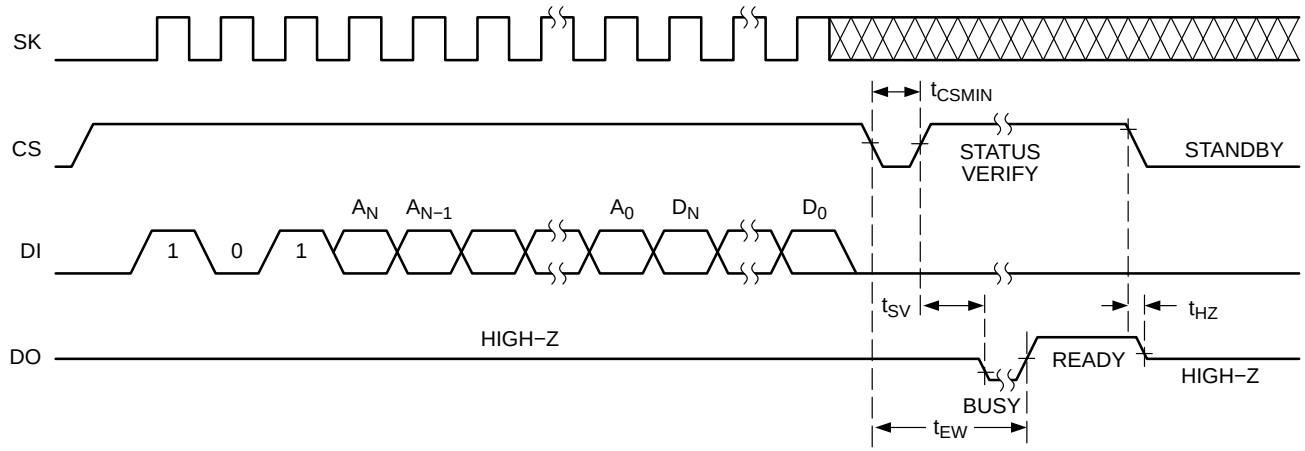

Figure 5. Write Instruction Timing

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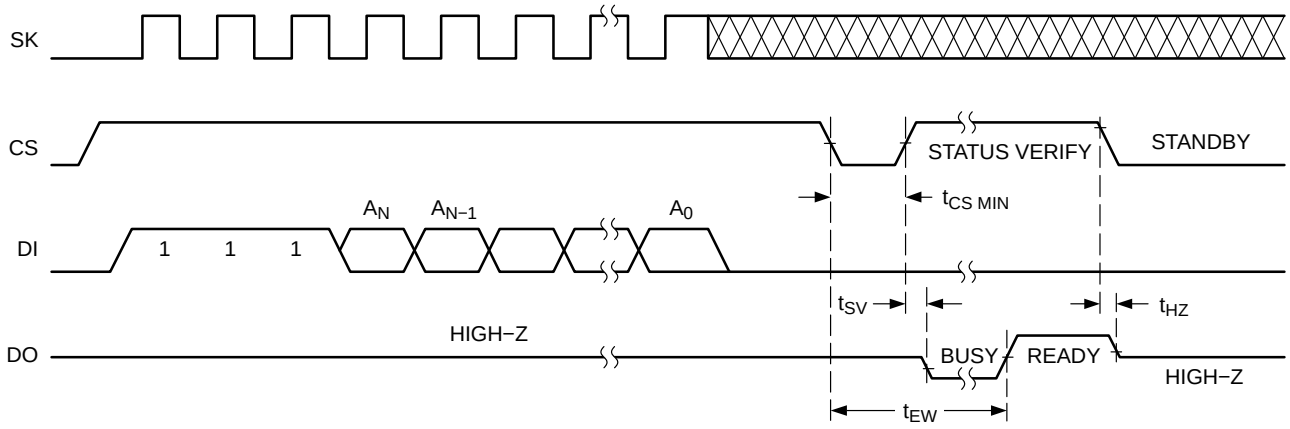

Figure 6. Erase Instruction Timing

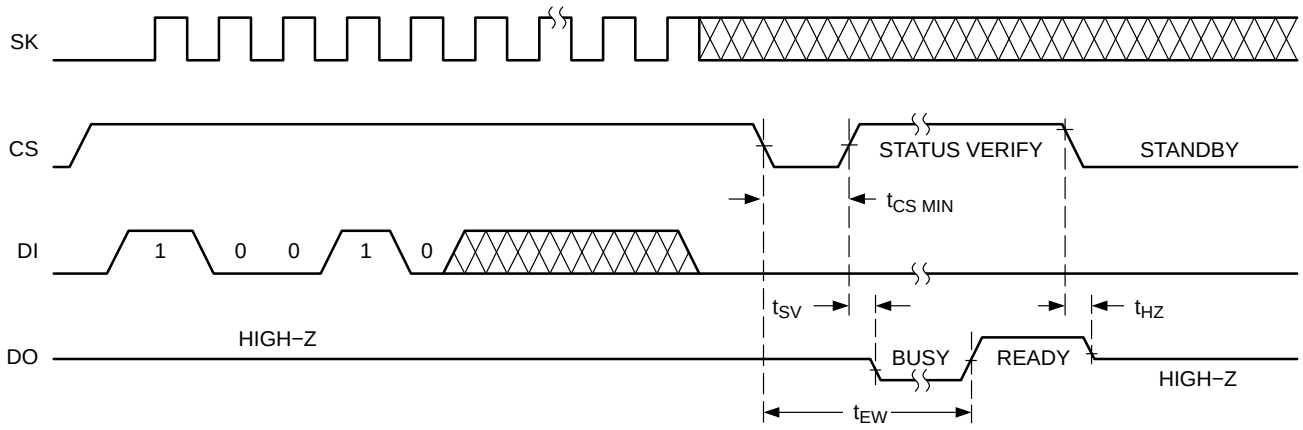

Figure 7. ERAL Instruction Timing

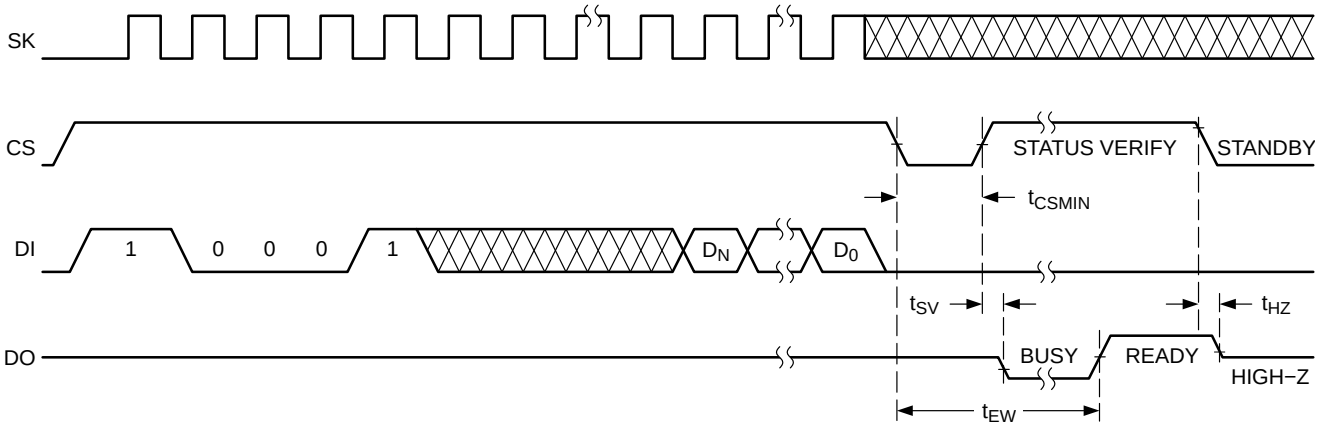

Figure 8. WRAL Instruction Timing

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ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Shipping†
NV93C46BMUW3VTBG	M0W	UDFN−8 (2x3 mm) Wettable Flank	V = Auto Grade 1 (−40°C to +125°C)	Tape & Reel, 3,000 Units / Reel
NV93C46RBMUW3VTBG	M1W	UDFN−8 (2x3 mm) Wettable Flank	V = Auto Grade 1 (−40°C to +125°C)	Tape & Reel, 3,000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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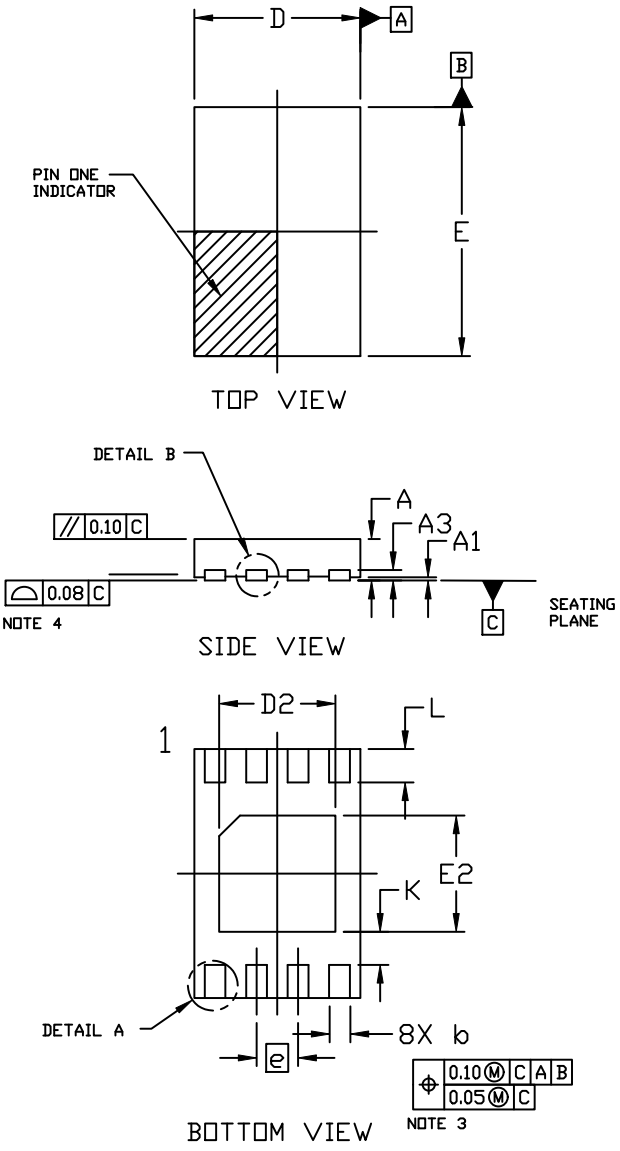
UDFN8 2x3, 0.5P
CASE 517DH
ISSUE A

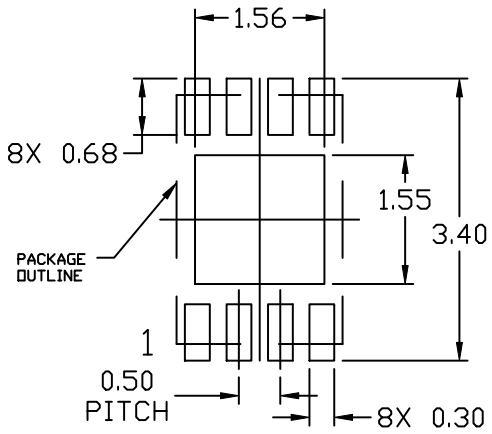
SCALE 2:1

DATE 10 DEC 2020



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
A1	0.00	---	0.05
A3	0.13 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.30	1.40	1.50
e	0.50 BSC		
K	0.40 REF		
L	0.30	0.40	0.50



RECOMMENDED MOUNTING FOOTPRINT*

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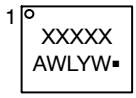
GENERIC MARKING DIAGRAM*



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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