NUP4012PXV6

Quad Transient Voltage Suppressor Array

ESD Protection Diodes with Ultra−Low (0.7 pF) Capacitance

The four−line voltage transient suppressor array is designed to protect voltage−sensitive components that require ultra−low capacitance from ESD and transient voltage events. This device features a common anode design which protects four independent data lines in a single SOT−563 low profile package.

Excellent clamping capability, low capacitance, low leakage, and fast response time make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs.

Features

- Low Capacitance (0.7 pF Typical)
- Protects up to Four Data Lines
- SOT−563 1.6 mm x 1.6 mm
- Low Profile of 0.55 mm for Slim Design Ultra
- D_1, D_2, D_3, and D_4 Pins = 5.2 V Minimum Protection
- ESD Rating: IEC61000−4−2: Level 4
- This is a Pb−Free Device

Typical Applications

- USB 2.0 High−Speed Interface
- Cell Phones
- MP3 Players
- SIM Card Protection

MAXIMUM RATINGS (T_J = 25°C, unless otherwise specified)

Symbol	Rating	Value	Unit
T_J	Operating Junction Temperature Range	−40 to 125	°C
T_{STG}	Storage Temperature Range	−55 to 150	°C
T_L	Lead Solder Temperature − Maximum (10 seconds)	260	°C
ESD	IEC 61000−4−2 Contact	8000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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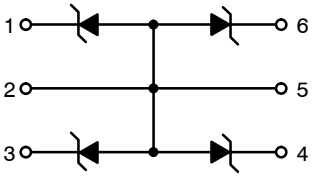


SOT−563
CASE 463A

MARKING DIAGRAM

P7 = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NUP4012PXV6T1G	SOT−563 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

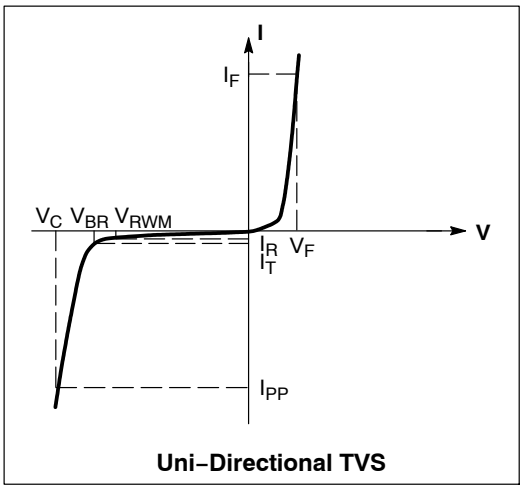
See Application Note AND8308/D for further description of survivability specs.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Max. Capacitance @ V_R = 0 and f = 1.0 MHz

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Uni−Directional TVS

ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Reverse Working Voltage (D_1, D_2, D_3, and D_4)	(Note 1)	V_{RWM}	–	–	4.0	V
Breakdown Voltage (D_1, D_2, D_3, and D_4)	I_T = 1 mA, (Note 2)	V_{BR}	5.2	5.5	–	V
Reverse Leakage Current (D_1, D_2, D_3, and D_4)	@ V_{RWM}	I_R	–	–	1.0	μA
Capacitance (D_1, D_2, D_3, and D_4)	V_R = 0 V, f = 1 MHz (Line to GND)	C_J	–	0.7	0.9	pF
Clamping Voltage	@ I_{PP} = 1 A (Note 3)	V_C	–	–	9.5	V
Clamping Voltage	Per IEC61000−4−2 (Note 4)	V_C	Figures 1 and 2			V

1. TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
2. V_{BR} is measured at pulse test current I_T.
3. Surge current waveform per Figure 5.
4. Typical waveform. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

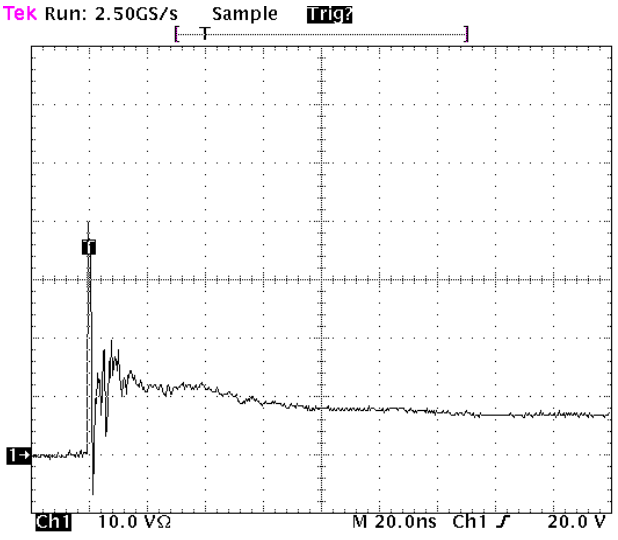


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

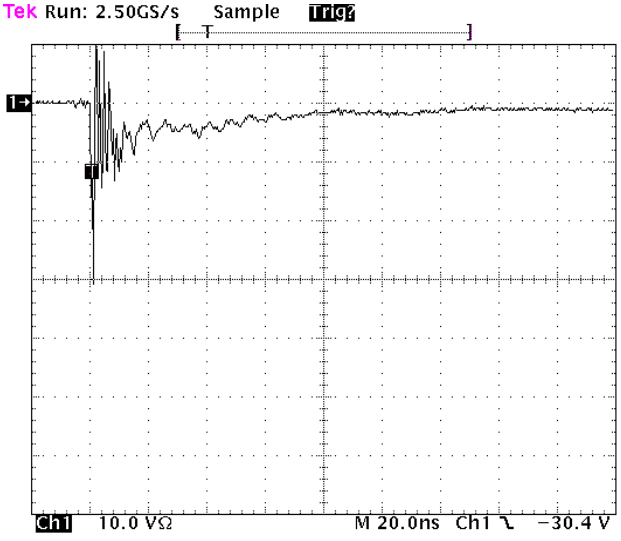


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

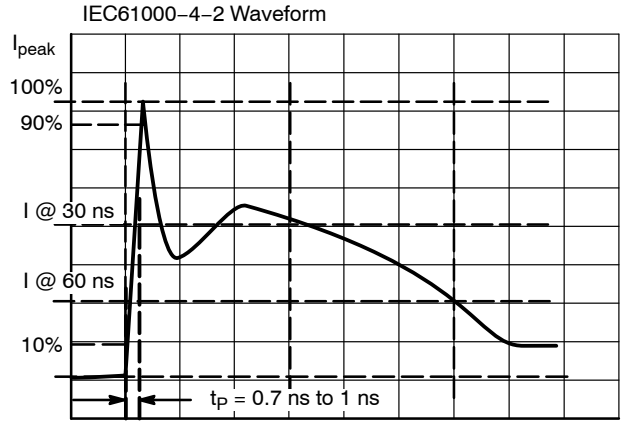


Figure 3. IEC61000−4−2 Spec

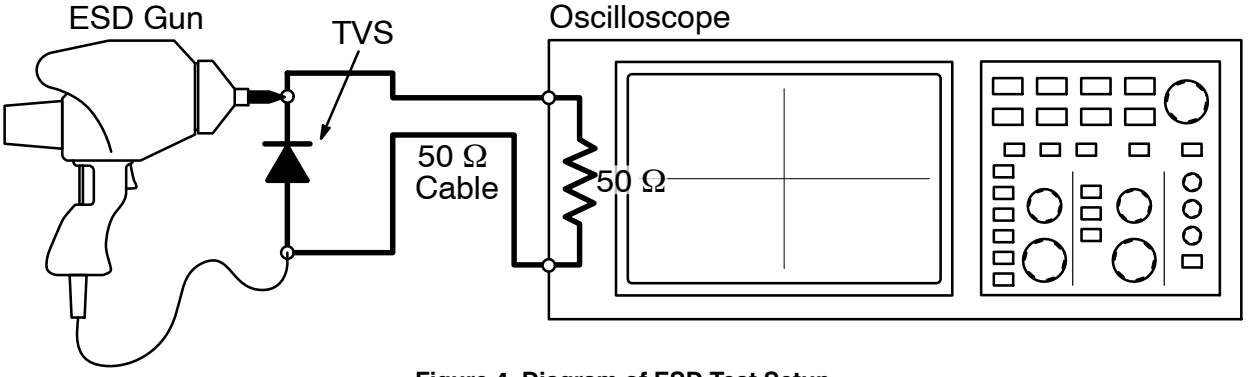


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

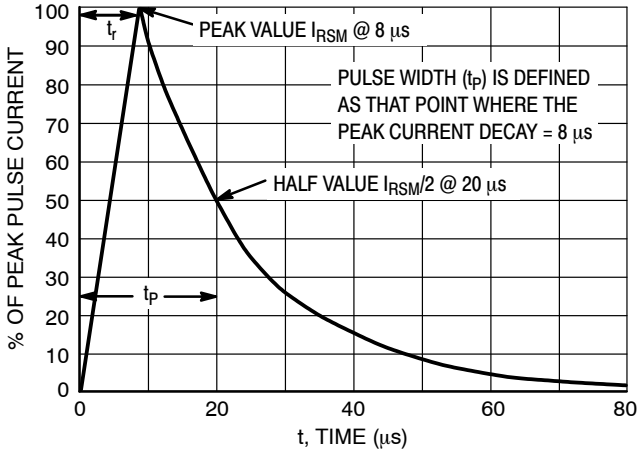
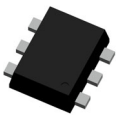


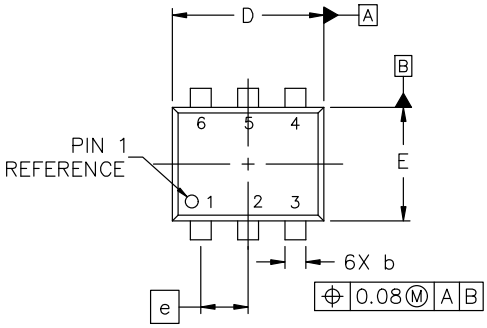
Figure 5. 8 X 20 μs Pulse Waveform



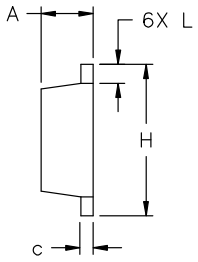
SOT−563−6 1.60x1.20x0.55, 0.50P
CASE 463A
ISSUE J

DATE 15 FEB 2024

NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

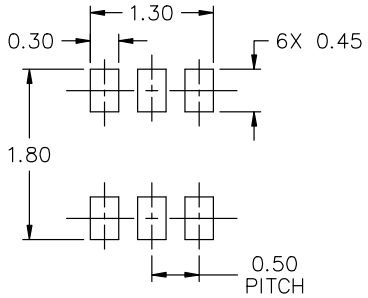


TOP VIEW



SIDE VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.50	1.60	1.70
E	1.10	1.20	1.30
e	0.50 BSC		
H	1.50	1.60	1.70
L	0.10	0.20	0.30



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

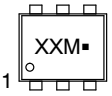
STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOT−563−6 1.60x1.20x0.55, 0.50P**		**PAGE 1 OF 1**

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