NUP4012PMU

ESD Protection Diode Array

Quad, Ultra−Low Capacitance

The four−line surge protection array is designed to protect voltage−sensitive components that require ultra−low capacitance from ESD and transient voltage events. This device features a common anode design which protects four independent high speed data lines in a single six−lead UDFN low profile package.

Excellent clamping capability, low capacitance, low leakage, and fast response time make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs.

Features

- Low Capacitance Data Lines (0.7 pF Typical)
- Protects up to Four Data Lines
- UDFN Package, 1.6 x 1.6 mm
- Low Profile of 0.50 mm for Ultra Slim Design
- ESD Rating: IEC61000−4−2: Level 4
  − Contact (14 kV)
- D_1, D_2, D_3 and D_4 Pins = 5.2 V Minimum Protection
- RoHS Compliant
- This is a Pb−Free Device

Typical Applications

- USB 2.0 High−Speed Interface
- Cell Phones
- MP3 Players
- SIM Card Protection

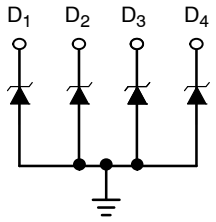
MAXIMUM RATINGS (T_J = 25°C, unless otherwise specified)

Symbol	Rating	Value	Unit
T_J	Operating Junction Temperature Range	−40 to 125	°C
T_{STG}	Storage Temperature Range	−55 to 150	°C
T_L	Lead Solder Temperature − Maximum (10 seconds)	260	°C
ESD	IEC 61000−4−2 Contact	14000	V

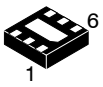
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ON Semiconductor®

www.onsemi.com



MARKING DIAGRAM

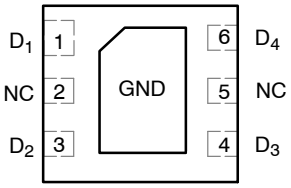


UDFN6 1.6x1.6
MU SUFFIX
CASE 517AP

P7 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

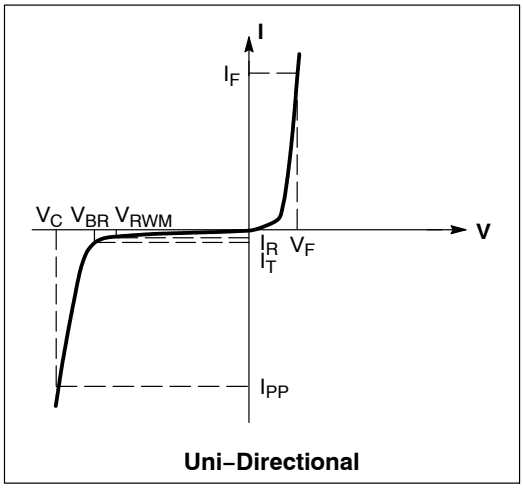
Device	Package	Shipping†
NUP4012PMUTAG	UDFN6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Max. Capacitance @ V_R = 0 and f = 1.0 MHz



ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Reverse Working Voltage (D_1, D_2, D_3 and D_4)	(Note 1)	V_{RWM}	–	–	4.0	V
Breakdown Voltage (D_1, D_2, D_3 and D_4)	I_T = 1 mA, (Note 2)	V_{BR}	5.2	5.5	–	V
Reverse Leakage Current (D_1, D_2, D_3 and D_4)	@ V_{RWM}	I_R	–	–	1.0	μA
Capacitance (D_1, D_2, D_3 and D_4)	V_R = 0 V, f = 1 MHz (Line to GND)	C_J	–	0.7	0.9	pF

1. Surge protection devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
2. V_{BR} is measured at pulse test current I_T.

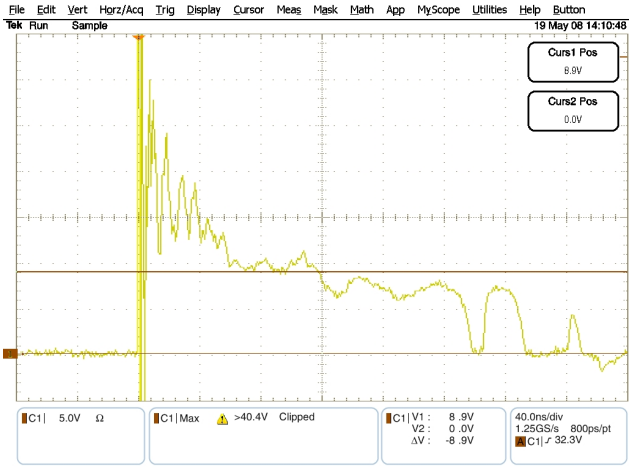


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

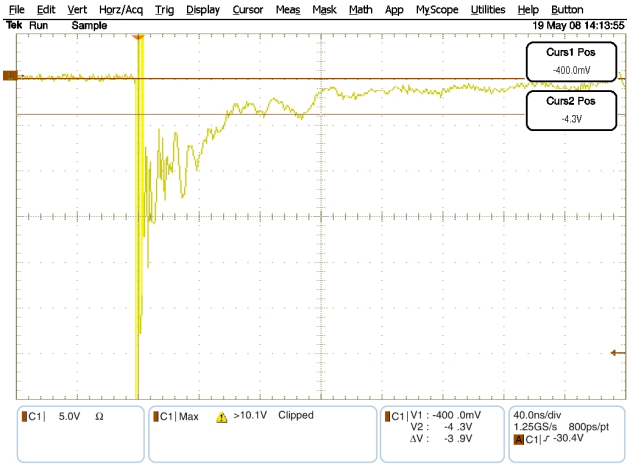
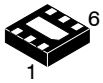


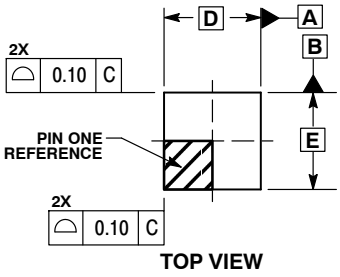
Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

UDFN6 1.6x1.6, 0.5P
CASE 517AP
ISSUE O

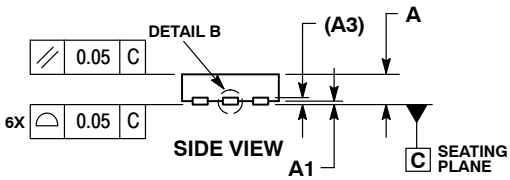
DATE 26 OCT 2007

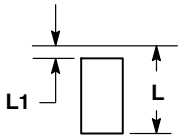


SCALE 4:1

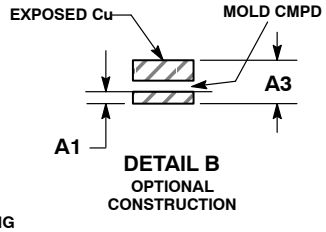


TOP VIEW

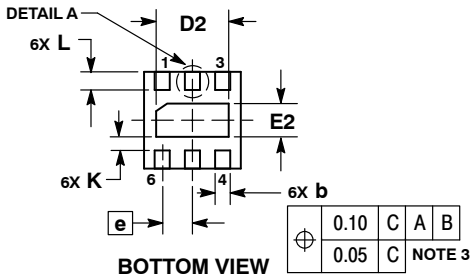




DETAIL A
OPTIONAL CONSTRUCTION

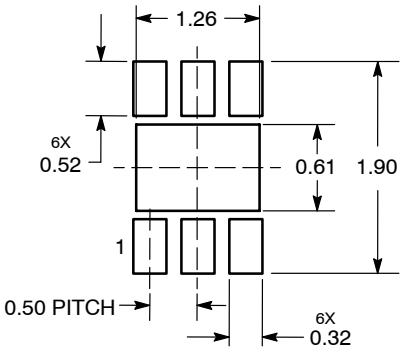


DETAIL B
OPTIONAL CONSTRUCTION



BOTTOM VIEW

SOLDERMASK DEFINED MOUNTING FOOTPRINT*



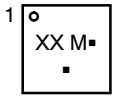
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.20	0.30
D	1.60 BSC	
E	1.60 BSC	
e	0.50 BSC	
D2	1.10	1.30
E2	0.45	0.65
K	0.20	---
L	0.20	0.40
L1	0.00	0.15

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98AON25711D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**6 PIN UDFN, 1.6X1.6, 0.5P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales