MOSFET – P-Channel, Small Signal, SOT-563

-20 V, -950 mA

NTZS3151P

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max
−20 V	120 mΩ @ −4.5 V	−950 mA
	144 mΩ @ −2.5 V	
	195 mΩ @ −1.8 V	

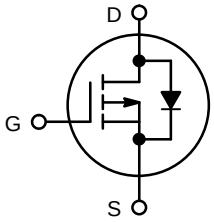
Features

- Low $R_{DS(on)}$ Improving System Efficiency
- Low Threshold Voltage
- Small Footprint 1.6 x 1.6 mm
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Load/Power Switches
- Battery Management
- Cell Phones, Digital Cameras, PDAs, Pagers, etc.

P-Channel MOSFET

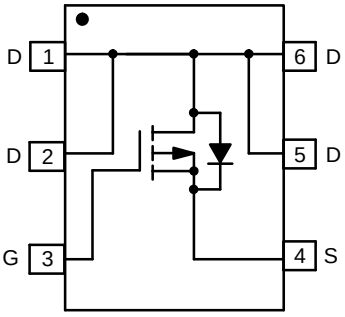


SOT-563-6
CASE 463A

MARKING DIAGRAM

TX = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PINOUT: SOT-563



Top View

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted.)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	−20	V
Gate-to-Source Voltage			V_{GS}	±8.0	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25 °C	I_D	−860	mA
		T_A = 70 °C		−690	
Power Dissipation (Note 1)	Steady State		P_D	170	mW
Continuous Drain Current (Note 1)	t ≤ 5 s	T_A = 25 °C	I_D	−950	mA
		T_A = 70 °C		−760	
Power Dissipation (Note 1)	t ≤ 5 s		P_D	210	mW
Pulsed Drain Current	t_p = 10 μs		I_{DM}	−4.0	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	−360	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient − Steady State (Note 1)	$R_{\theta JA}$	720	°C/W
Junction-to-Ambient − t ≤ 5 s (Note 1)	$R_{\theta JA}$	600	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in. sq. pad size (Cu. area = 1.127 in. sq. [1 oz.] including traces).

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 4.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted.)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				−13		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V	T_J = 25 °C			−1.0	μA
		V_{DS} = −20 V	T_J = 125 °C			−5.0	
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8.0 V				±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−0.45		−1.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				2.4		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V, I_D = −950 mA			120	150	mΩ
		V_{GS} = −4.5 V, I_D = −770 mA			112	142	
		V_{GS} = −2.5 V, I_D = −670 mA			144	200	
		V_{GS} = −1.8 V, I_D = −200 mA			195	240	
Forward Transconductance	g_{FS}	V_{DS} = −10 V, I_D = −810 mA			3.1		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −16 V			458		pF
Output Capacitance	C_{OSS}				61		
Reverse Transfer Capacitance	C_{RSS}				38		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −10 V; I_D = −770 mA			5.6		nC
Threshold Gate Charge	$Q_{G(TH)}$				0.6		
Gate-to-Source Charge	Q_{GS}				0.9		
Gate-to-Drain Charge	Q_{GD}				1.2		
SWITCHING CHARACTERISTICS (Note 3)							
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = −4.5 V, V_{DD} = −10 V, I_D = −950 mA, R_G = 6.0 Ω			5.0		ns
Rise Time	t_r				12		
Turn-Off Delay Time	$t_{d(OFF)}$				23.7		
Fall Time	t_f				18		
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −360 mA	T_J = 25 °C		−0.64	−0.9	V
			T_J = 125 °C		−0.5		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = −360 mA			10.5		ns

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES (T_J = 25 °C unless otherwise noted)

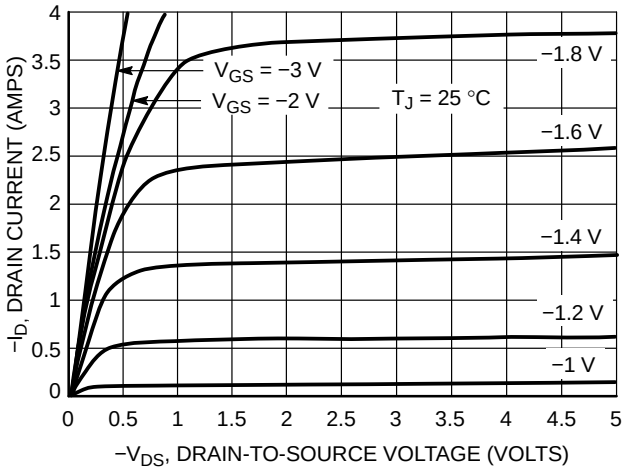


Figure 1. On-Region Characteristics

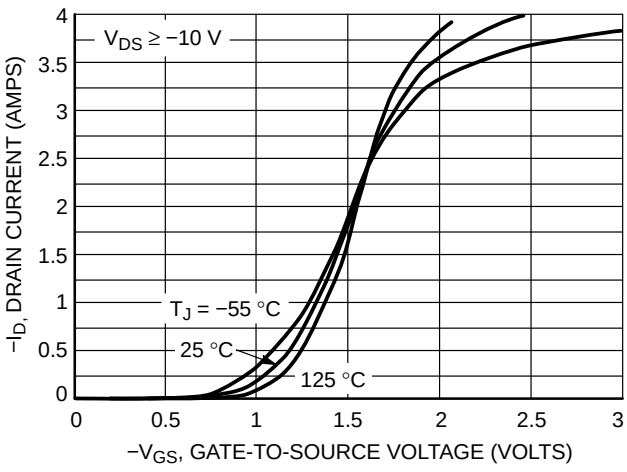


Figure 2. Transfer Characteristics

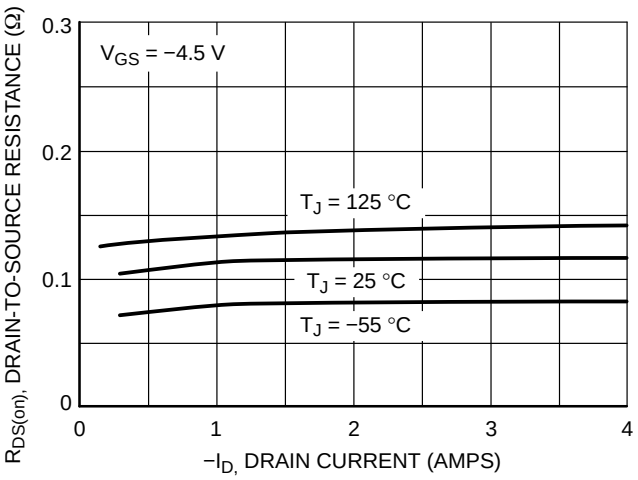


Figure 3. On-Resistance vs. Drain Current and Temperature

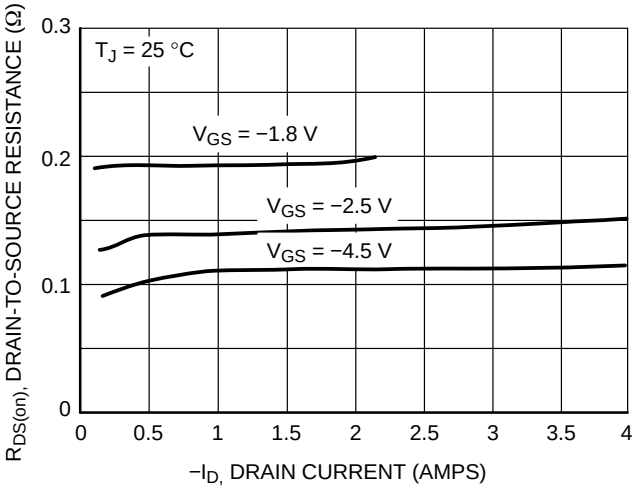


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

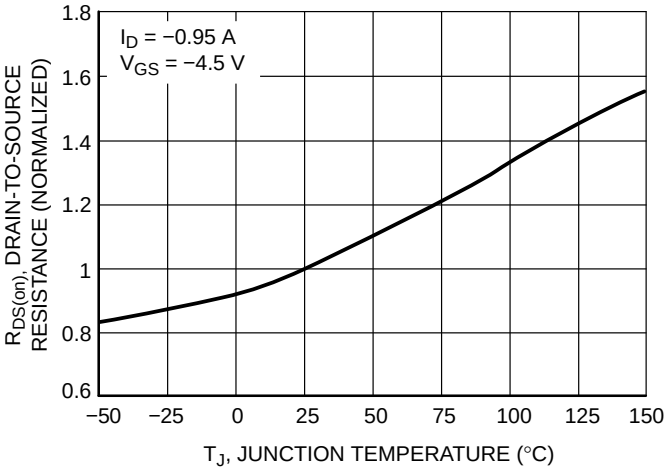


Figure 5. On-Resistance Variation with Temperature

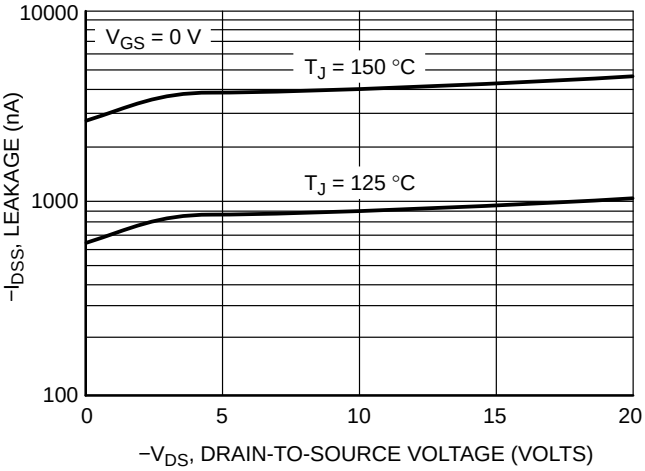


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES (T_J = 25 °C unless otherwise noted)

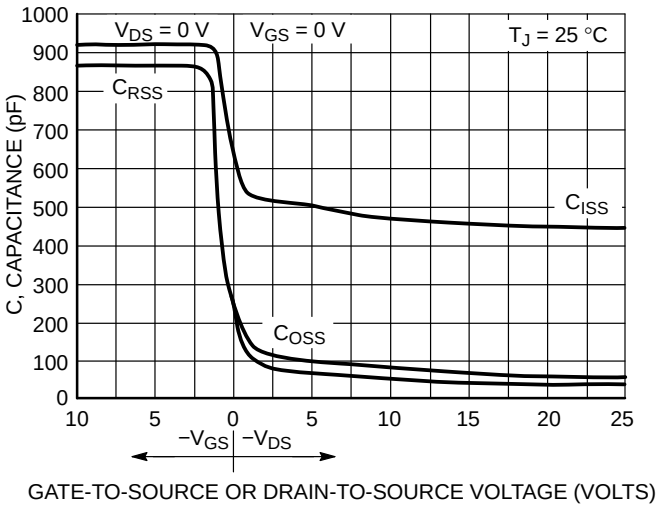


Figure 7. Capacitance Variation

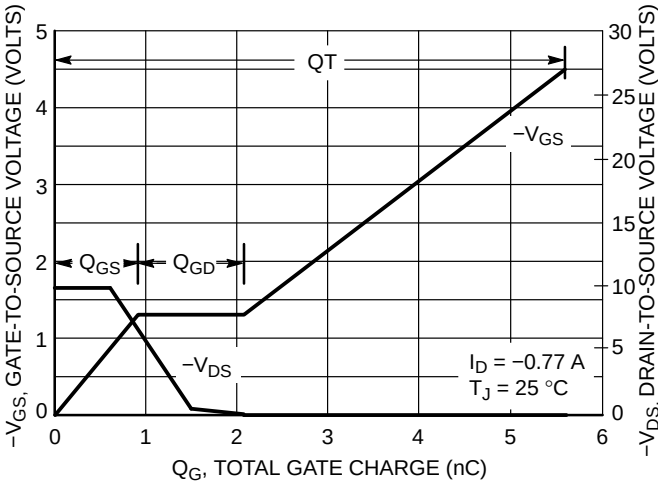


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

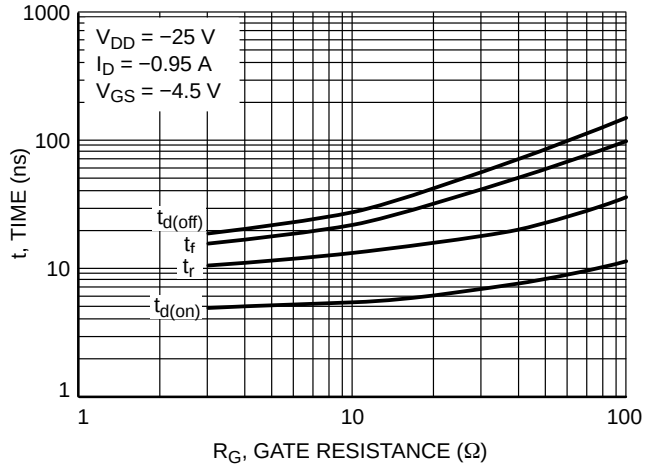


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

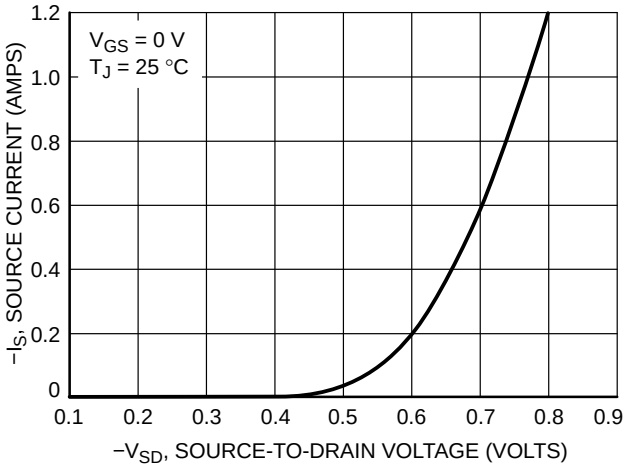


Figure 10. Diode Forward Voltage vs. Current

ORDERING INFORMATION

Device	Package	Shipping
NTZS3151PT1G	SOT-563 (Pb-Free)	4000 / Tape & Reel

DISCONTINUED (Note 4)

NTZS3151PT1H	SOT-563 (Pb-Free)	4000 / Tape & Reel
NTZS3151PT5G	SOT-563 (Pb-Free)	8000 / Tape & Reel

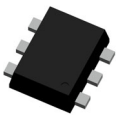
† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

4. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

REVISION HISTORY

Revision	Description of Changes	Date
4	Rebranded the Data Sheet to **onsemi** format. NTZS3151PT1H, NTZS3151PT5G OPN marked as Discontinued.	10/16/2025

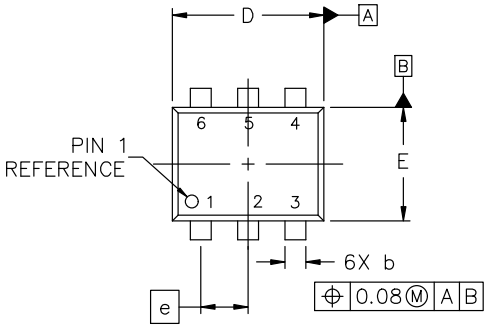
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



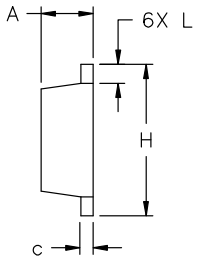
SOT−563−6 1.60x1.20x0.55, 0.50P
CASE 463A
ISSUE J

DATE 15 FEB 2024

NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

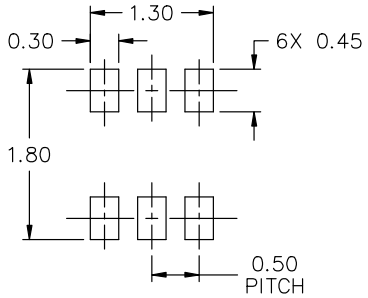


TOP VIEW



SIDE VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.50	1.60	1.70
E	1.10	1.20	1.30
e	0.50 BSC		
H	1.50	1.60	1.70
L	0.10	0.20	0.30



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

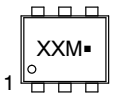
STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOT−563−6 1.60x1.20x0.55, 0.50P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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