

MOSFET - Symmetrical Dual N-Channel

40 V, 4.5 mΩ, 60 A

NTTFD4D0N04HL

General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q2) and synchronous (Q1) have been designed to provide optimal power efficiency.

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 4.5 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$
- Max $r_{DS(on)}$ = 7 mΩ at $V_{GS} = 4.5$, $I_D = 8.0\text{ A}$

Q2: N-Channel

- Max $r_{DS(on)}$ = 4.5 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$
- Max $r_{DS(on)}$ = 7 mΩ at $V_{GS} = 4.5$, $I_D = 8.0\text{ A}$
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- RoHS Compliant

Typical Applications

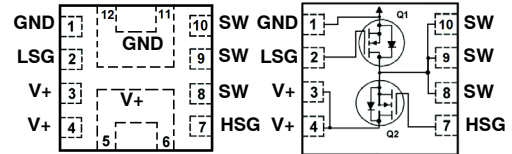
- Computing
- Communications
- General Purpose Point of Load

PIN DESCRIPTION

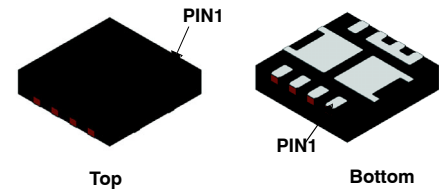
Pin	Name	Description
1, 11, 12	GND (LSS)	Low Side Source
2	LSG	Low Side Gate
3, 4, 5, 6	V + (HSD)	High Side Drain
7	HSG	High Side Gate
8, 9, 10	SW	Switching Node, Low Side Drain

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
40 V	4.5 mΩ @ 10 V	60 A
	7 mΩ @ 4.5 V	

ELECTRICAL CONNECTION



Dual N-Channel MOSFET



WQFN12, 3x3
CASE 510CJ

MARKING DIAGRAM



- D4D0 = Specific Device Code
- A = Assembly Plant Code
- Y = Numeric Year Code
- WW = Work Week Code
- ZZ = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping [†]
NTTFD4D0N04HLTWG	WQFN12 (Pb-Free)	3000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

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MOSFET MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$, Unless otherwise specified)

Symbol	Parameter	Q1	Q2	Unit	
V_{DS}	Drain-to-Source Voltage	40	40	V	
V_{GS}	Gate-to-Source Voltage	± 20	± 20	V	
I_D	Drain Current $T_C = 25\text{ }^\circ\text{C}$	-Continuous (Note 4)	60	60	A
	-Continuous	$T_C = 100\text{ }^\circ\text{C}$ (Note 4)	37	37	
	-Continuous	$T_A = 25\text{ }^\circ\text{C}$	15 (Note 1a)	15 (Note 1b)	
	-Pulsed	$T_A = 25\text{ }^\circ\text{C}$	349	349	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	67	67	mJ	
P_D	Power Dissipation for Single Operation $T_C = 25\text{ }^\circ\text{C}$	26	26	W	
	Power Dissipation for Single Operation $T_A = 25\text{ }^\circ\text{C}$	1.7 (Note 1a)	1.7 (Note 1b)		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	4.8	4.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a), max copper	70 (Note 1a)	70 (Note 1b)	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1c), min copper	135 (Note 1a)	135 (Note 1b)	

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-to-Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	Q1	40			V
		$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	Q2	40			
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$	Q1		16.63		mV/ $^\circ\text{C}$
		$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$	Q2		16.63		
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	Q1			10	μA
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	Q2			10	
I_{GSS}	Gate-to-Source Leakage Current, Forward	$V_{GS} = +20/-16\text{ V}, V_{DS} = 0\text{ V}$	Q1			± 100	nA
		$V_{GS} = +20/-16\text{ V}, V_{DS} = 0\text{ V}$	Q2			± 100	

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ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 50\text{ }\mu\text{A}$	Q1	1.2	1.5	2.0	V
		$V_{GS} = V_{DS}, I_D = 50\text{ }\mu\text{A}$	Q2	1.2	1.5	2.0	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate-to-Source Threshold Voltage Temperature Coefficient	$I_D = 50\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$	Q1		-5.75		mV/ $^\circ\text{C}$
		$I_D = 50\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$	Q2		-5.75		
$r_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Q1		3.7	4.5	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$			5.8	7	
		$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$			6.4		
$r_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Q2		3.7	4.5	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$			5.8	7	
		$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$			6.4		
g_{FS}	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$	Q1		61		S
		$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$	Q2		61		

DYNAMIC CHARACTERISTICS

C_{ISS}	Input Capacitance	Q1: $V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ Mhz}$	Q1		1100		pF
			Q2		1100		
C_{OSS}	Output Capacitance	Q2: $V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1		271		pF
			Q2		271		
C_{RSS}	Reverse Transfer Capacitance		Q1		22		pF
			Q2		22		
R_G	Gate Resistance	$T_A = 25\text{ }^\circ\text{C}$	Q1		2.0		Ω
			Q2		2.0		

SWITCHING CHARACTERISTICS

$t_{d(ON)}$	Turn-On Delay Time	Q1: $V_{DD} = 32\text{ V}, I_D = 30.5\text{ A}$, $V_{GS} = 4.5\text{ V}, R_{GEN} = 2.5\text{ }\Omega$	Q1		9.5		ns
			Q2		9.5		
t_r	Rise Time	Q2: $V_{DD} = 32\text{ V}, I_D = 30.5\text{ A}$, $V_{GS} = 4.5\text{ V}, R_{GEN} = 2.5\text{ }\Omega$	Q1		5.6		ns
			Q2		5.6		
$t_{D(OFF)}$	Turn-Off Delay Time		Q1		1.7		ns
			Q2		1.7		
t_f	Fall Time		Q1		5.8		ns
			Q2		5.8		
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	Q1		18		nC
			Q2		18		
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$	Q1		8.6		nC
			Q2		8.6		
Q_{gs}	Gate-to-Source Gate Charge	Q1: $V_{DD} = 32\text{ V}$, $I_D = 30.5\text{ A}$ Q2:	Q1		3.1		nC
			Q2		3.1		
Q_{gd}	Gate-to-Drain "Miller" Charge	$V_{DD} = 32\text{ V}$, $I_D = 30.5\text{ A}$	Q1		3.2		nC
			Q2		3.2		

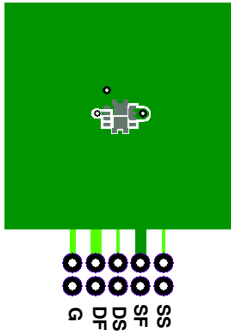
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ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) (continued)

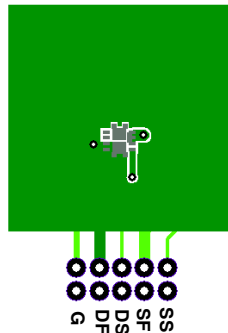
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$ (Note 2)	Q1		0.78	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$ (Note 2)	Q2		0.78	1.2	
t_{rr}	Reverse Recovery Time	Q1: $I_F = 30.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ Q2: $I_F = 30.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1		26		ns
			Q2		26		
Q_{rr}	Reverse Recovery Charge	$I_F = 30.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1		9		nC
			Q2		9		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

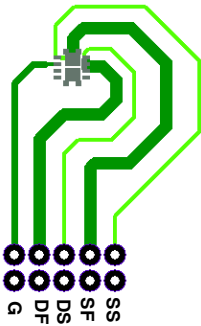
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



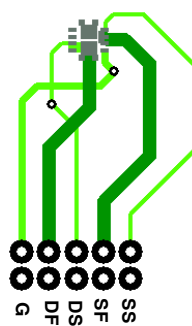
a) 70°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 70°C/W when mounted on a 1 in² pad of 2 oz copper.



c) 135°C/W when mounted on a minimum pad of 2 oz copper.



d) 135°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. Q1: E_{AS} of 67 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$; N-ch: $L = 1\text{ mH}$, $I_{AS} = 11.6\text{ A}$, $V_{DD} = 40\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 1\text{ mH}$, $I_{AS} = 11.6\text{ A}$.
Q2: E_{AS} of 67 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$; N-ch: $L = 1\text{ mH}$, $I_{AS} = 11.6\text{ A}$, $V_{DD} = 40\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 1\text{ mH}$, $I_{AS} = 11.6\text{ A}$.

4. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS

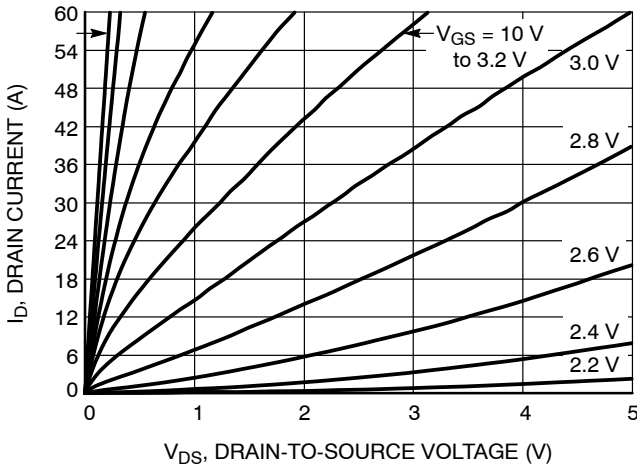


Figure 1. On-Region Characteristics

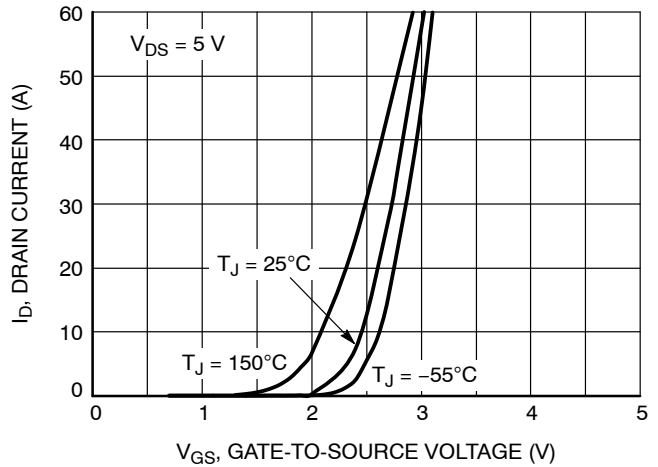


Figure 2. Transfer Characteristics

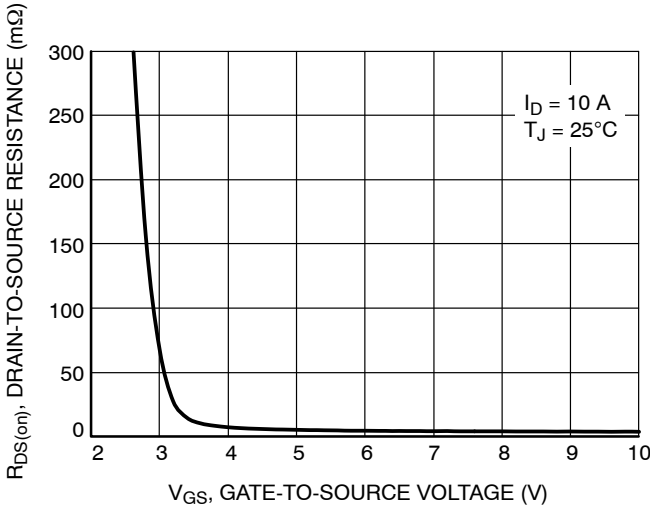


Figure 3. On-Resistance vs. Gate-to-Source Voltage

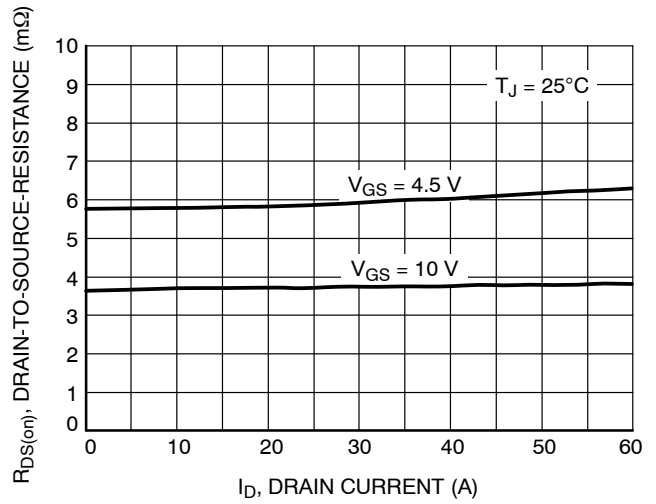


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

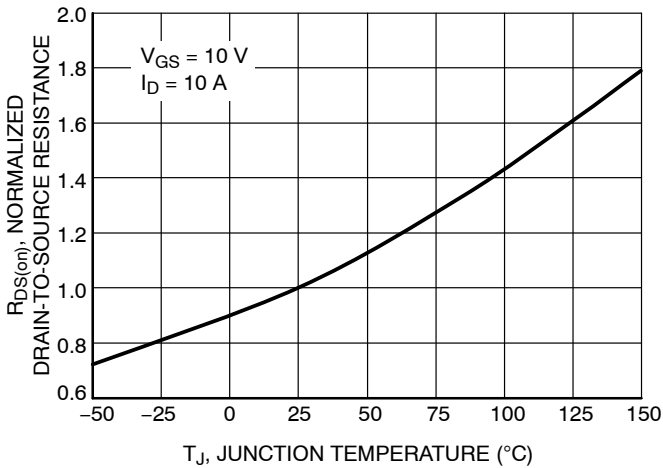


Figure 5. On-Resistance Variation with Temperature

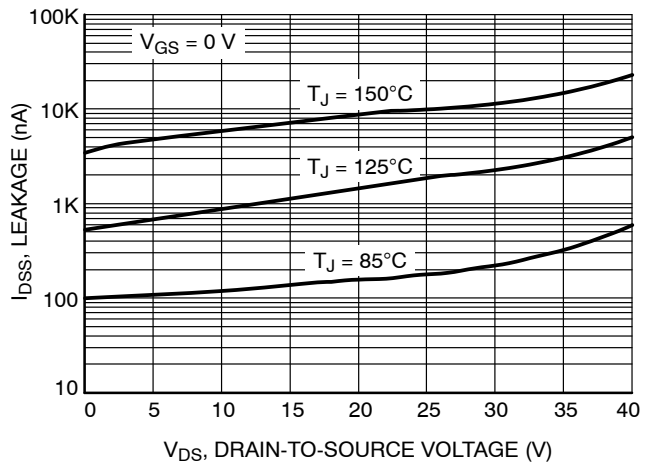


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

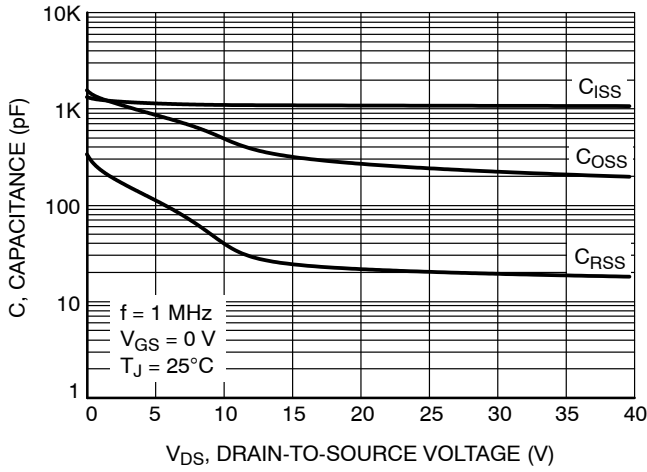


Figure 7. Capacitance Variation

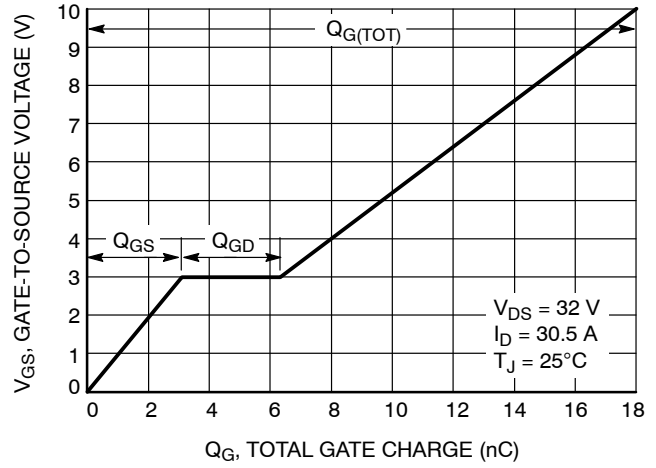


Figure 8. Gate-to-Source vs. Total Charge

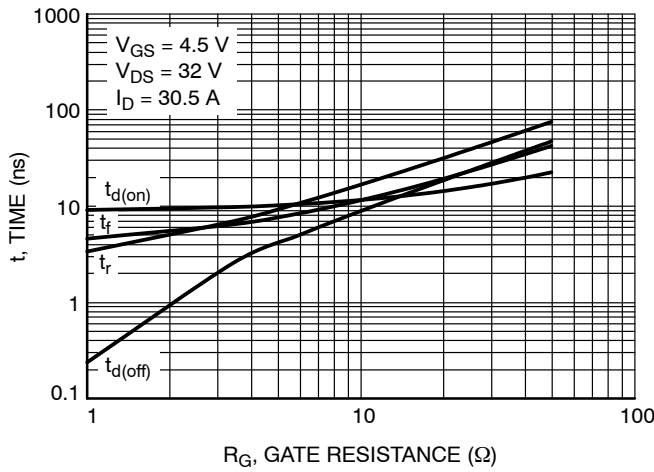


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

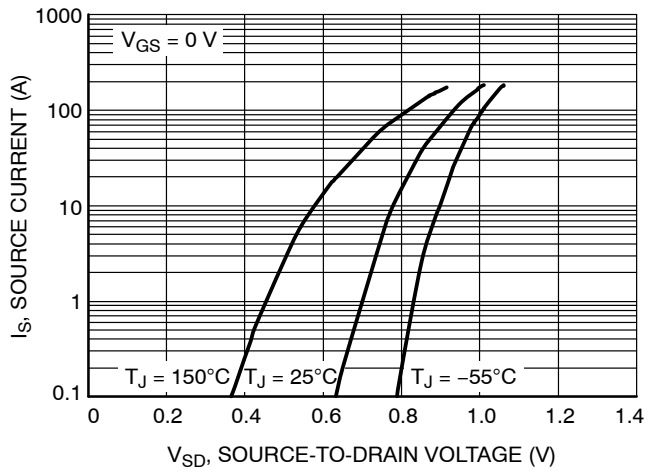


Figure 10. Diode Forward Voltage vs. Current

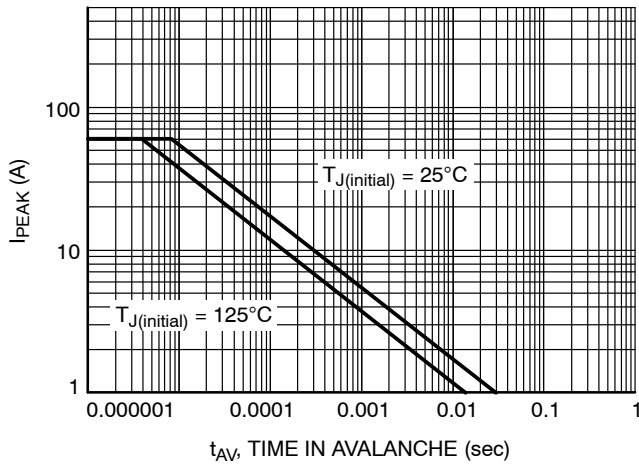


Figure 11. Unclamped Inductive Switching Capability

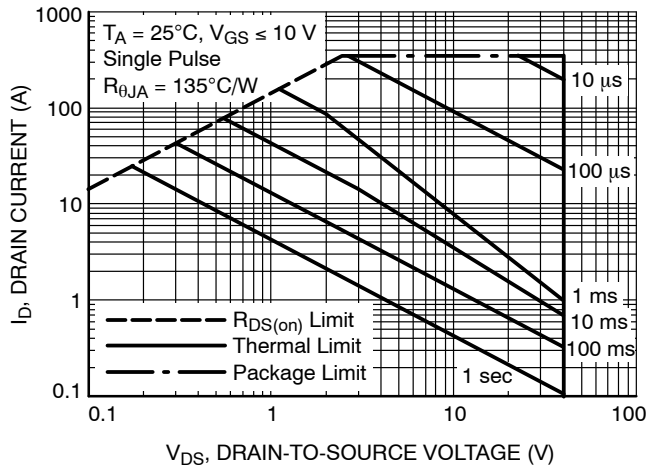


Figure 12. Forward Bias Safe Operating Area

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TYPICAL CHARACTERISTICS

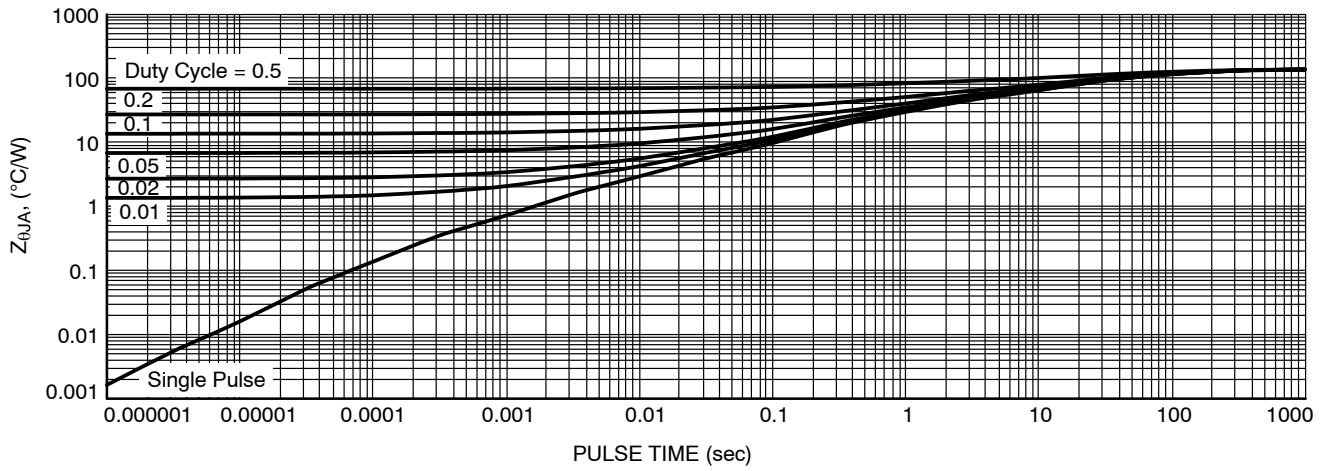


Figure 13. Transient Thermal Impedance

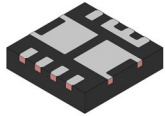
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REVISION HISTORY

Revision	Description of Changes	Date
3	Updated for synchronous MOSFET(Q1) body-diode symbol.	06/30/2025

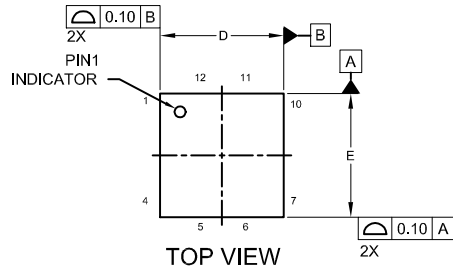
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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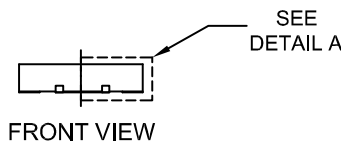


WQFN12 3.3X3.3, 0.65P
CASE 510CJ
ISSUE A

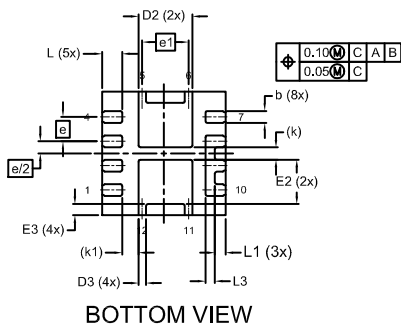
DATE 08 AUG 2022



TOP VIEW

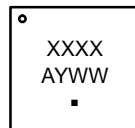


FRONT VIEW



BOTTOM VIEW

GENERIC
MARKING DIAGRAM*

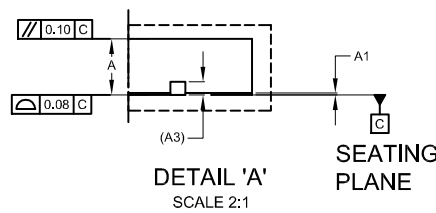


- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

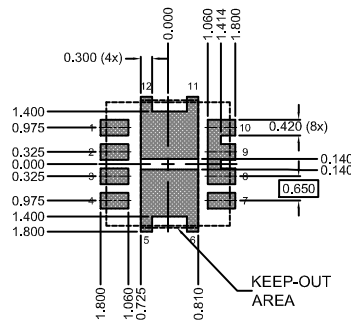
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
5. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DETAIL 'A'
SCALE 2:1



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	--	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	1.34	1.44	1.54
D3	0.10	0.20	0.30
E	3.20	3.30	3.40
E2	1.09	1.19	1.29
E3	0.20	0.30	0.40
e	0.65 BSC		
e/2	0.325 BSC		
e1	1.24 BSC		
k	0.33 REF		
k1	0.43 REF		
L	0.44	0.54	0.64
L1	0.19	0.29	0.39
L3	0.15	0.25	0.35

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DESCRIPTION:	WQFN12 3.3X3.3, 0.65P	PAGE 1 OF 1

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