

MOSFET – Power, N-Channel POWERTRENCH® Power Clip 25 V Asymmetric Dual

NTTFD1D8N02P1E

Features

- Small Footprint (3.3 mm x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- DC-DC Converters
- System Voltage Rails

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

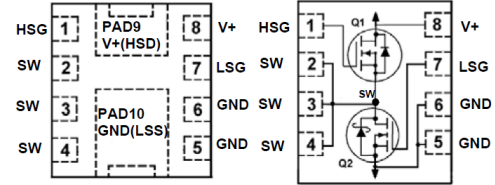
Parameter			Symbol	Q1	Q2	Unit
Drain-to-Source Voltage			V_{DS}	25	25	V
Gate-to-Source Voltage			V_{GS}	+16 -12	+16 -12	V
Continuous Drain Current $R_{\theta JC}$ (Note 3)	Steady State	$T_C = 250^\circ\text{C}$	I_D	61	126	A
		$T_C = 850^\circ\text{C}$		44	91	
Power Dissipation $R_{\theta JC}$ (Note 3)	Steady State	$T_A = 250^\circ\text{C}$	P_D	25	36	W
		$T_A = 850^\circ\text{C}$				
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 250^\circ\text{C}$	I_D	15	30	A
		$T_A = 850^\circ\text{C}$		11	21	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 250^\circ\text{C}$	P_D	1.6	2.0	W
		$T_A = 850^\circ\text{C}$				
Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)	Steady State	$T_A = 250^\circ\text{C}$	I_D	11	21	A
		$T_A = 850^\circ\text{C}$		8	15	
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)	Steady State	$T_A = 250^\circ\text{C}$	P_D	0.8	0.9	W
		$T_A = 850^\circ\text{C}$				
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$		I_{DM}	483	861	A
Single Pulse Drain-to-Source Avalanche Energy Q1: $I_L = 15.8 A_{pk}, L = 0.3 \text{ mH}$ (Note 4) Q2: $I_L = 31.63 A_{pk}, L = 0.3 \text{ mH}$ (Note 4)			E_{AS}	37.3	150.1	mJ
Operating Junction and Storage Temperature			T_J, T_{stg}	-55 to + 150		$^\circ\text{C}$
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in² pad size, 2 oz. Cu pad.
2. Surface-mounted on FR4 board using minimum pad size, 2 oz. Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro-mechanical application board design. $R_{\theta JC}$ is determined by the user's board design.
4. Q1 100% UIS tested at $L = 0.1 \text{ mH}$, $I_{AS} = 24.2 \text{ A}$.
Q2 100% UIS tested at $L = 0.1 \text{ mH}$, $I_{AS} = 48.1 \text{ A}$.
5. This device does not have ESD protection diode.

FET	$V_{(BR)DS}$	$R_{DS(ON)}$ MAX	I_D MAX
Q1	25 V	4.2 m Ω @ 10 V	61 A
		5.3 m Ω @ 4.5 V	
Q2	25 V	1.4 m Ω @ 10 V	126 A
		1.8 m Ω @ 4.5 V	

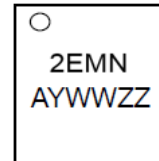
ELECTRICAL CONNECTION



MARKING DIAGRAM



PQFN12 3.3x3.3
CASE 483AZ



2EMN = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping†
NTTFD1D8N02P1E	PQFN8 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Q1 Max	Q2 Max	Unit
Junction-to-Case – Steady State (Notes 1, 3)	$R_{\theta JC}$	5.0	3.5	°C/W
Junction-to-Ambient – Steady State (Notes 1, 3)	$R_{\theta JA}$	77	63	
Junction-to-Ambient – Steady State (Notes 2, 3)	$R_{\theta JA}$	158	132	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	FET	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Q1	25			V
		$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	Q2	25			
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C	Q1		16		mV/°C
		$I_D = 1\text{ mA}$, ref to 25°C	Q2		16		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$	$T_J = 25^\circ\text{C}$	Q1		10	μA
				Q2		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = +16\text{ V} / -12\text{ V}$	Q1			± 100	nA
		$V_{DS} = 0\text{ V}, V_{GS} = +16\text{ V} / -12\text{ V}$	Q2			± 100	

ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 190\text{ }\mu\text{A}$	Q1	1.2		2.0	V
		$V_{GS} = V_{DS}, I_D = 310\text{ }\mu\text{A}$	Q2	1.2		2.0	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 190\text{ }\mu\text{A}$, ref to 25°C	Q1		-4.4		mV/°C
		$I_D = 310\text{ }\mu\text{A}$, ref to 25°C	Q2		-4.7		
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	Q1		3.3	4.2	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 13\text{ A}$			4.2	5.3	
		$V_{GS} = 10\text{ V}, I_D = 29\text{ A}$	Q2		1.04	1.4	
		$V_{GS} = 4.5\text{ V}, I_D = 26\text{ A}$			1.34	1.8	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 15\text{ A}$	Q1		105		S
		$V_{DS} = 5\text{ V}, I_D = 29\text{ A}$	Q2		207		
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$	Q1		0.54		Ω
			Q2		0.45		

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, V _{DS} = 13 V, f = 1 MHz	Q1		873		pF
			Q2		2700		
Output Capacitance	C _{OSS}		Q1		243		pF
			Q2		748		
Reverse Transfer Capacitance	C _{RSS}		Q1		19		pF
			Q2		48		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

7. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	FET	Min	Typ	Max	Unit
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CHARGES, CAPACITANCES & GATE RESISTANCE

Total Gate Charge	Q _{G(TOT)}	Q1: V _{GS} = 4.5 V, V _{DS} = 13 V; I _D = 15 A Q2: V _{GS} = 4.5 V, V _{DS} = 13 V; I _D = 29 A	Q1		5.5		nC
			Q2		17		
Gate-to-Drain Charge	Q _{GD}		Q1		1.0		nC
			Q2		2.7		
Gate-to-Source Charge	Q _{GS}		Q1		2.4		nC
			Q2		7.3		
Total Gate Charge	Q _{G(TOT)}	Q1: V _{GS} = 10 V, V _{DS} = 13 V; I _D = 15 A	Q1		12		nC
		Q2: V _{GS} = 10 V, V _{DS} = 13 V; I _D = 29 A	Q2		37.5		

SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 7)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V Q1: I _D = 15 A, V _{DD} = 13 V, R _G = 6 Ω Q2: I _D = 29 A, V _{DD} = 13 V, R _G = 6 Ω	Q1		9.5		ns
			Q2		19.1		
Rise Time	t _r		Q1		2.3		ns
			Q2		6.6		
Turn-Off Delay Time	t _{d(OFF)}		Q1		12.6		ns
			Q2		26.3		
Fall Time	t _f		Q1		2.7		ns
			Q2		6.3		

SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 7)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V Q1: I _D = 15 A, V _{DD} = 13 V, R _G = 6 Ω Q2: I _D = 29 A, V _{DD} = 13 V, R _G = 6 Ω	Q1		6.6		ns
			Q2		9.4		
Rise Time	t _r		Q1		1.1		ns
			Q2		2.3		
Turn-Off Delay Time	t _{d(OFF)}		Q1		17.3		ns
			Q2		37.6		
Fall Time	t _f		Q1		1.7		ns
			Q2		5.2		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 15 A	T _J = 25 °C	Q1		0.80	1.2	V
			T _J = 125 °C			0.70		
		V _{GS} = 0 V, I _S = 29 A	T _J = 25 °C	Q2		0.80	1.2	
			T _J = 125 °C			0.69		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V Q1: I _S = 15 A, dI _S /dt = 100 A/μs Q2: I _S = 29 A, dI _S /dt = 100 A/μs		Q1		19		ns
				Q2		35		
Reverse Recovery Charge	Q _{RR}			Q1		6.0		nC
				Q2		21		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

7. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS – Q1

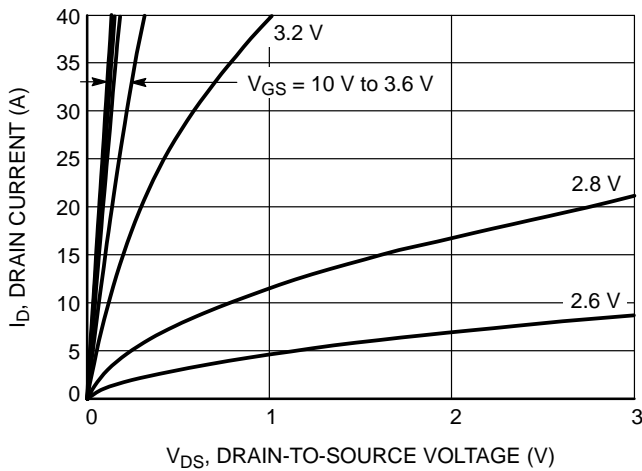


Figure 1. On-Region Characteristics

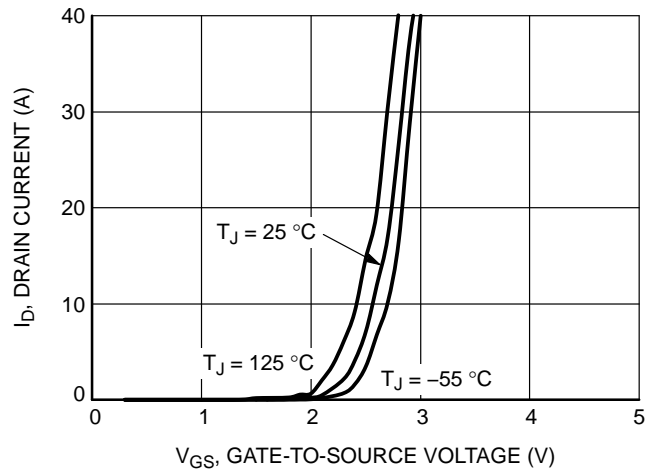


Figure 2. Transfer Characteristics

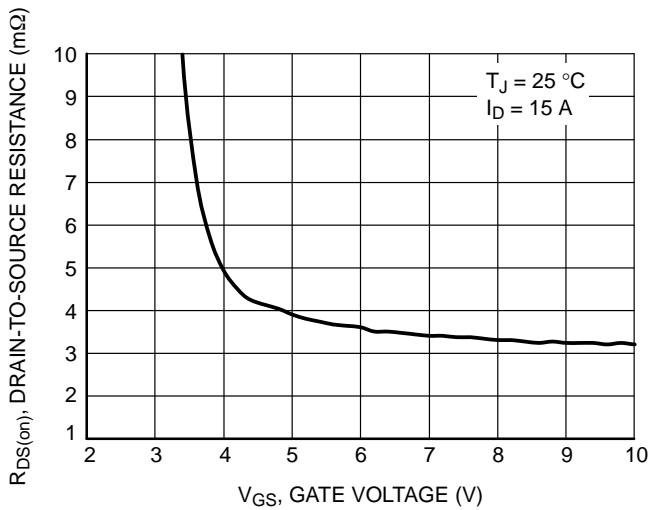


Figure 3. On-Resistance vs. Gate-to-Source Voltage

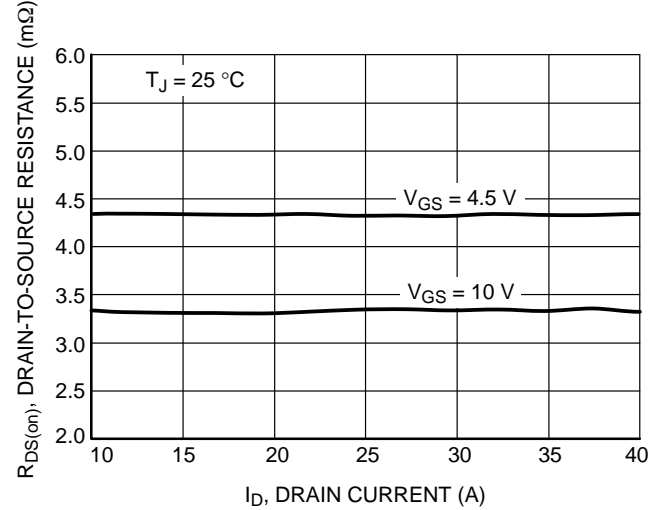


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

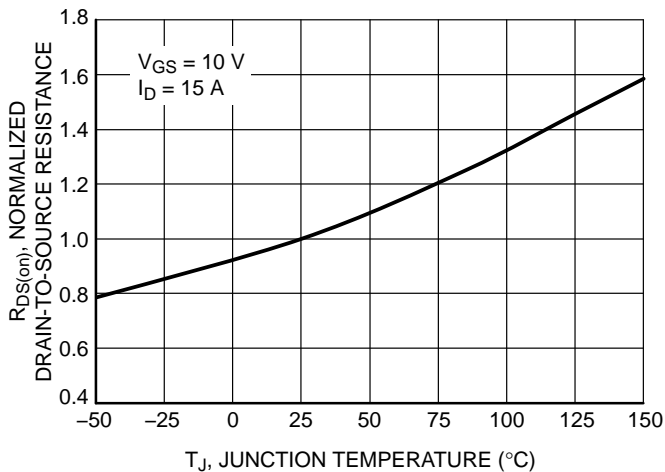


Figure 5. On-Resistance Variation with Temperature

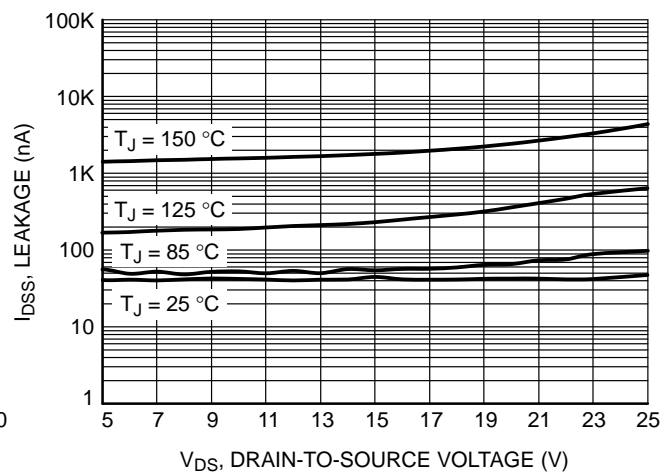


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – Q1

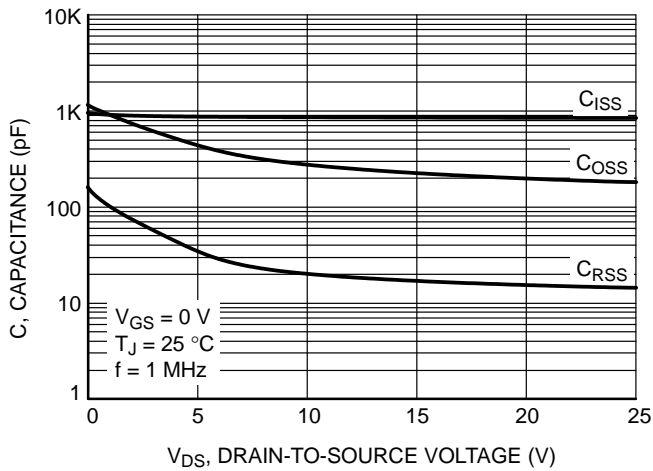


Figure 7. Capacitance Variation

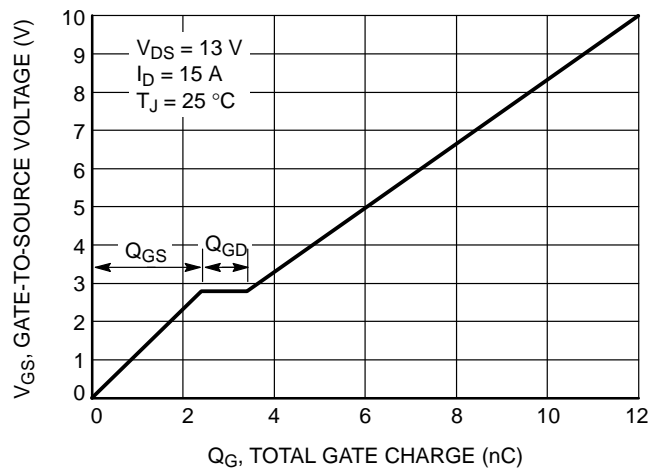


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

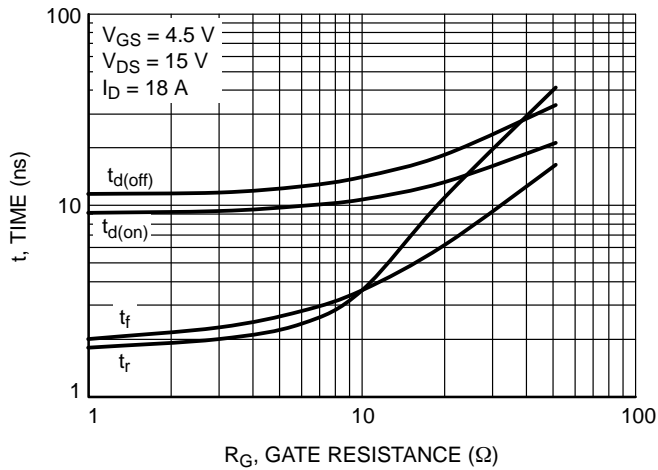


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

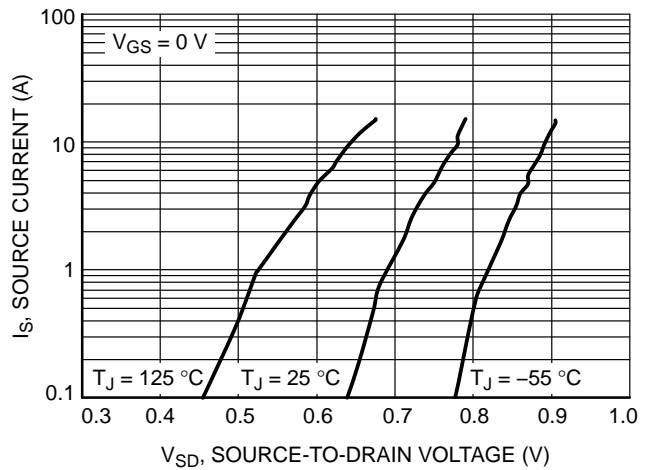


Figure 10. Diode Forward Voltage vs. Current

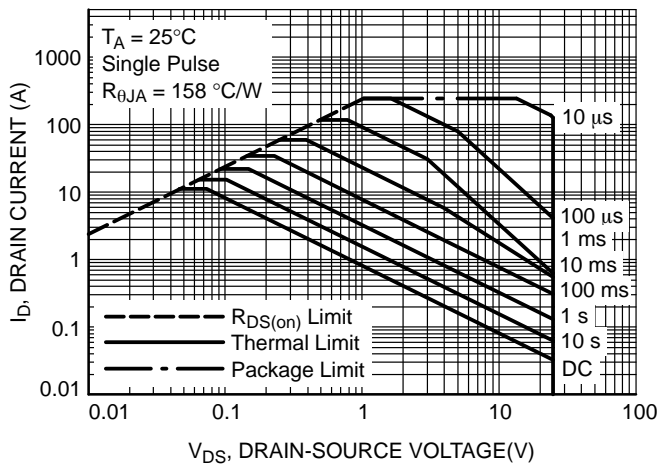


Figure 11. Safe Operating Area

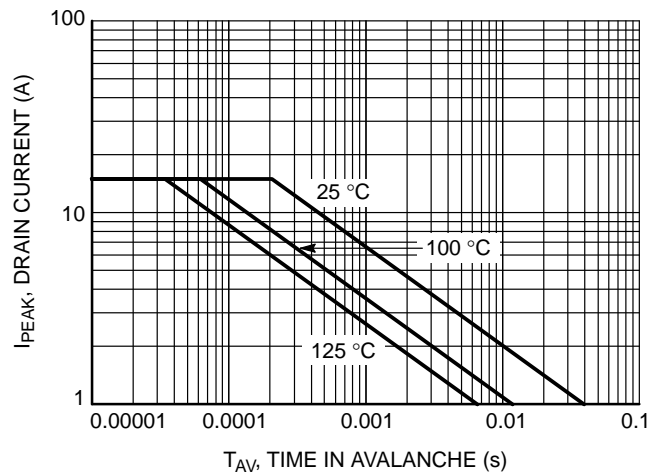


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS – Q1

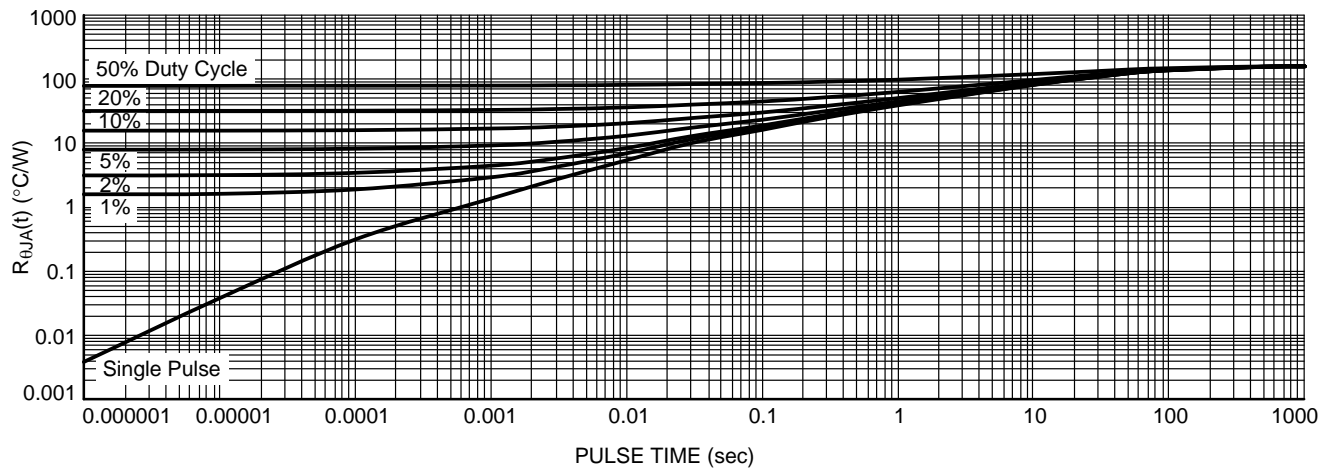


Figure 13. Thermal Characteristics

TYPICAL CHARACTERISTICS – Q2

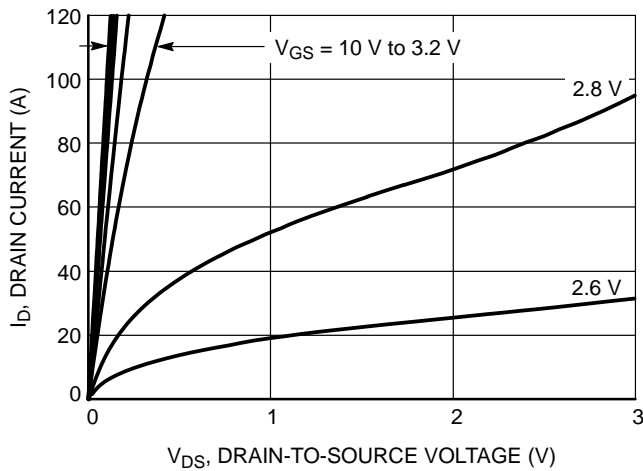


Figure 14. On-Region Characteristics

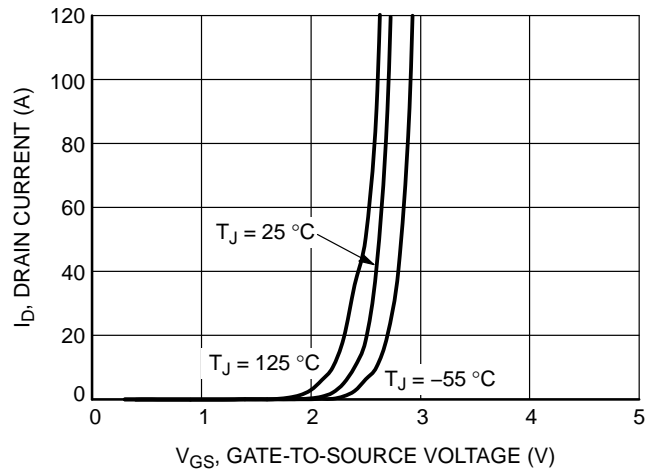


Figure 15. Transfer Characteristics

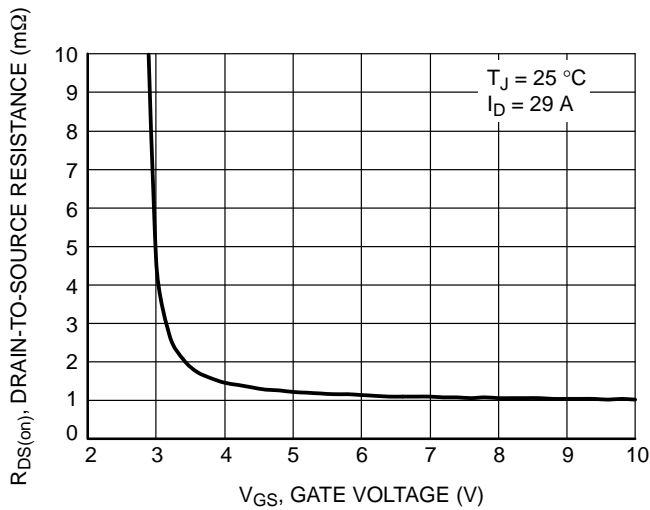


Figure 16. On-Resistance vs. Gate-to-Source Voltage

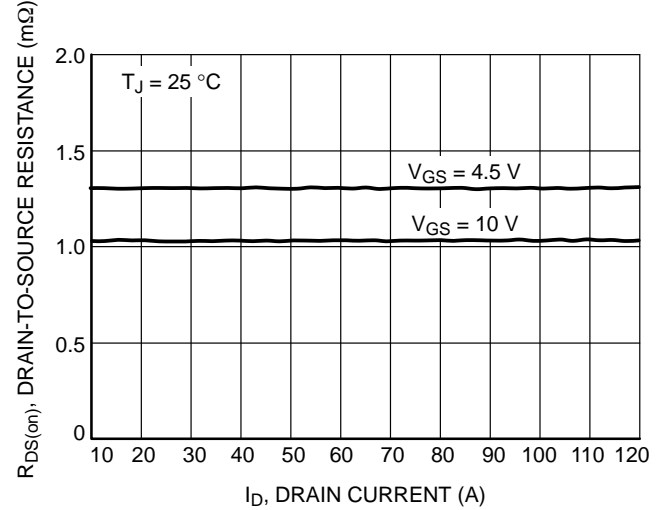


Figure 17. On-Resistance vs. Drain Current and Gate Voltage

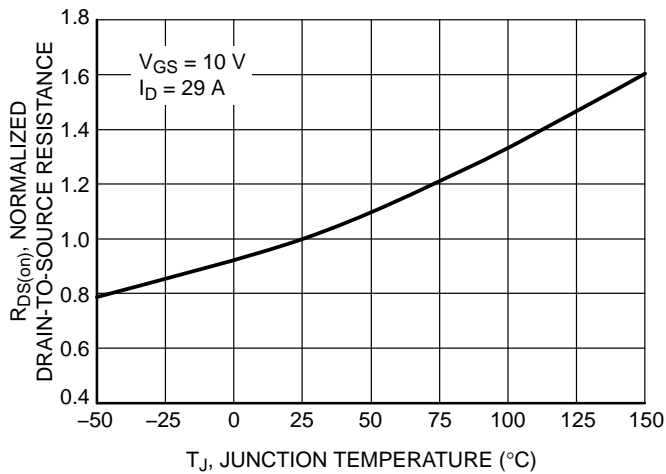


Figure 18. On-Resistance Variation with Temperature

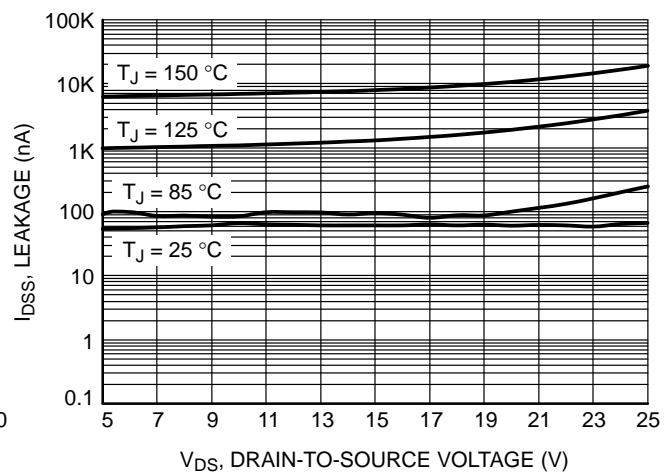


Figure 19. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – Q2

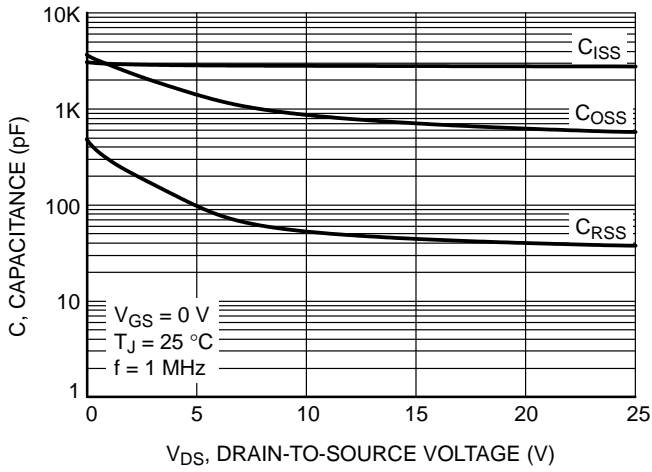


Figure 20. Capacitance Variation

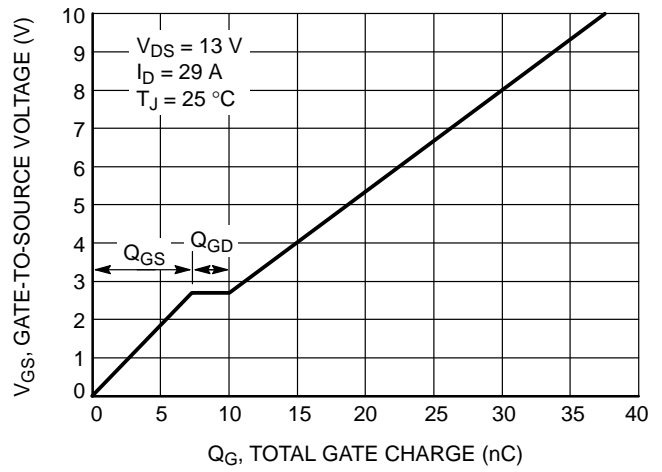


Figure 21. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

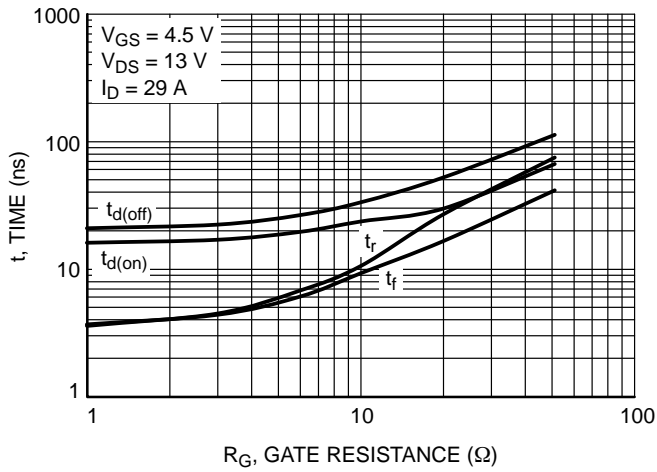


Figure 22. Resistive Switching Time Variation vs. Gate Resistance

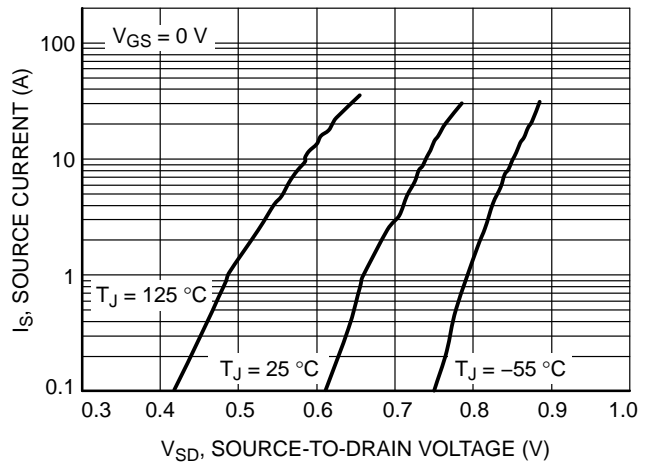


Figure 23. Diode Forward Voltage vs. Current

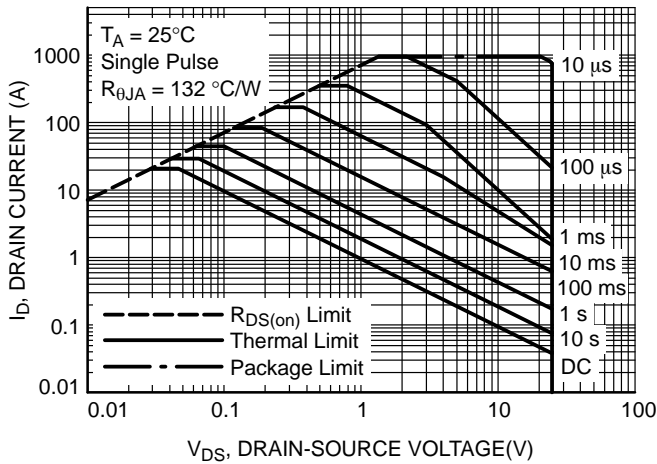


Figure 24. Safe Operating Area

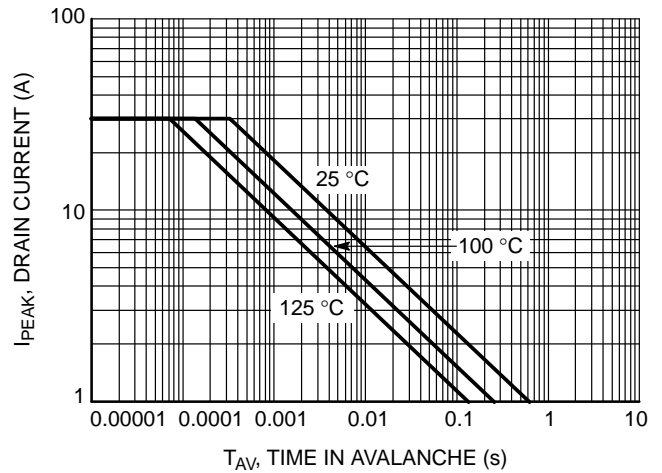


Figure 25. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS – Q2

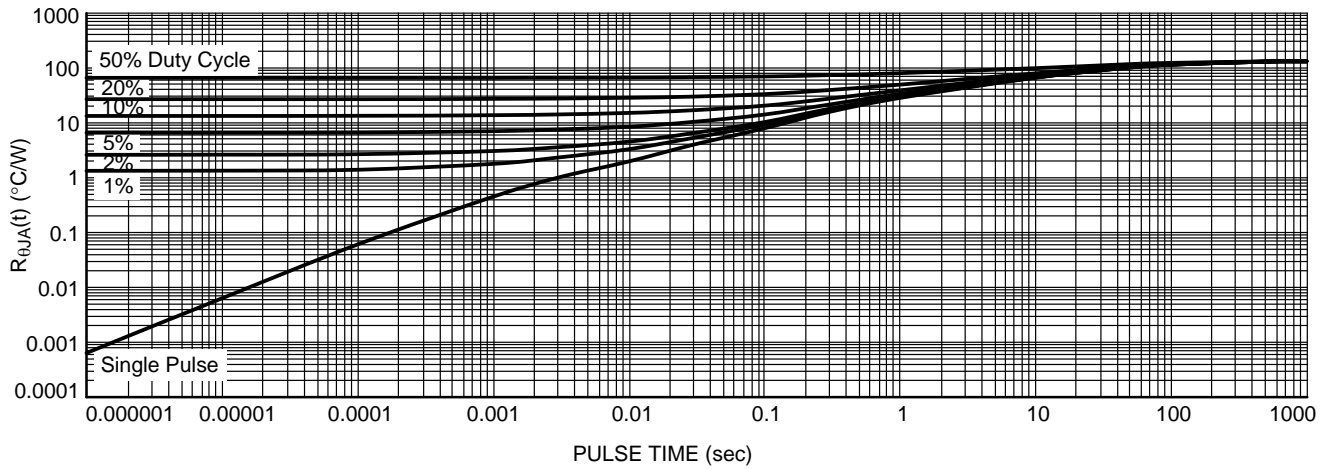
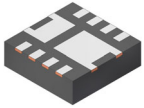


Figure 26. Thermal Characteristics

REVISION HISTORY

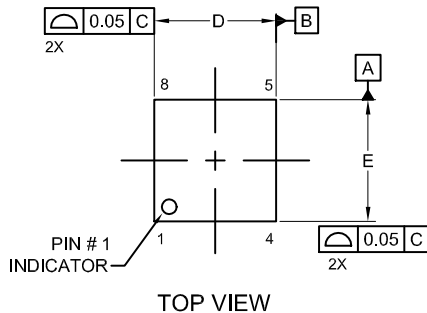
Revision	Description of Changes	Date
2	Rebranded the Data Sheet to onsemi format.	10/21/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

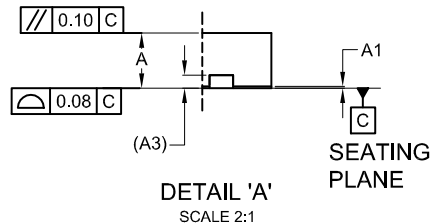


PQFN8 3.3X3.3, 0.65P
CASE 483AZ
ISSUE B

DATE 14 FEB 2022

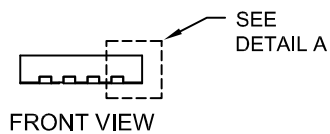


TOP VIEW

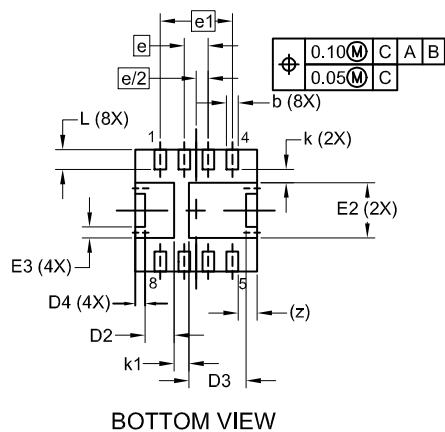


DETAIL 'A'

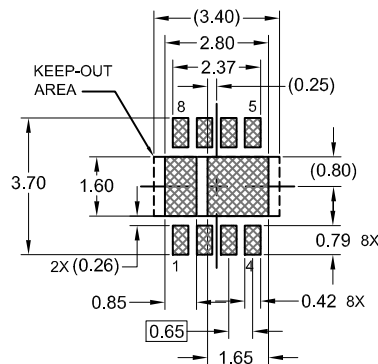
SCALE 2:1



FRONT VIEW



BOTTOM VIEW

LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	--	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	0.69	0.79	0.89
D3	1.45	1.55	1.65
D4	0.16	0.26	0.36
E	3.20	3.30	3.40
E2	1.40	1.50	1.60
E3	0.30 REF		
e	0.65 BSC		
e1	1.95 BSC		
e/2	0.325 BSC		
k	0.36 REF		
k1	0.40 REF		
L	0.44	0.54	0.64
z	0.52 REF		

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DESCRIPTION:	PQFN8 3.3X3.3, 0.65P	PAGE 1 OF 1

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