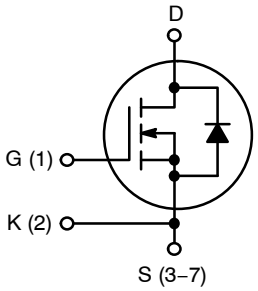
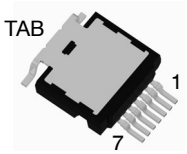
Silicon Carbide (SiC) MOSFET - EliteSiC, 16 mohm, 650 V, M3S, T2PAK

NTT2016N065M3S

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_D MAX
650 V	16 mΩ @ V_{GS} = 18 V	85 A



N-CHANNEL MOSFET



T2PAK-7
CASE 763AC

Features

- Typical $R_{DS(on)}$ = 16 mΩ @ V_{GS} = 18 V
- Ultra Low Gate Charge ($Q_{G(tot)}$ = 100 nC)
- High Speed Switching with Low Capacitance (C_{oss} = 208 pF)
- 100% Avalanche Tested
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

Applications

- SMPS, Solar Inverters, UPS, Energy Storages, EV Charging Infrastructure

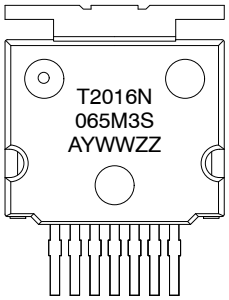
MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	650	V
Gate-to-Source Voltage		V_{GS}	−8/+22	V
Continuous Drain Current	T_C = 25 °C	I_D	85	A
Power Dissipation		P_D	333	W
Continuous Drain Current	T_C = 100 °C	I_D	62	A
Power Dissipation		P_D	167	W
Pulsed Drain Current (Note 1)	T_C = 25 °C, t_p = 100 µs	I_{DM}	178	A
Continuous Source-Drain Current (Body Diode)	T_C = 25 °C, V_{GS} = −3 V	I_S	49	A
	T_C = 100 °C, V_{GS} = −3 V		29	
Pulsed Source-Drain Current (Body Diode) (Note 1)	T_C = 25 °C, V_{GS} = −3 V, t_p = 100 µs	I_{SM}	198	A
Single Pulse Avalanche Energy (I_{LPK} = 60 A, L = 0.1 mH) (Note 2)		E_{AS}	180	mJ
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +175	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 seconds)		T_L	245	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Single pulse, limited by max junction temperature.
2. E_{AS} of 180 mJ is based on starting T_J = 25 °C, L = 0.1 mH, I_{AS} = 60 A, V_{DD} = 100 V, V_{GS} = 18 V.

MARKING DIAGRAM



NTT2016N065M3S = Specific Device Code
A = Assembly Site
WW = Work Week Number
Y = Year of Production, Last Number
ZZ = Assembly Lot Number, Last Two Numbers

ORDERING INFORMATION

Device	Package	Shipping†
NTT2016N065M3S	T2PAK-7L	800 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 3)	$R_{\theta JC}$	0.45	°C/W

3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

RECOMMENDED OPERTATING CONDITIONS

Parameter	Symbol	Value	Unit
Operation Values of Gate-to-Source Voltage	V_{GSop}	−3/18	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25 °C	650	–	–	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650 V, T_J = 25 °C	–	–	10	μA
		V_{DS} = 650 V, T_J = 175 °C (Note 5)	–	–	500	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = −10 V, V_{DS} = 0 V	−1	–	–	μA
		V_{GS} = +22 V, V_{DS} = 0 V	–	–	1	
ON CHARACTERISTICS						
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 18 V, I_D = 29 A, T_J = 25 °C	–	17	23.4	mΩ
		V_{GS} = 18 V, I_D = 29 A, T_J = 175 °C (Note 5)	–	26	–	
		V_{GS} = 15 V, I_D = 29 A, T_J = 25 °C	–	22	–	
		V_{GS} = 15 V, I_D = 29 A, T_J = 175 °C (Note 5)	–	29	–	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 15 mA, T_J = 25 °C	2.0	2.7	4.0	V
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 29 A (Note 5)	–	19	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz (Note 5)	–	2735	–	pF
Output Capacitance	C_{OSS}		–	208	–	
Reverse Transfer Capacitance	C_{RSS}		–	18	–	
Total Gate Charge	$Q_{G(TOT)}$	V_{DD} = 400 V, I_D = 29 A, V_{GS} = −3/18 V (Note 5)	–	100	–	nC
Gate-to-Source Charge	Q_{GS}		–	26	–	
Gate-to-Drain Charge	Q_{GD}		–	25	–	
Gate Resistance	R_G	f = 1 MHz	–	2.8	–	Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = −3/18 V, V_{DD} = 400 V, I_D = 30 A, R_G = 4.7 Ω, T_J = 25 °C, L_{stray} = 13 nH (Notes 4, 5)	–	25	–	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	54	–	
Rise Time	t_r		–	17	–	
Fall Time	t_f		–	10.5	–	
Turn-On Switching Loss	E_{ON}		–	146	–	μJ
Turn-Off Switching Loss	E_{OFF}		–	55	–	
Total Switching Loss	E_{TOT}		–	201	–	

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = −3/18 V, V_{DD} = 400 V, I_D = 30 A, R_G = 4.7 Ω, T_J = 175 °C, L_{stray} = 13 nH (Notes 4, 5)	–	30.6	–	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	63	–	
Rise Time	t_r		–	16	–	
Fall Time	t_f		–	11.5	–	
Turn-On Switching Loss	E_{ON}		–	150	–	μJ
Turn-Off Switching Loss	E_{OFF}		–	65	–	
Total Switching Loss	E_{TOT}		–	216	–	
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	I_{SD} = 29 A, V_{GS} = −3 V, T_J = 25 °C	–	4.5	6.0	V
		I_{SD} = 29 A, V_{GS} = −3 V, T_J = 175 °C (Note 5)	–	4.2	–	
Reverse Recovery Time	t_{RR}	V_{GS} = −3 V, I_S = 29 A, dI/dt = 1000 A/μs, V_{DS} = 400 V, T_J = 25 °C (Note 5)	–	23	–	ns
Charge Time	t_a		–	13	–	
Discharge Time	t_b		–	10	–	
Reverse Recovery Charge	Q_{RR}		–	146	–	nC
Reverse Recovery Energy	E_{REC}		–	12	–	μJ
Peak Reverse Recovery Current	I_{RRM}		–	11	–	A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. E_{ON}/E_{OFF} result is with body diode.
5. Defined by design, not subject to production test.

TYPICAL CHARACTERISTICS

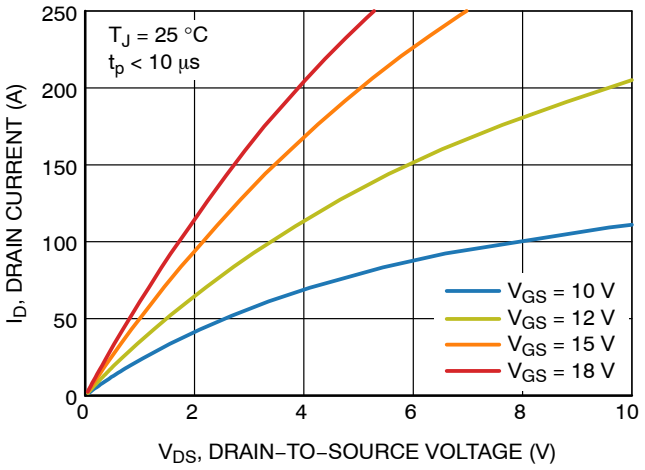


Figure 1. Output Characteristics

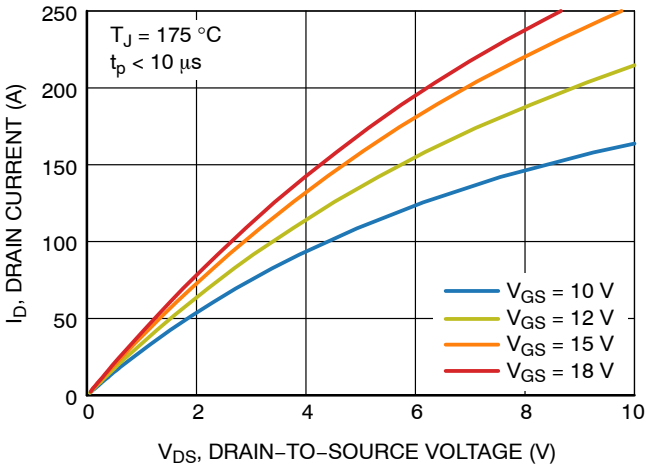


Figure 2. Output Characteristics

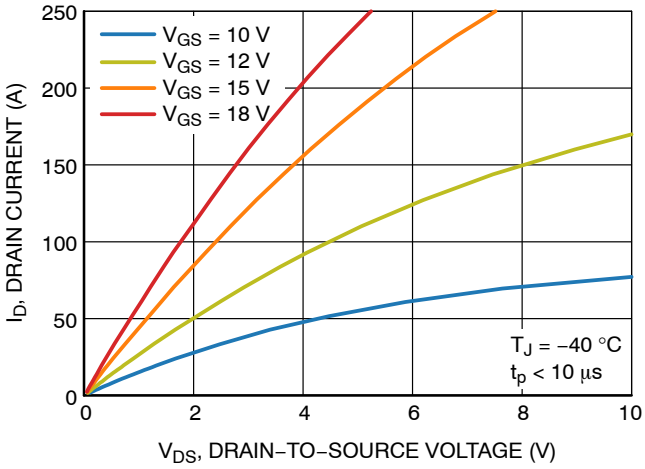


Figure 3. Output Characteristics

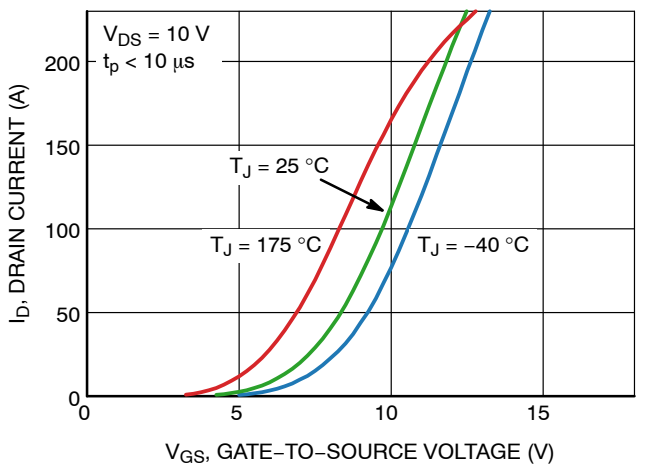


Figure 4. I_D vs. V_{GS}

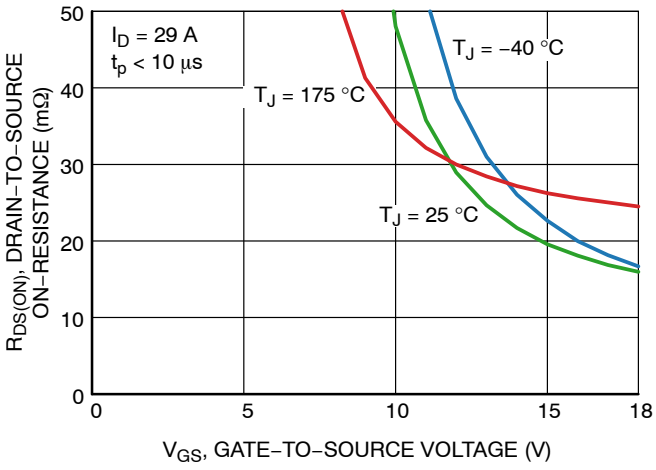


Figure 5. $R_{DS(ON)}$ vs. V_{GS}

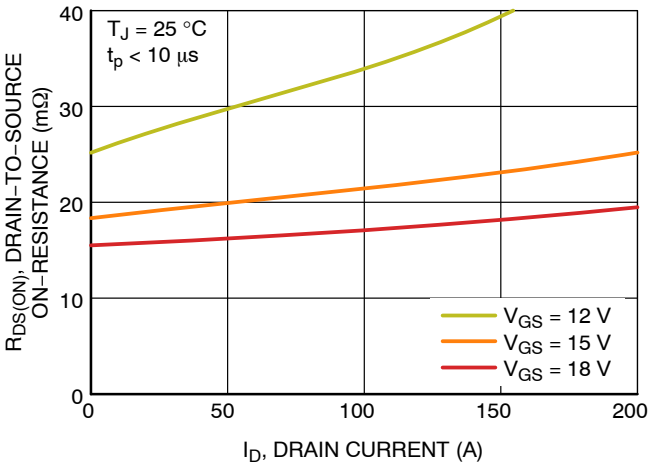


Figure 6. $R_{DS(ON)}$ vs. I_D

TYPICAL CHARACTERISTICS

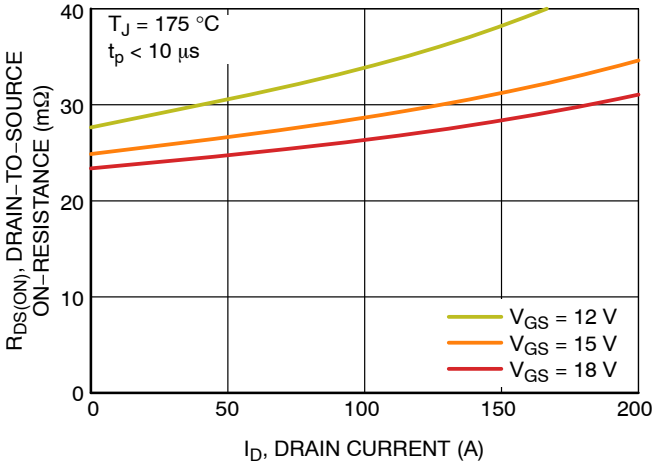


Figure 7. $R_{DS(ON)}$ vs. I_D

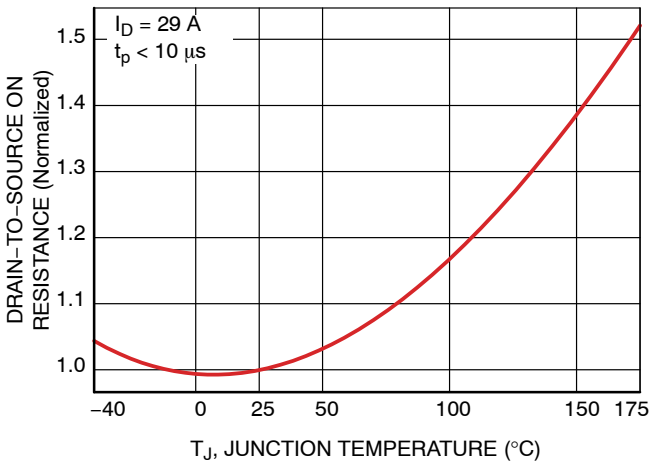


Figure 8. $R_{DS(ON)}$ vs. T_J

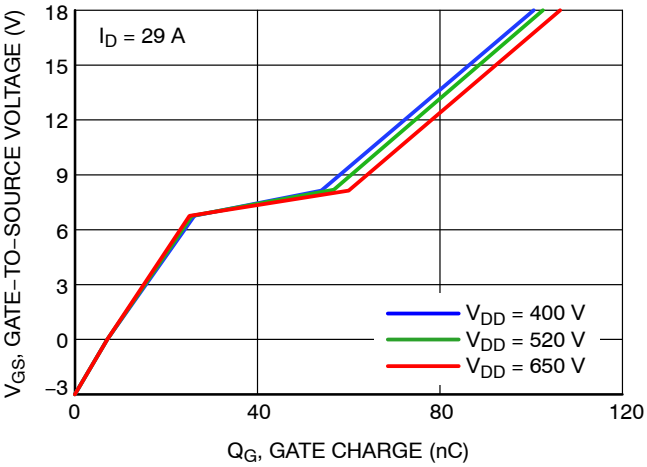


Figure 9. Gate Charge Characteristics

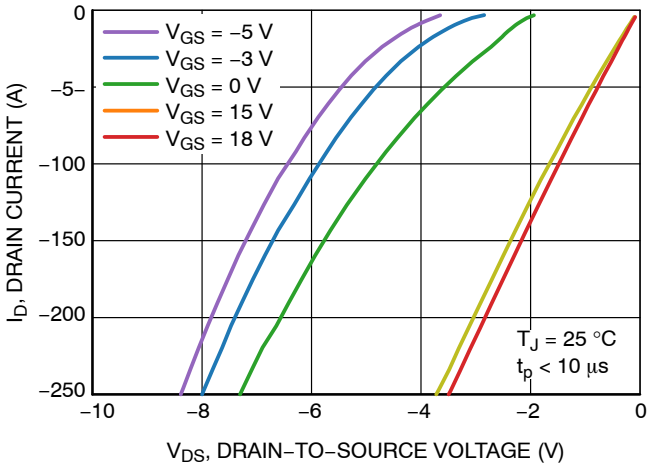


Figure 10. I_D vs. V_{DS}

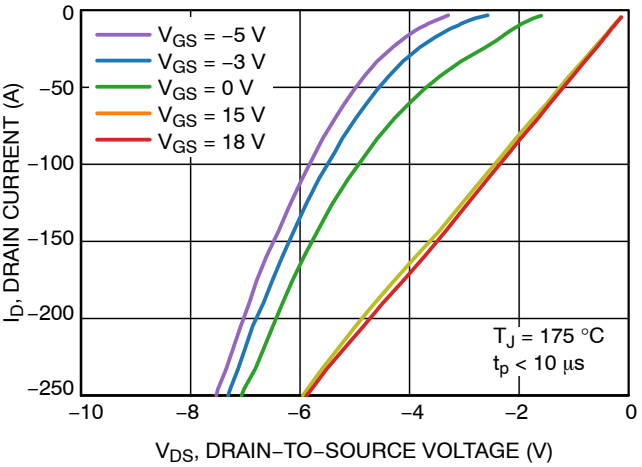


Figure 11. I_D vs. V_{DS}

TYPICAL CHARACTERISTICS

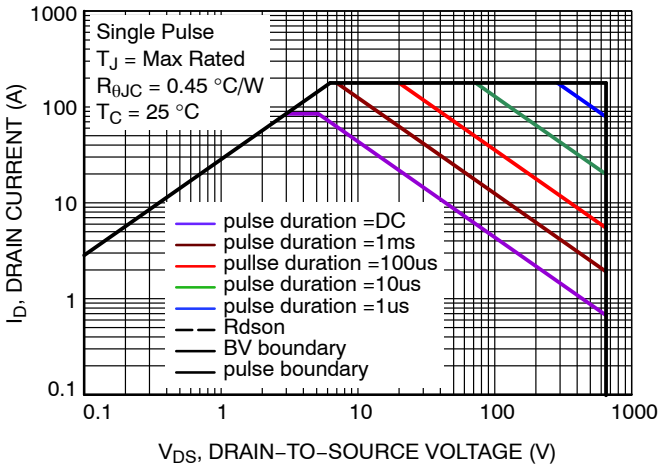


Figure 12. Safe Operating Area

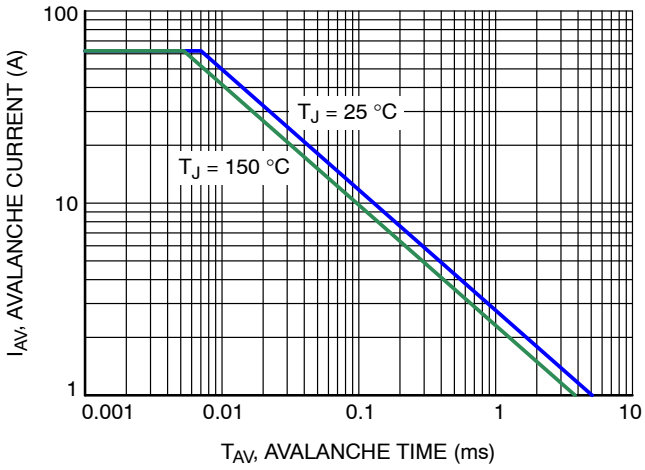


Figure 13. Avalanche Current vs. Pulse Time (UIS)

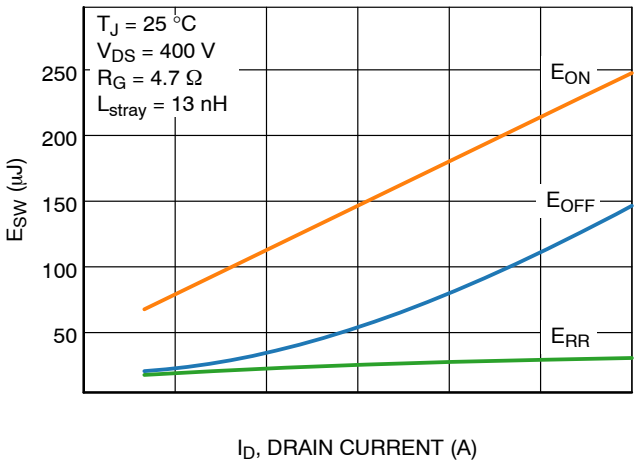


Figure 14. E_{SW} vs. I_D

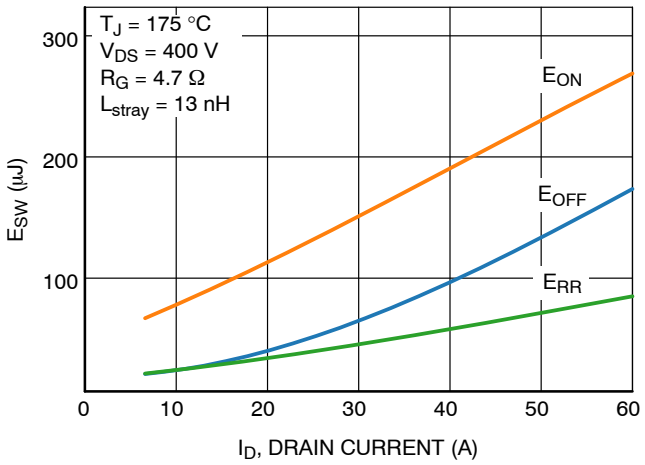


Figure 15. E_{SW} vs. I_D

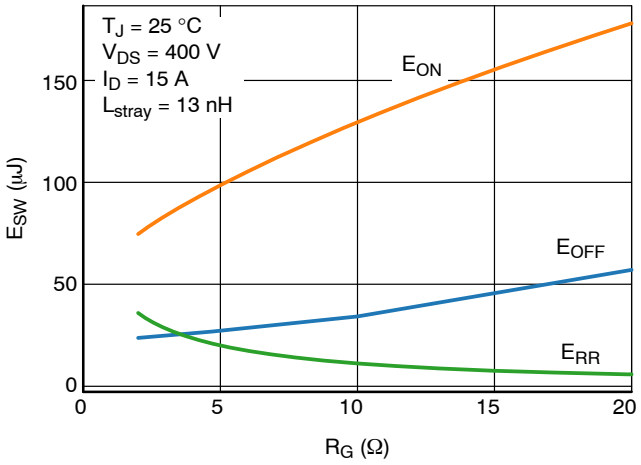


Figure 16. E_{SW} vs. R_G

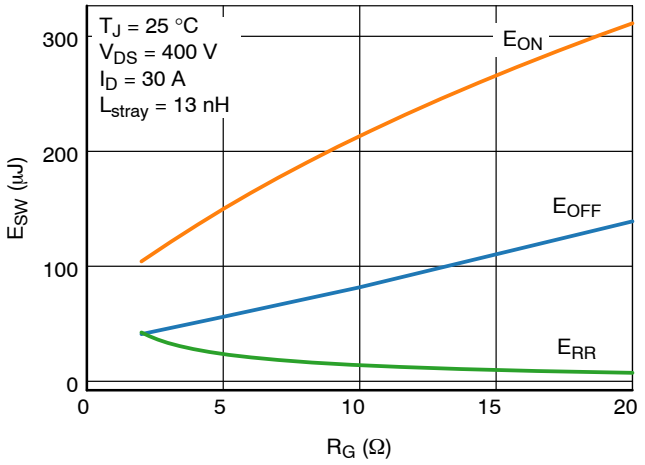


Figure 17. E_{SW} vs. R_G

TYPICAL CHARACTERISTICS

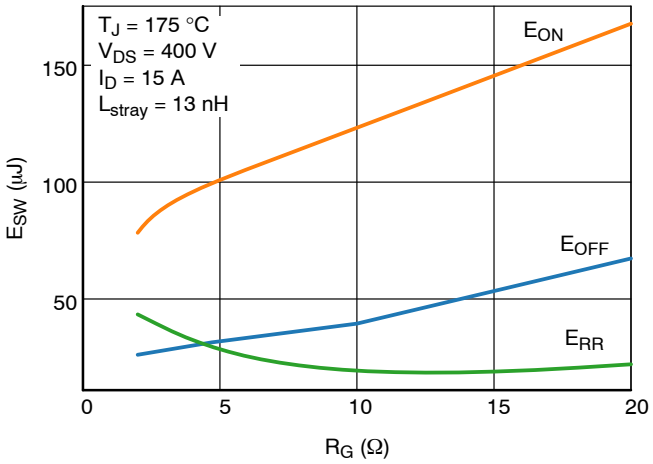


Figure 18. E_{SW} vs. R_G

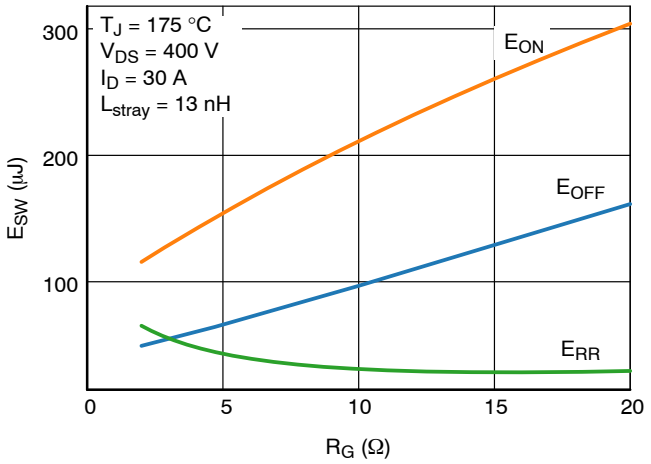


Figure 19. E_{SW} vs. R_G

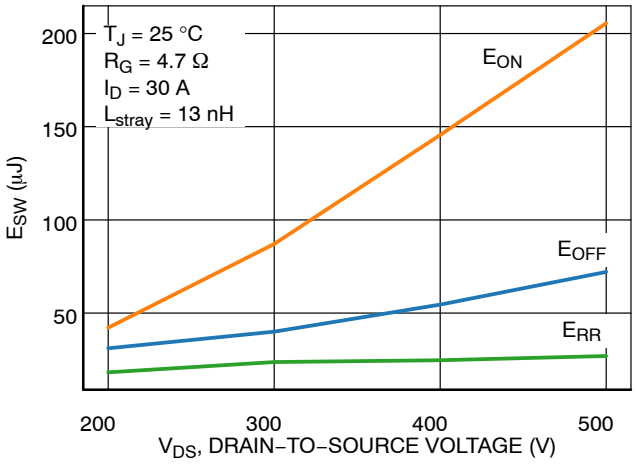


Figure 20. E_{SW} vs. V_{DS}

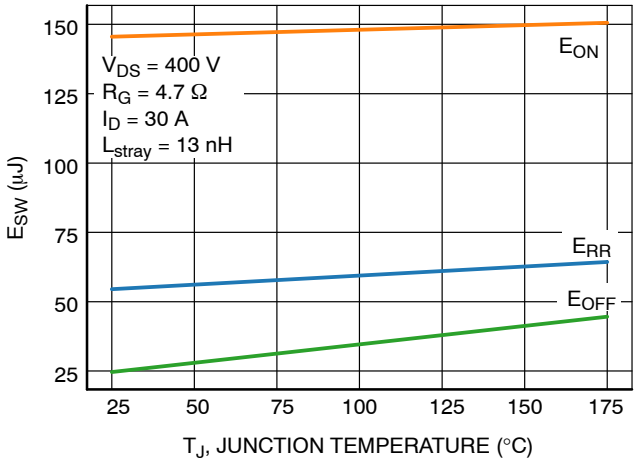


Figure 21. E_{SW} vs. T_J

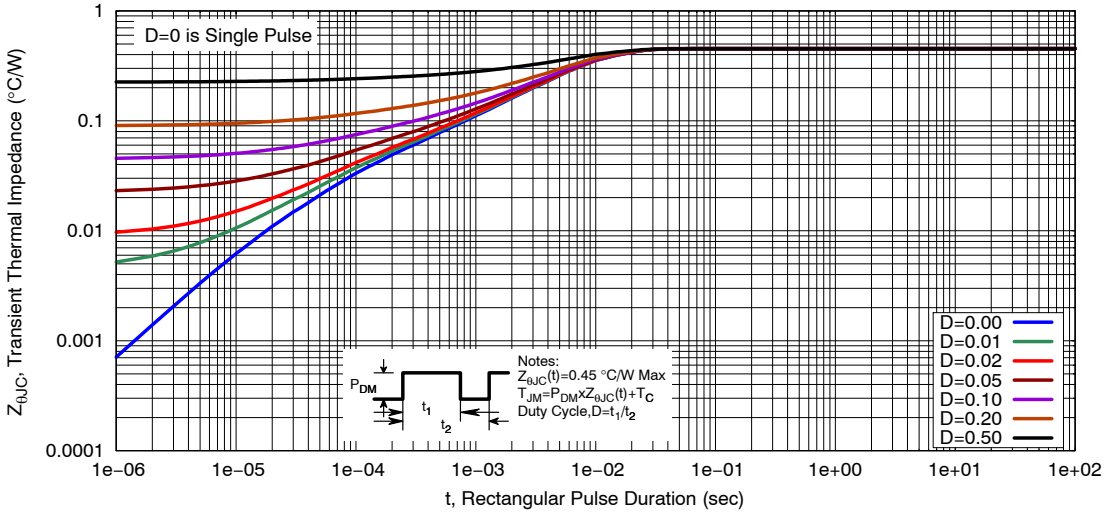
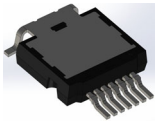


Figure 22. Thermal Response Characteristics

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial data sheet release.	09/29/2025
1	Edits to figures 5 and 8	10/10/2025

PACKAGE DIMENSIONS



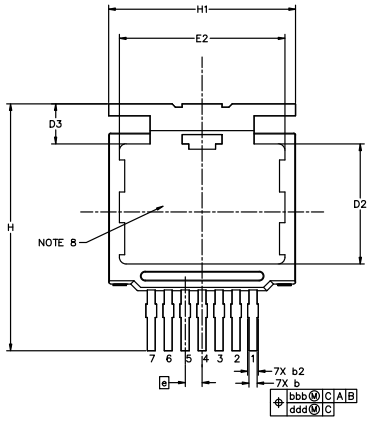
T2PAK-7 11.80x14.00x3.50, 1.27P
CASE 763AC
ISSUE A

DATE 20 JUN 2025

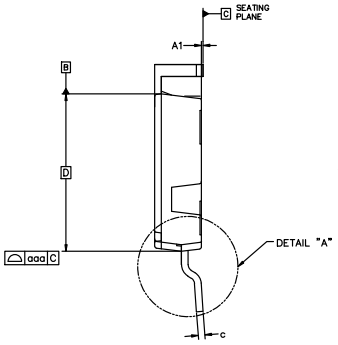
NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b, b2, b3 AND c TO BE MEASURED ON FLAT SECTION OF THE LEAD BETWEEN 0.13 AND 0.25mm FROM LEAD TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO THE TERMINALS AND EXPOSED PAD.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
8. ALLOWABLE ENCROACHED FLASH ON HEAT SINK AREA MAXIMUM OF 0.05mm.
9. EJECTOR PINS ø12.5mm REF.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	3.53	3.63	3.73
A1	0.07	0.13	0.18
A2	3.40	3.50	3.60
b	0.50	0.60	0.70
b2	0.50	0.75	1.00
b3	0.80	0.90	1.00
c	0.40	0.50	0.60
c2	0.40	0.50	0.60
D	11.80 BSC		
D2	8.90	9.00	9.10
D3	3.00	3.10	3.20
D4	3.80	3.90	4.00
D5	2.10	2.20	2.30
E	14.00 BSC		
E2	12.30	12.40	12.50
e	1.27 BSC		

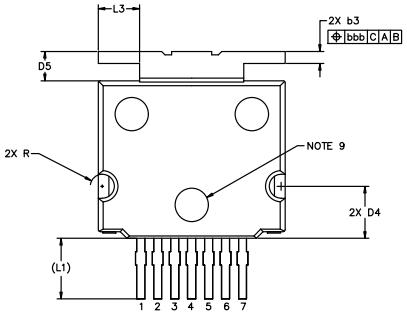
MILLIMETERS			
DIM	MIN	NOM	MAX
H	18.00	18.50	19.00
H1	13.80	14.00	14.20
L	2.42	2.52	2.62
L1	4.53 REF		
L2	0.25 BSC		
L3	3.00	3.10	3.20
R	0.80	---	1.00
Θ	0°	---	8°
Θ1	0°	---	8°
TOLERANCE FORM AND POSITION			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		



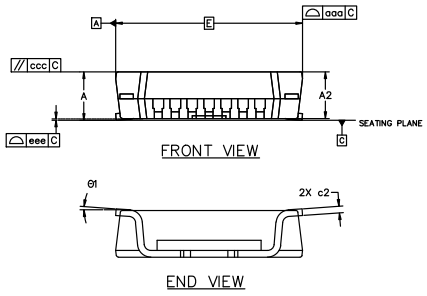
TOP VIEW



SIDE VIEW

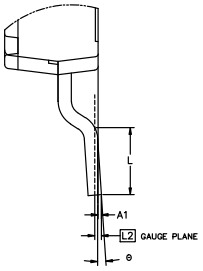


BOTTOM VIEW

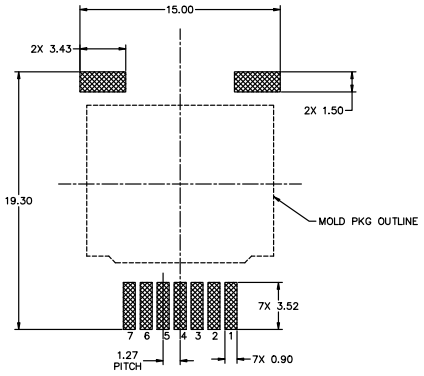


FRONT VIEW

END VIEW



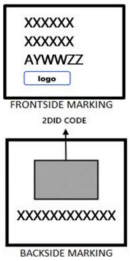
DETAIL "A"
SCALE 2:1



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales