

NTR3162P

Power MOSFET

-20 V, -3.6 A, Single P-Channel, SOT-23

Features

- Low $R_{DS(on)}$ at Low Gate Voltage
- -0.3 V Low Threshold Voltage
- Fast Switching Speed
- This is a Pb-Free Device

Applications

- Battery Management
- Load Switch in PWM
- Battery Protection

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	-20	V
Gate-to-Source Voltage			V_{GS}	± 8	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	-2.2	A
		$T_A = 85^{\circ}\text{C}$		-1.6	
	$t \leq 5 \text{ s}$	$T_A = 25^{\circ}\text{C}$		-3.6	
Power Dissipation (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	P_D	0.48	W
	$t \leq 5 \text{ s}$			1.25	
Pulsed Drain Current	$t_p = 10 \mu\text{s}$		I_{DM}	-10.7	A
Operating Junction and Storage Temperature			T_J, T_{stg}	-55 to 150	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	-0.6	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	260	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - $t < 10 \text{ s}$ (Note 1)	$R_{\theta JA}$	100	

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

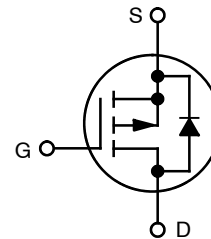


ON Semiconductor®

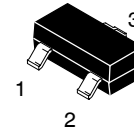
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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
-20 V	70 m Ω @ -4.5 V	-2.2 A
	95 m Ω @ -2.5 V	-1.9 A
	120 m Ω @ -1.8 V	-1.7 A

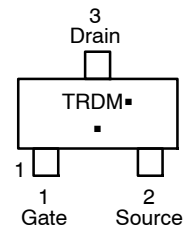
P-CHANNEL MOSFET



MARKING DIAGRAM/ PIN ASSIGNMENT



SOT-23
CASE 318
STYLE 21



TRD = Specific Device Code
M = Date Code
■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTR3162PT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
NTR3162PT3G	SOT-23 (Pb-Free)	10000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTR3162P

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} / T _J	I _D = -250 μA, Reference to 25°C		14.5		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -16 V, T _J = 25°C V _{GS} = 0 V, V _{DS} = -16 V, T _J = 85°C			-1.0 -5.0	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250 μA	-0.3	-0.6	-1.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} / T _J			2.5		mV/°C
Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -2.2 A		48	70	mΩ
		V _{GS} = -2.5 V, I _D = -1.9 A		57	95	
		V _{GS} = -1.8 V, I _D = -1.7 A		72	120	
		V _{GS} = -1.5 V, I _D = -1.0 A		88		
Forward Transconductance	g _{FS}	V _{DS} = -5.0 V, I _D = -2.2 A		9.0		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = -10 V		940		pF
Output Capacitance	C _{oss}			140		
Reverse Transfer Capacitance	C _{rss}			100		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -3.6 A		10.3		nC
Threshold Gate Charge	Q _{G(TH)}			0.5		
Gate-to-Source Charge	Q _{GS}			1.4		
Gate-to-Drain Charge	Q _{GD}			2.7		
Gate Resistance	R _G			6.0		Ω

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(on)}	V _{GS} = -4.5 V, V _{DD} = -10 V, I _D = -3.6 A, R _G = 6 Ω		8.0		ns
Rise Time	t _r			15		
Turn-Off Delay Time	t _{d(off)}			31		
Fall Time	t _f			50		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = -1.0 A, T _J = 25°C		0.7	1.2	V
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, I _D = -1.0 A, dI _{SD} /dt = 100 A/μs		25		ns
Charge Time	t _a			8.0		
Discharge Time	t _b			17		
Reverse Recovery Charge	Q _{RR}			11		nC

2. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

P-CHANNEL TYPICAL CHARACTERISTICS

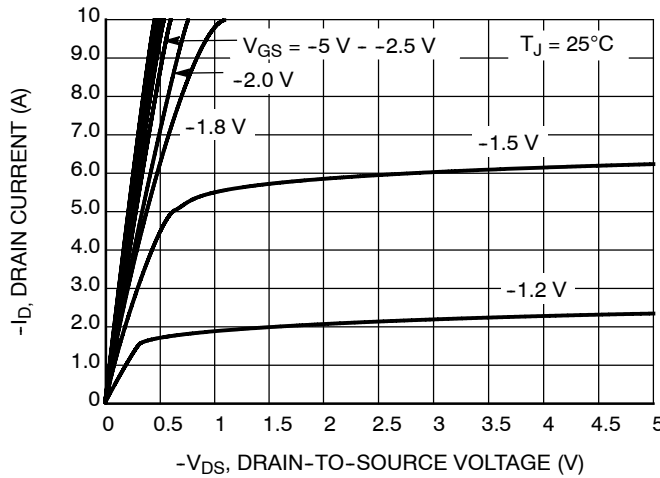


Figure 1. On-Region Characteristics

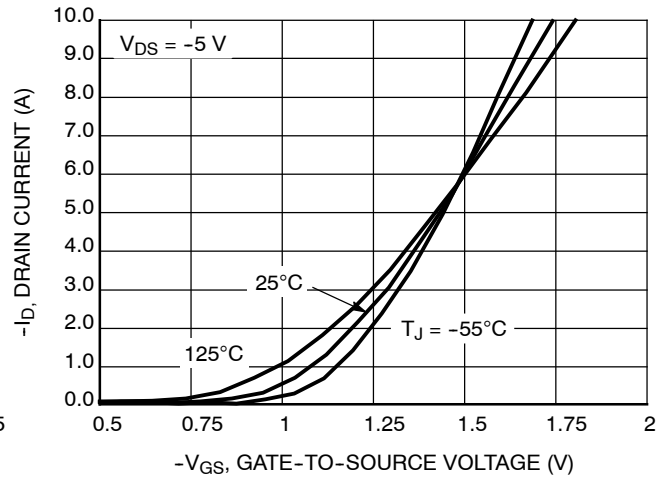


Figure 2. Transfer Characteristics

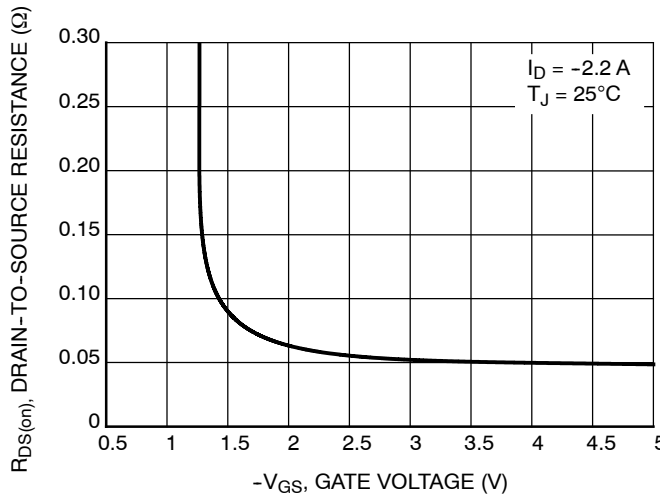


Figure 3. On-Resistance vs. Gate-to-Source Voltage

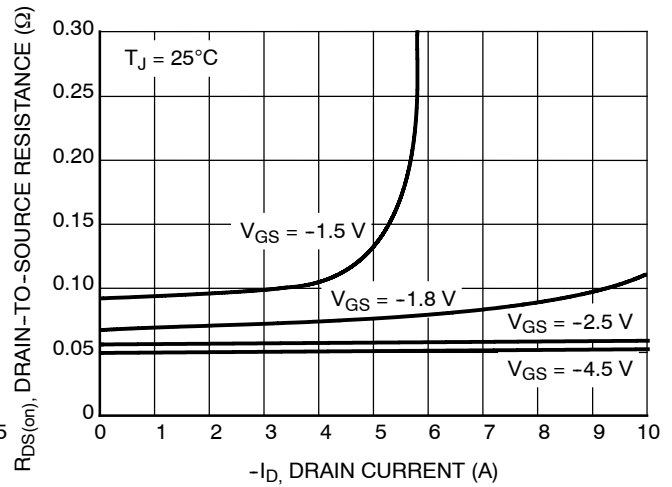


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

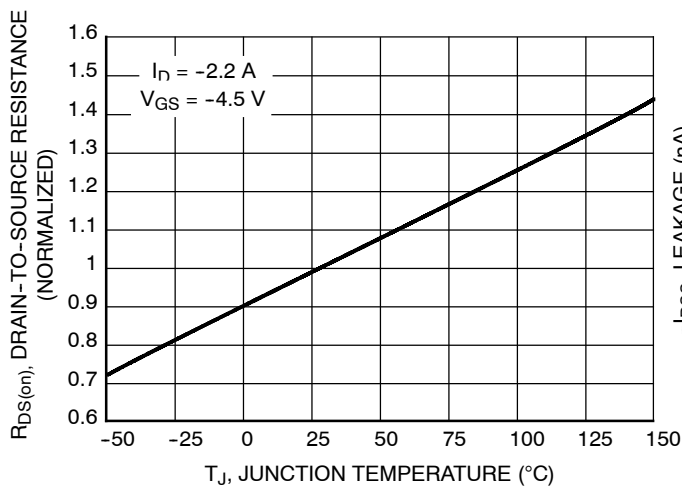


Figure 5. On-Resistance Variation with Temperature

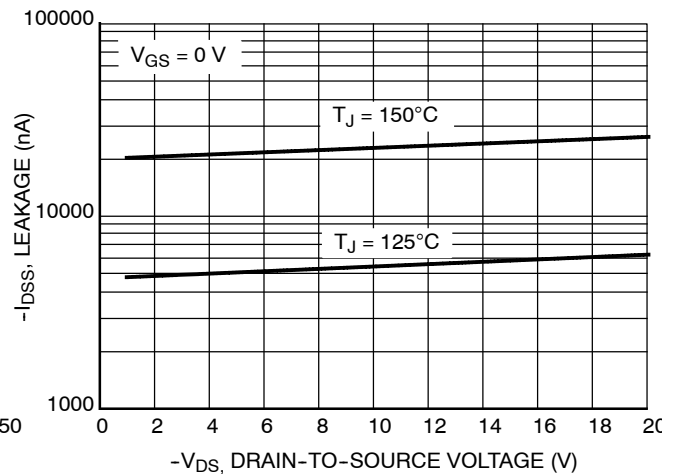
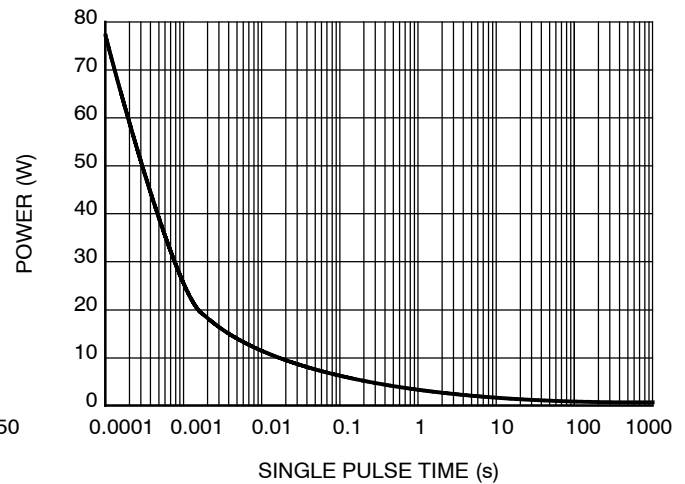
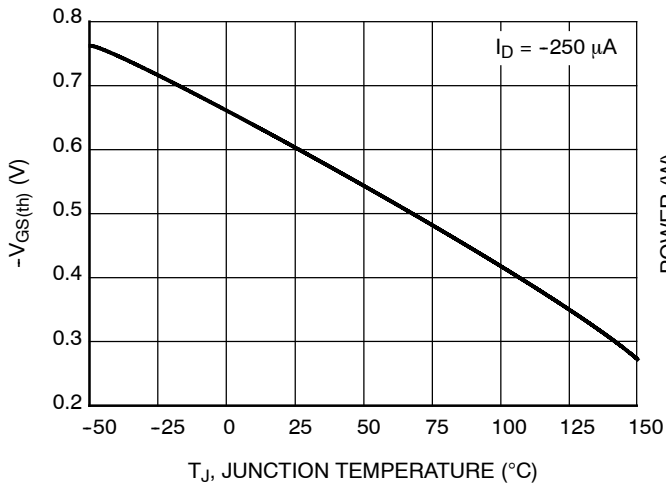
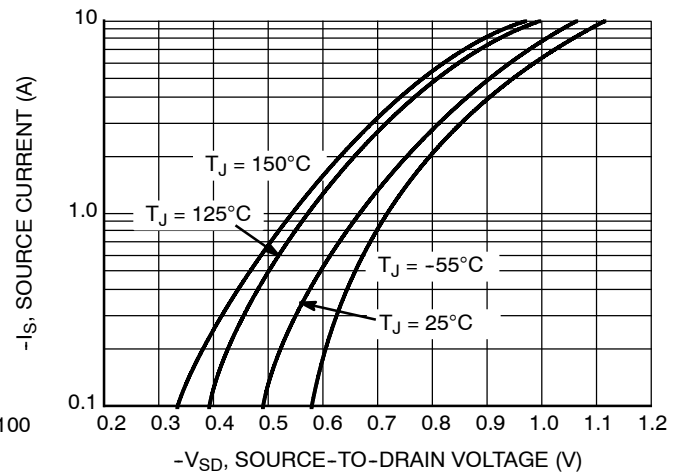
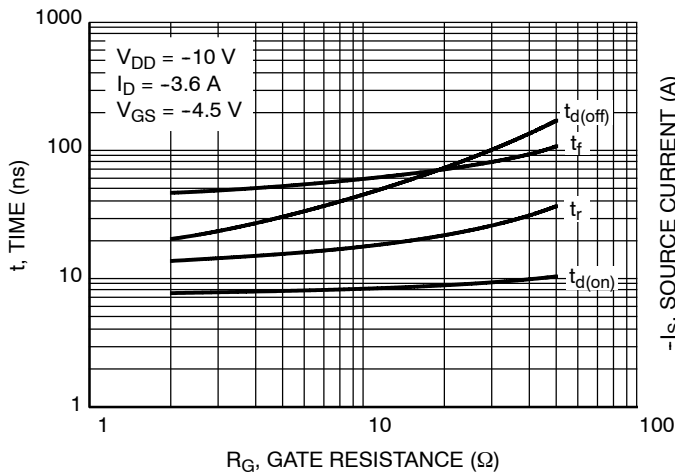
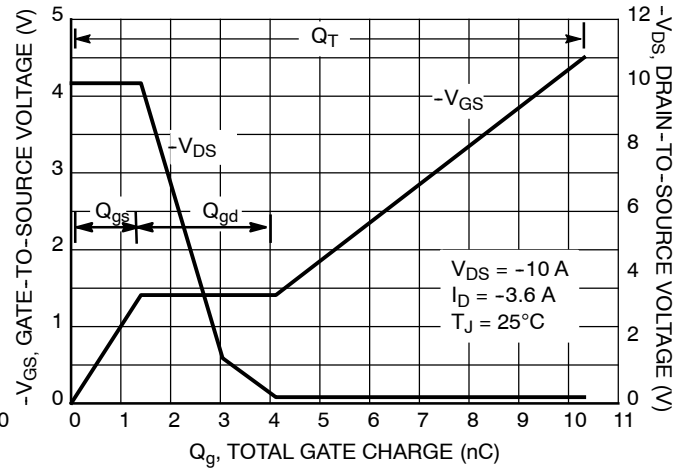
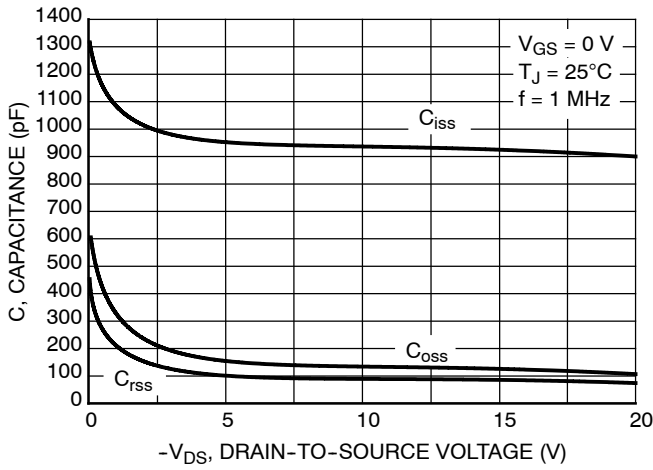


Figure 6. Drain-to-Source Leakage Current vs. Voltage



NTR3162P

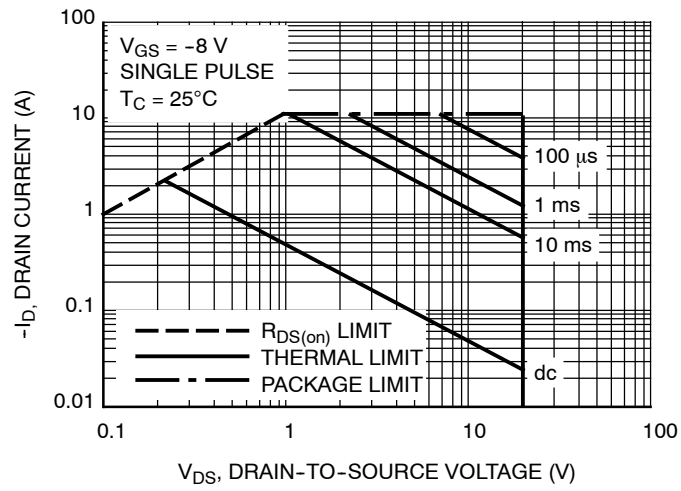


Figure 13. Maximum Rated Forward Biased Safe Operating Area

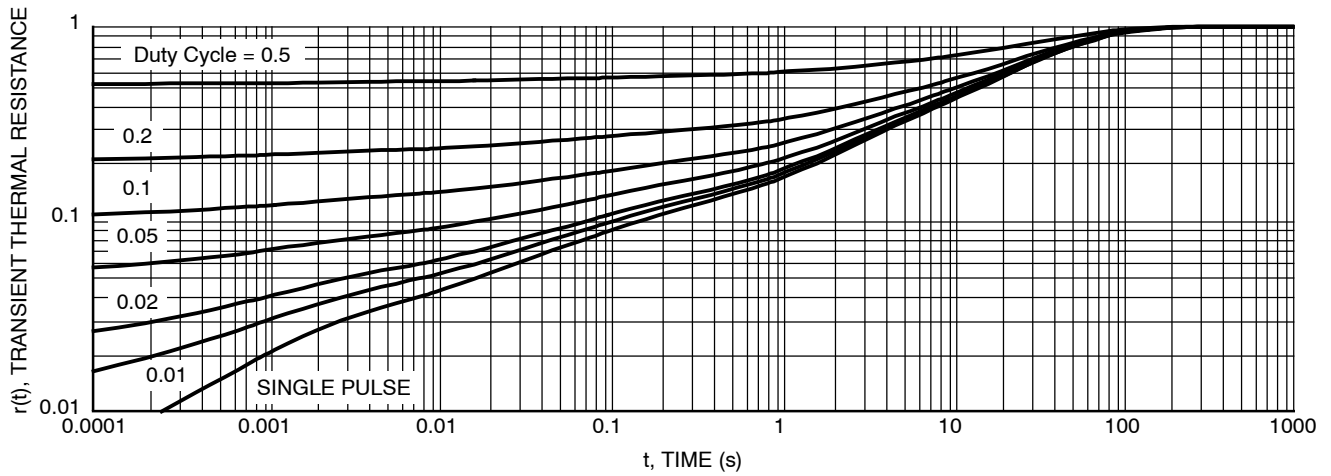


Figure 14. Thermal Response



SCALE 4:1

SOT-23 (TO-236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
HE	2.10	2.40	2.64
T	0°	---	10°

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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