# NTR2101P

# MOSFET – Single P-Channel, Small Signal, SOT-23

## -8.0 V, -3.7 A

### Features

- Leading Trench Technology for Low $R_{DS(on)}$
- −1.8 V Rated for Low Voltage Gate Drive
- SOT−23 Surface Mount for Small Footprint (3 x 3 mm)
- This is a Pb−Free Device

### Applications

- High Side Load Switch
- DC−DC Conversion
- Cell Phone, Notebook, PDAs, etc.

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise stated)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | −8.0 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±8.0 | V |
| Continuous Drain Current (Note 1) | t ≤ 5 s | $T_A$ = 25°C | $I_D$ | −3.7 | A |
| | | $T_A$ = 70°C | | −3.0 | |
| Power Dissipation (Note 1) | t ≤ 5 s | | $P_D$ | 0.96 | W |
| Pulsed Drain Current | $t_p$ = 10 μs | | $I_{DM}$ | −11 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to 150 | °C |
| Source Current (Body Diode) | | | $I_S$ | −1.2 | A |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

**THERMAL RESISTANCE RATINGS**

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Junction−to−Ambient − Steady State | $R_{\theta JA}$ | 160 | °C/W |
| Junction−to−Ambient − t ≤ 5 s | $R_{\theta JA}$ | 130 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

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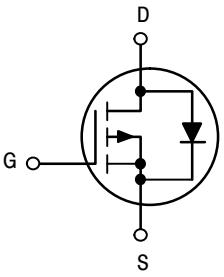
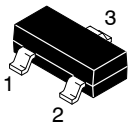
| $V_{(BR)DSS}$ | $R_{DS(on)}$ Typ | $I_D$ Max |
|---|---|---|
| −8.0 V | 39 mΩ @ −4.5 V | −3.7 A |
| | 52 mΩ @ −2.5 V | |
| | 79 mΩ @ −1.8 V | |

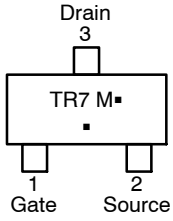
**P−Channel**




**SOT−23**
**CASE 318**
**STYLE 21**

**MARKING DIAGRAM & PIN ASSIGNMENT**




TR7 = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTR2101PT1G | SOT−23 (Pb−Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise stated)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = −250 μA | | −8.0 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | | 10 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = −6.4 V | $T_J$ = 25°C | | | −1.0 | μA |
| | | | $T_J$ = 125°C | | | −100 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±8.0 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = −250 μA | | −0.40 | | −1.0 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | | 2.7 | | mV/°C |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = −4.5 V, $I_D$ = −3.5 A | | | 39 | 52 | mΩ |
| | | $V_{GS}$ = −2.5 V, $I_D$ = −3.0 A | | | 52 | 72 | |
| | | $V_{GS}$ = −1.8 V, $I_D$ = −2.0 A | | | 79 | 120 | |
| Forward Transconductance | $g_{FS}$ | $V_{GS}$ = −5.0 V, $I_D$ = −3.5 A | | | 9.0 | | S |
| **CHARGES AND CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1.0 MHz, $V_{DS}$ = −4.0 V | | | 1173 | | pF |
| Output Capacitance | $C_{OSS}$ | | | | 289 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | 218 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = −4.5 V, $V_{DS}$ = −4.0 V, $I_D$ = −3.5 A | | | 12 | 15 | nC |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 3.8 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 2.5 | | |
| **SWITCHING CHARACTERISTICS** (Note 3) | | | | | | | |
| Turn−On Delay Time | $t_{d(on)}$ | $V_{GS}$ = −4.5 V, $V_{DD}$ = −4.0 V, $I_D$ = −1.2 A, $R_G$ = 6.0 Ω | | | 7.4 | 15 | ns |
| Rise Time | $t_r$ | | | | 15.75 | 25 | |
| Turn−Off Delay Time | $t_{d(off)}$ | | | | 38 | 58 | |
| Fall Time | $t_f$ | | | | 31 | 51 | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = −1.2 A | $T_J$ = 25°C | | −0.73 | −1.2 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

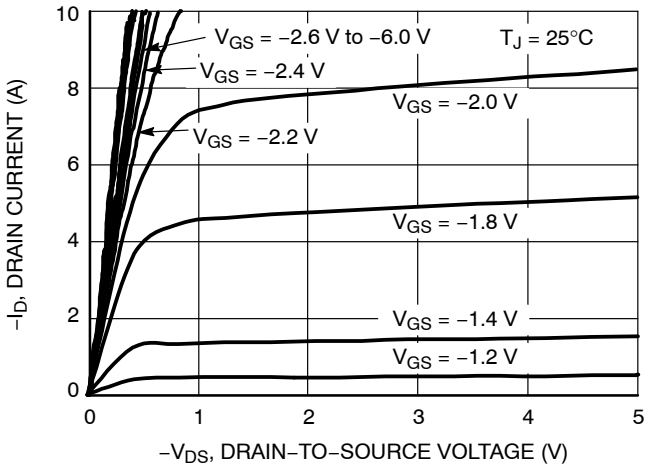



**Figure 1. On−Region Characteristics**

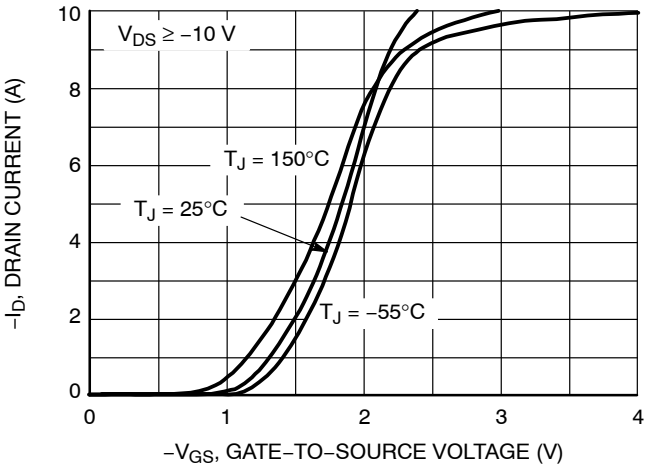



**Figure 2. Transfer Characteristics**

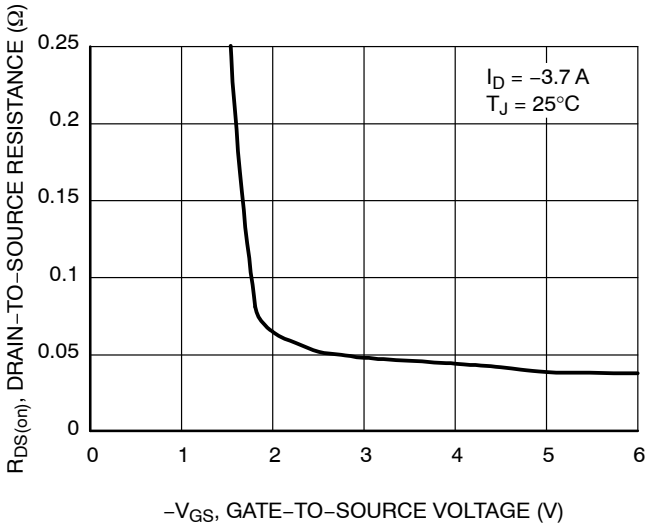



**Figure 3. On−Resistance versus Gate−to−Source Voltage**

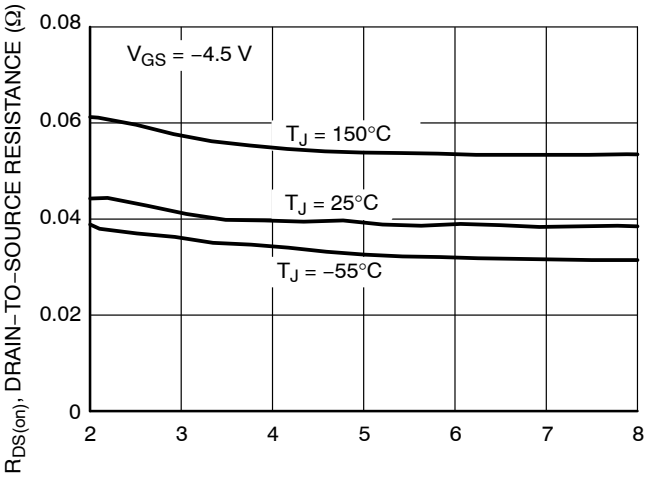



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

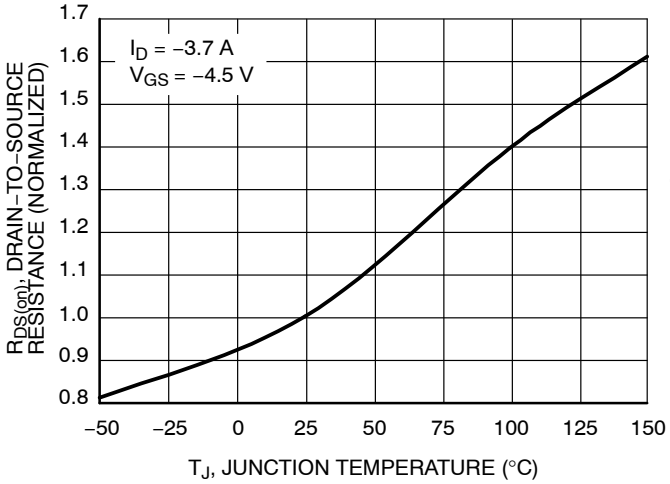



**Figure 5. On−Resistance Variation with Temperature**

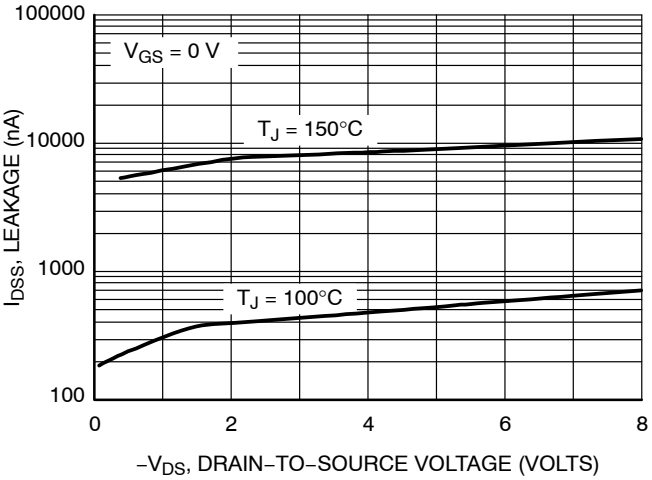



**Figure 6. Drain−to−Source Leakage Current versus Voltage**

## TYPICAL CHARACTERISTICS

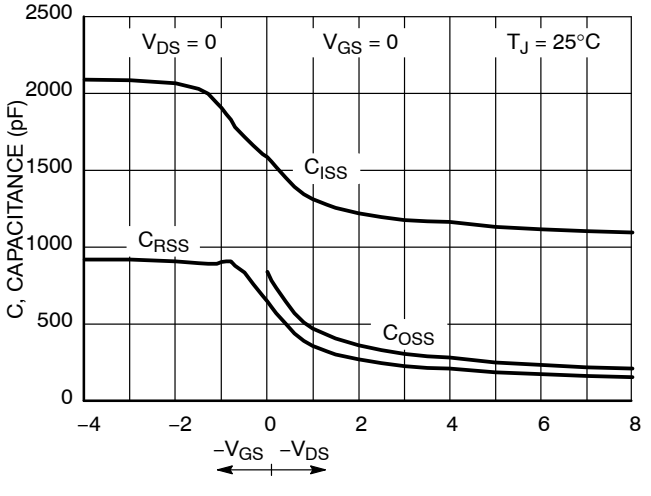



**Figure 7. Capacitance Variation**

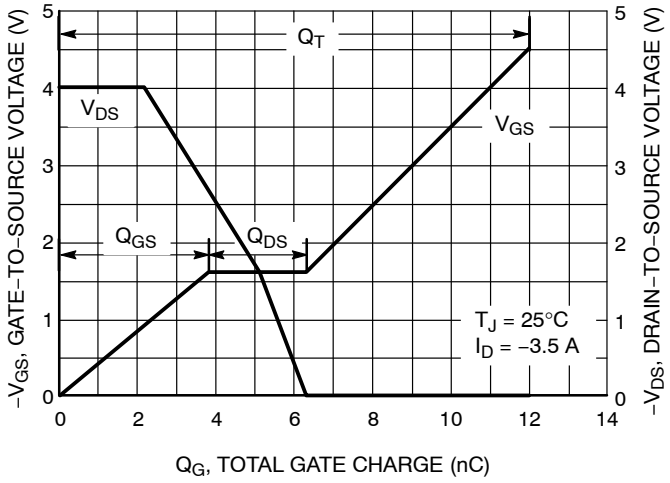



**Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge**

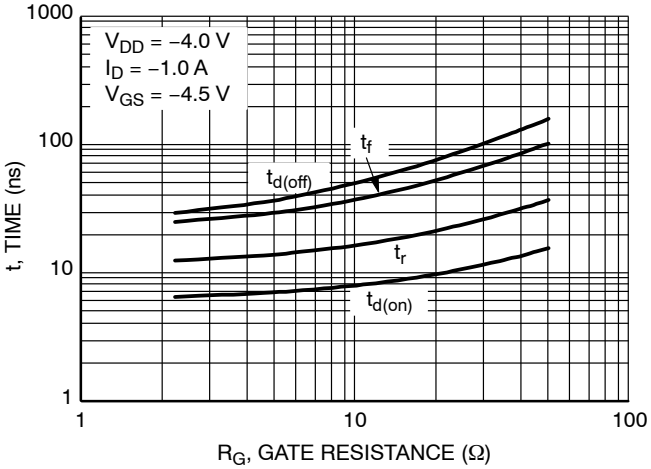



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

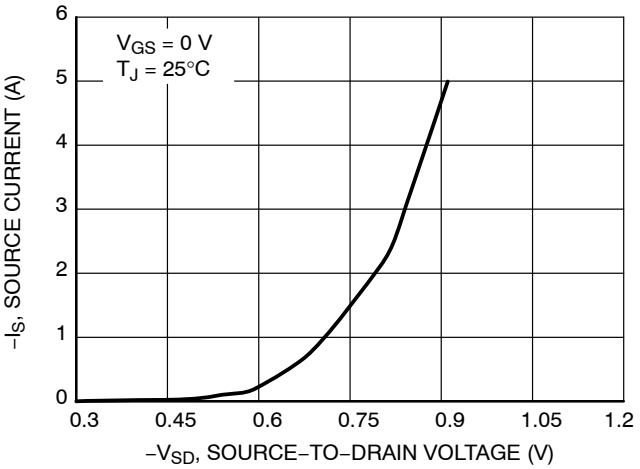



**Figure 10. Diode Forward Voltage versus Current**

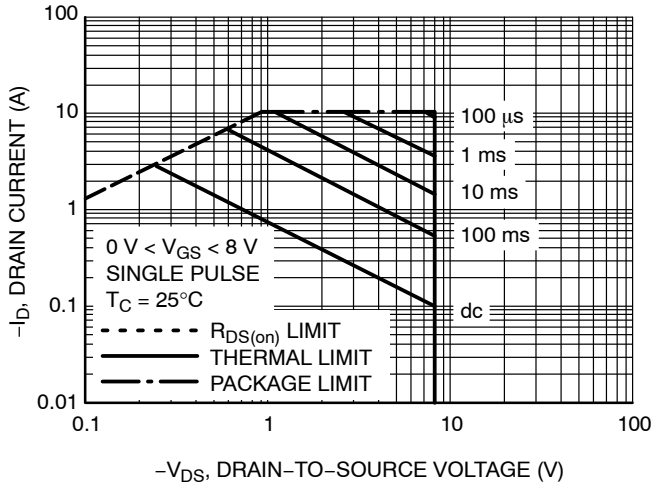



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL CHARACTERISTICS

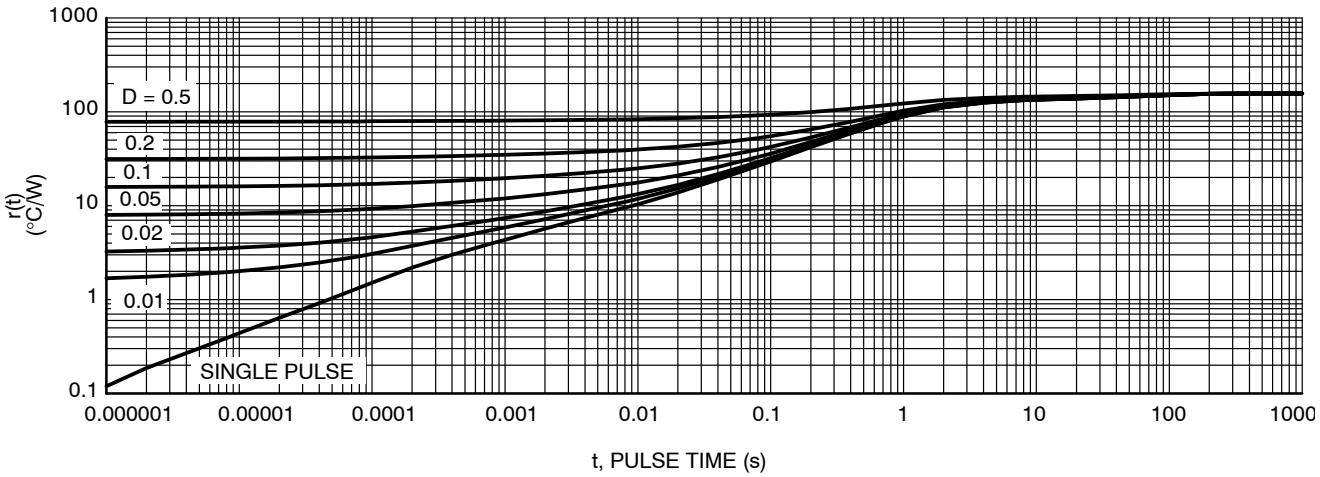
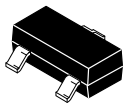



**Figure 12. Thermal Response**

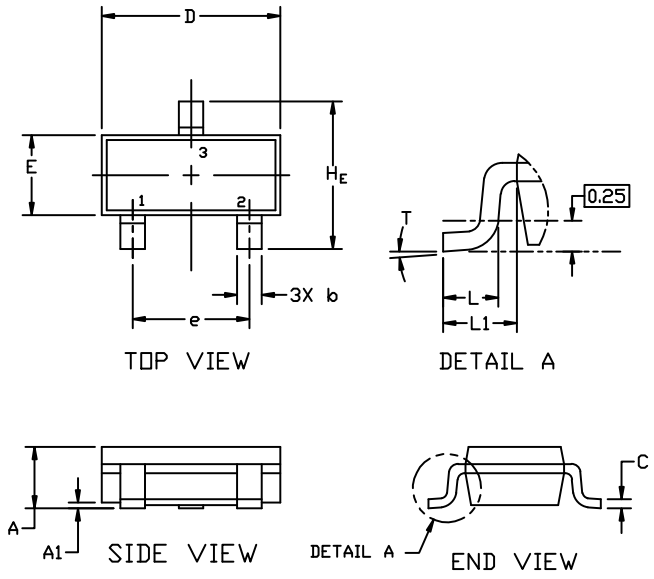
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



SCALE 4:1

**SOT−23 (TO−236)**
CASE 318
ISSUE AT

DATE 01 MAR 2023

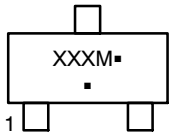



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

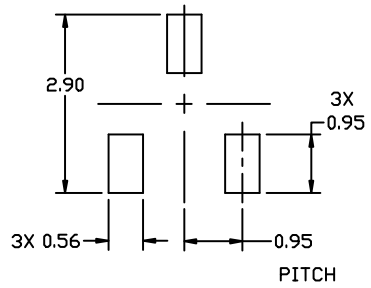
| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.89 | 1.00 | 1.11 | 0.035 | 0.039 | 0.044 |
| A1 | 0.01 | 0.06 | 0.10 | 0.000 | 0.002 | 0.004 |
| b | 0.37 | 0.44 | 0.50 | 0.015 | 0.017 | 0.020 |
| c | 0.08 | 0.14 | 0.20 | 0.003 | 0.006 | 0.008 |
| D | 2.80 | 2.90 | 3.04 | 0.110 | 0.114 | 0.120 |
| E | 1.20 | 1.30 | 1.40 | 0.047 | 0.051 | 0.055 |
| e | 1.78 | 1.90 | 2.04 | 0.070 | 0.075 | 0.080 |
| L | 0.30 | 0.43 | 0.55 | 0.012 | 0.017 | 0.022 |
| L1 | 0.35 | 0.54 | 0.69 | 0.014 | 0.021 | 0.027 |
| $H_E$ | 2.10 | 2.40 | 2.64 | 0.083 | 0.094 | 0.104 |
| T | 0° | --- | 10° | 0° | --- | 10° |

### GENERIC MARKING DIAGRAM*




XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.




RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42226B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. | |
| **DESCRIPTION:** | **SOT−23 (TO−236)** | | **PAGE 1 OF 2** |

**SOT−23 (TO−236)**
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
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