

MOSFET - N-Channel Shielded Gate, POWERTRENCH®

150 V, 5.0 mΩ, 139 A

NTP5D0N15MC

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)} = 5.0 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 97 \text{ A}$
- 50% Lower Qrr than other MOSFET Suppliers
- Lowers Switching Noise/EMI
- 100% UIL Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

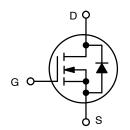
MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parar	neter		Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	150	V
Gate-to-Source Voltage			V _{GS}	±20	٧
Continuous Drain Current R _{θJC} (Note 2)	Steady State	T _C = 25 °C	Ι _D	139	Α
Power Dissipation R _{θJC} (Note 2)	Glate		P _D	214	W
Continuous Drain Current R _{0,JA} (Notes 1, 2)	Steady State	T _A = 25 °C	Ι _D	15	Α
Power Dissipation R _{0JA} (Notes 1, 2)	State		P _D	2.4	W
Pulsed Drain Current	$T_A = 25^{\circ}$	$^{\circ}$ C, $t_{p} = 100 \ \mu s$	I _{DM}	818	Α
Operating Junction and Range	Storage To	emperature	T _J , T _{stg}	-55 to +175	°C
Single Pulse Drain-to-So Energy (I _L = 26 A _{pk} , L =		anche	E _{AS}	1014	mJ
Lead Temperature for So (1/8" from case for 10 s)		urposes	T _L	260	°C

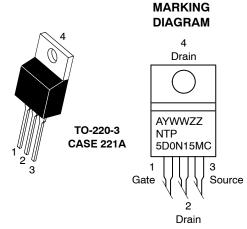
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Surface-mounted on FR4 board using a 1 in2, 2 oz. Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
150 V	$5.0~\mathrm{m}\Omega$ @ $10~\mathrm{V}$	139 A



N-CHANNEL MOSFET



NTP5D0N15MC = Specific Device Code

A = Assembly Location

Y = Year WW = Work Week ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping [†]
NTP5D0N15MC	TO-220-3 (Pb-Free)	800 / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 2)	$R_{ hetaJC}$	0.7	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{ hetaJA}$	62.5	

ELECTRICAL CHARACTERISTICS (T₁ = 25 °C unless otherwise specified)

Parameter	Symbol	Test Condi	tion	Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		150			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /	I _D = 250 μA, ref	to 25 °C		76		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 120 V	T _J = 25 °C			1.0	μΑ
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS}	= ±20 V			±100	nA
ON CHARACTERISTICS							-
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D =$	= 532 μΑ	2.5		4.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	I _D = 532 μA, ref	to 25 °C		-8.5		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D	₎ = 97 A		4.2	5	mΩ
Forward Transconductance	9FS	V _{DS} = 10 V, I _D	₎ = 97 A		146		S
CHARGES, CAPACITANCES & GATE RESIS	STANCE						-
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 75 V			6300		
Output Capacitance	C _{OSS}				1900		pF
Reverse Transfer Capacitance	C _{RSS}				13		
Gate-Resistance	R_{G}				1.1	2.2	Ω
Total Gate Charge	Q _{G(TOT)}				75		
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 10 V, V _{DS} = 75 V; I _D = 97 A			18		nC
Gate-to-Source Charge	Q_{GS}				31		
Gate-to-Drain Charge	Q_{GD}				10		
Plateau Voltage	V_{GP}				5.4		V
Output Charge	Q _{OSS}	V _{DD} = 75 V, V _O	_{GS} = 0 V		227		nC
SWITCHING CHARACTERISTICS (Note 3)							
Turn-On Delay Time	t _{d(ON)}				32		
Rise Time	t _r	$V_{GS} = 10 \text{ V}, V_{DI}$	_o = 75 V,		14		1
Turn-Off Delay Time	t _{d(OFF)}	$I_D = 97 \text{ A}, R_G = 4.7 \Omega$			45		ns
Fall Time	t _f				9.0		1
DRAIN-SOURCE DIODE CHARACTERISTIC	s						
Forward Diode Voltage	V _{SD}	$V_{GS} = 0 \text{ V},$ $I_{S} = 97 \text{ A}$	T _J = 25 °C		0.96	1.2	V
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, V _{DD}) = 75 V		92		ns
Reverse Recovery Charge	Q _{RR}	$dI_S/dt = 100 A/\mu s$			189		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

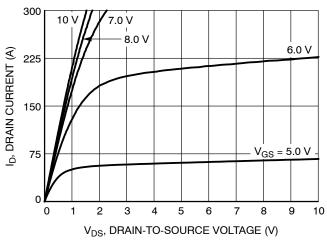


Figure 1. On-Region Characteristics

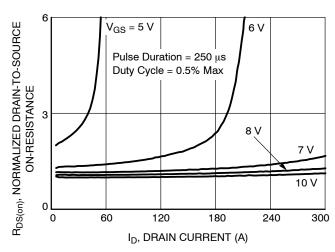


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

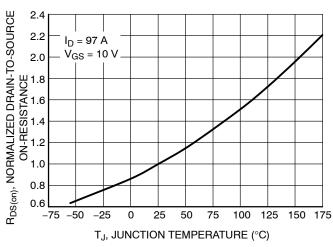


Figure 3. Normalized On-Resistance vs. Junction Temperature

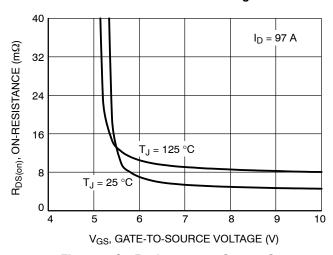


Figure 4. On-Resistance vs. Gate-to-Source Voltage

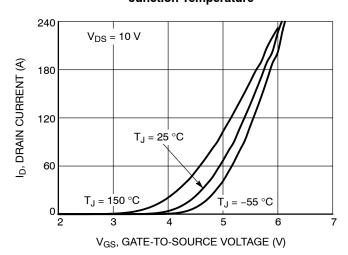


Figure 5. Transfer Characteristics

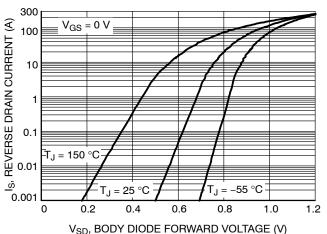


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS

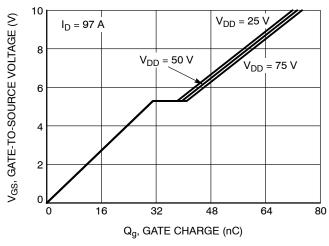
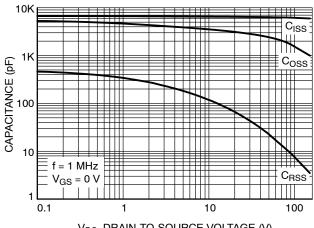


Figure 7. Gate Charge Characteristics



 $\label{eq:VDS} V_{DS}, \, \text{DRAIN-TO-SOURCE VOLTAGE (V)}$ Figure 8. Capacitance vs. Drain-to-Source

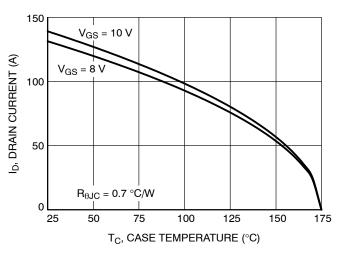
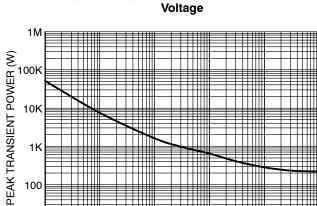


Figure 9. Drain Current vs. Case Temperature



100 10 0.00001 0.0001 0.001 0.01 0. t, PULSE WIDTH (s)

Figure 10. Peak Power

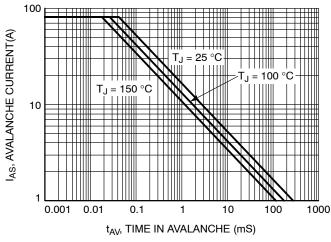


Figure 11. Unclamped Inductive Switching Capability

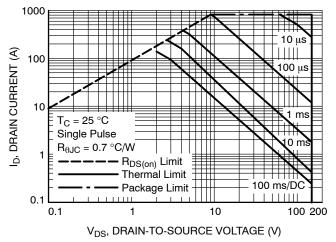


Figure 12. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS

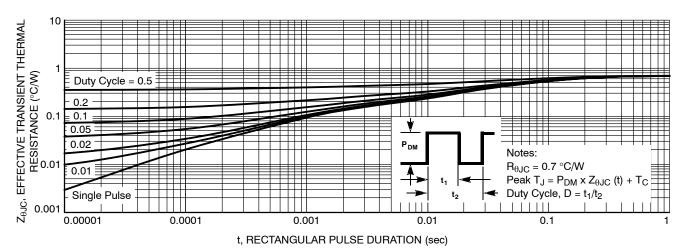


Figure 13. Transient Thermal Impedance

REVISION HISTORY

I	Revision	Description of Changes	Date
	2	Rebranded the Data Sheet to onsemi format.	6/27/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

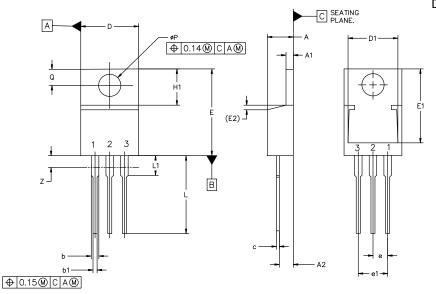
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TO-220-3 10.10x15.12x4.45, 2.54P CASE 221A **ISSUE AL**

DATE 05 FEB 2025



NOM 4.45 1.28 2.42	MAX 4.83 1.41 2.79	
1.28	1.41	
2.42		
	2.79	
4 7 4		
1.54	1.52	
0.80	0.96	
0.49	0.61	
10.10	10.53	
8.63	8.83	
15.12	15.75	
12.78	12.98	
1.27 REF		
	0.49 10.10 8.63 15.12 12.78	

MILLIMETERS						
DIM	MIN	NOM	MAX			
е	2.42	2.54	2.66			
e1	4.83	5.08	5.33			
H1	5.97	6.22	6.47			
L	12.70	13.49	14.27			
L1	2.80	3.45	4.10			
Q	2.54	2.79	3.04			
ØΡ	3.60	3.85	4.09			
Z			3.48			

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:	
PIN 1.	BASE	PIN 1.	BASE	PIN 1.	CATHODE	PIN 1.	MAIN TERMINAL 1
2.	COLLECTOR	2.	EMITTER	2.	ANODE	2.	MAIN TERMINAL 2
3.	EMITTER	3.	COLLECTOR	3.	GATE	3.	GATE
4.	COLLECTOR	4.	EMITTER	4.	ANODE	4.	MAIN TERMINAL 2
STYLE 5:		STYLE 6:		STYLE 7:		STYLE 8:	
PIN 1.	GATE	PIN 1.	ANODE	PIN 1.	CATHODE	PIN 1.	CATHODE
2.	DRAIN	2.	CATHODE	2.	ANODE	2.	ANODE
3.	SOURCE	3.	ANODE	3.	CATHODE	3.	EXTERNAL TRIP/DELAY
4.	DRAIN	4.	CATHODE	4.	ANODE	4.	ANODE
STYLE 9:		STYLE 10:		STYLE 11:	:	STYLE 12:	:
PIN 1.	GATE	PIN 1.	GATE	PIN 1.	DRAIN	PIN 1.	MAIN TERMINAL 1
2.	COLLECTOR	2.	SOURCE	2.	SOURCE	2.	MAIN TERMINAL 2
3.	EMITTER	3.	DRAIN	3.	GATE	3.	GATE
4.	COLLECTOR	4.	SOURCE	4.	SOURCE	4.	NOT CONNECTED

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DESCRIPTION:	TO-220-3 10.10x15.12x4.45, 2.54P		PAGE 1 OF 1	

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