# NTMSD3P102R2

# FETKY™

## P−Channel Enhancement−Mode Power MOSFET and Schottky Diode Dual SO−8 Package

### Features

- High Efficiency Components in a Single SO−8 Package
- High Density Power MOSFET with Low $R_{DS(on)}$, Schottky Diode with Low $V_F$
- Independent Pin−Outs for MOSFET and Schottky Die Allowing for Flexibility in Application Use
- Less Component Placement for Board Space Savings
- SO−8 Surface Mount Package, Mounting Information for SO−8 Package Provided
- Pb−Free Packages are Available

### Applications

- DC−DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery−Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular and Cordless Telephones

**MOSFET MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted).

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain−to−Source Voltage | $V_{DSS}$ | −20 | V |
| Gate−to−Source Voltage − Continuous | $V_{GS}$ | ±20 | V |
| Thermal Resistance − Junction−to−Ambient (Note 1)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 4) | $R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | 171<br>0.73<br>−2.34<br>−1.87<br>−8.0 | °C/W<br>W<br>A<br>A<br>A |
| Thermal Resistance − Junction−to−Ambient (Note 2)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 4) | $R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | 100<br>1.25<br>−3.05<br>−2.44<br>−12 | °C/W<br>W<br>A<br>A<br>A |
| Thermal Resistance − Junction−to−Ambient (Note 3)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 4) | $R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | 62.5<br>2.0<br>−3.86<br>−3.10<br>−15 | °C/W<br>W<br>A<br>A<br>A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |
| Single Pulse Drain−to−Source Avalanche Energy − Starting $T_J$ = 25°C ($V_{DD}$ = −20 Vdc, $V_{GS}$ = −4.5 Vdc, Peak $I_L$ = −7.5 Apk, L = 5 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 140 | mJ |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

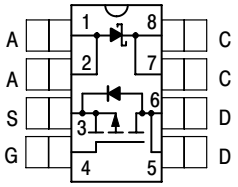
1. Minimum FR−4 or G−10 PCB, Steady State.
2. Mounted onto a 2″ square FR−4 Board (1 in sq, 2 oz Cu 0.06″ thick single−sided), Steady State.
3. Mounted onto a 2″ square FR−4 Board (1 in sq, 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

**ON Semiconductor®**

**http://onsemi.com**

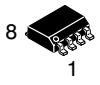
**MOSFET**
**−3.05 AMPERES**
**−20 VOLTS**
**0.085 Ω @ $V_{GS}$ = −10 V**

**SCHOTTKY DIODE**
**1.0 AMPERE**
**20 VOLTS**
**470 mV @ $I_F$ = 1.0 A**

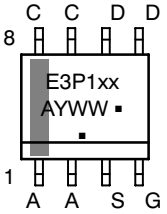


(TOP VIEW)

**MARKING DIAGRAM & PIN ASSIGNMENT**




**SO−8**
**CASE 751**
**STYLE 18**




| | |
|---|---|
| E3P1 | = Device Code |
| xx | = 02 or S |
| A | = Assembly Location |
| Y | = Year |
| WW | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTMSD3P102R2 | SO−8 | 2500/Tape & Reel |
| NTMSD3P102R2G | SO−8 (Pb−Free) | 2500/Tape & Reel |
| NTMSD3P102R2SG | SO−8 (Pb−Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**SCHOTTKY MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Peak Repetitive Reverse Voltage<br>DC Blocking Voltage | $V_{RRM}$<br>$V_R$ | 20 | V |
| Thermal Resistance – Junction–to–Ambient (Note 5) | $R_{\theta JA}$ | 204 | °C/W |
| Thermal Resistance – Junction–to–Ambient (Note 6) | $R_{\theta JA}$ | 122 | °C/W |
| Thermal Resistance – Junction–to–Ambient (Note 7) | $R_{\theta JA}$ | 83 | °C/W |
| Average Forward Current (Note 7)<br>(Rated $V_R$, $T_A$ = 100°C) | $I_O$ | 1.0 | A |
| Peak Repetitive Forward Current (Note 7)<br>(Rated $V_R$, Square Wave, 20 kHz, $T_A$ = 105°C) | $I_{FRM}$ | 2.0 | A |
| Non–Repetitive Peak Surge Current (Note 7)<br>(Surge Applied at Rated Load Conditions, Half–Wave, Single Phase, 60 Hz) | $I_{FSM}$ | 20 | A |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

5. Minimum FR–4 or G–10 PCB, Steady State.
6. Mounted onto a 2″ square FR–4 Board (1 in sq, 2 oz Cu 0.06″ thick single–sided), Steady State.
7. Mounted onto a 2″ square FR–4 Board (1 in sq, 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.

**SCHOTTKY ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 8)

| Characteristic | Symbol | Value | | Unit |
|---|---|---|---|---|
| Maximum Instantaneous Forward Voltage<br>$I_F$ = 1.0 Adc<br>$I_F$ = 2.0 Adc | $V_F$ | **$T_J$ = 25°C** | **$T_J$ = 125°C** | Volts |
| Maximum Instantaneous Forward Voltage<br>$I_F$ = 1.0 Adc<br>$I_F$ = 2.0 Adc | $V_F$ | 0.47<br>0.58 | 0.39<br>0.53 | Volts |
| Maximum Instantaneous Reverse Current<br>$V_R$ = 20 Vdc | $I_R$ | **$T_J$ = 25°C**<br>0.05 | **$T_J$ = 125°C**<br>10 | mA |
| Maximum Voltage Rate of Change $V_R$ = 20 Vdc | dV/dt | 10,000 | | V/μs |

8. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.

**MOSFET ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 9)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain−to−Source Breakdown Voltage<br>($V_{GS}$ = 0 Vdc, $I_D$ = −250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>−20<br>− | <br>−<br>−30 | <br>−<br>− | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = −20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C)<br>($V_{DS}$ = −20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>−<br>− | <br>−<br>− | <br>−1.0<br>−25 | μAdc |
| Gate−Body Leakage Current<br>($V_{GS}$ = −20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | <br>− | <br>− | <br>−100 | nAdc |
| Gate−Body Leakage Current<br>($V_{GS}$ = +20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | <br>− | <br>− | <br>100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = −250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>−1.0<br>− | <br>−1.7<br>3.6 | <br>−2.5<br>− | Vdc |
| Static Drain−to−Source On−State Resistance<br>($V_{GS}$ = −10 Vdc, $I_D$ = −3.05 Adc)<br>($V_{GS}$ = −4.5 Vdc, $I_D$ = −1.5 Adc) | | $R_{DS(on)}$ | <br>−<br>− | <br>0.063<br>0.090 | <br>0.085<br>0.125 | Ω |
| Forward Transconductance<br>($V_{DS}$ = −15 Vdc, $I_D$ = −3.05 Adc) | | $g_{FS}$ | <br>− | <br>5.0 | <br>− | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = −16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | − | 518 | 750 | pF |
| Output Capacitance | | $C_{oss}$ | − | 190 | 350 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | − | 70 | 135 | |
| **SWITCHING CHARACTERISTICS** (Notes 10 & 11) | | | | | | |
| Turn−On Delay Time | ($V_{DD}$ = −20 Vdc, $I_D$ = −3.05 Adc, $V_{GS}$ = −10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | − | 12 | 22 | ns |
| Rise Time | | $t_r$ | − | 16 | 30 | |
| Turn−Off Delay Time | | $t_{d(off)}$ | − | 45 | 80 | |
| Fall Time | | $t_f$ | − | 45 | 80 | |
| Turn−On Delay Time | ($V_{DD}$ = −20 Vdc, $I_D$ = −1.5 Adc, $V_{GS}$ = −4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | − | 16 | − | ns |
| Rise Time | | $t_r$ | − | 42 | − | |
| Turn−Off Delay Time | | $t_{d(off)}$ | − | 32 | − | |
| Fall Time | | $t_f$ | − | 35 | − | |
| Total Gate Charge | ($V_{DS}$ = −20 Vdc, $V_{GS}$ = −10 Vdc, $I_D$ = −3.05 Adc) | $Q_{tot}$ | − | 16 | 25 | nC |
| Gate−Source Charge | | $Q_{gs}$ | − | 2.0 | − | |
| Gate−Drain Charge | | $Q_{gd}$ | − | 4.5 | − | |
| **BODY−DRAIN DIODE RATINGS** (Note 10) | | | | | | |
| Diode Forward On−Voltage | ($I_S$ = −3.05 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = −3.05 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>− | <br>−0.96<br>−0.78 | <br>−1.25<br>− | Vdc |
| Reverse Recovery Time | ($I_S$ = −3.05 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | − | 34 | − | ns |
| | | $t_a$ | − | 18 | − | |
| | | $t_b$ | − | 16 | − | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | − | 0.03 | − | μC |

9. Handling precautions to protect against electrostatic discharge are mandatory.
10. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
11. Switching characteristics are independent of operating junction temperature.

## TYPICAL MOSFET ELECTRICAL CHARACTERISTICS

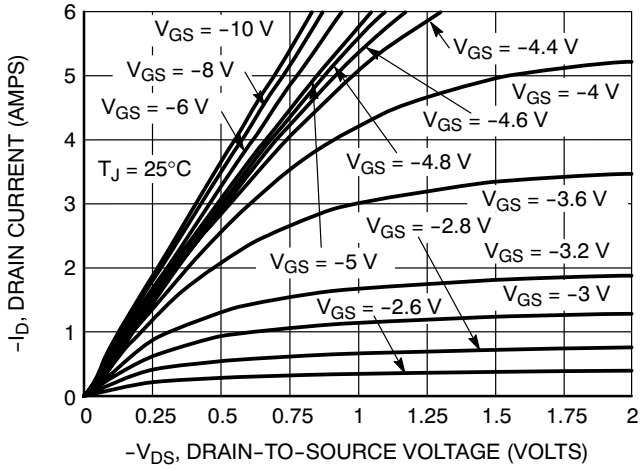



**Figure 1. On−Region Characteristics**

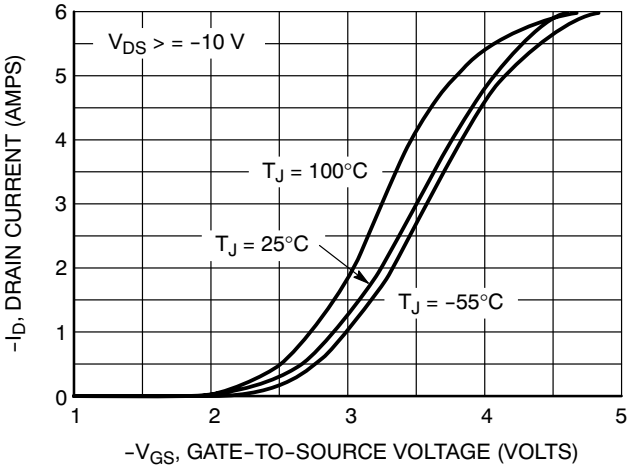



**Figure 2. Transfer Characteristics**

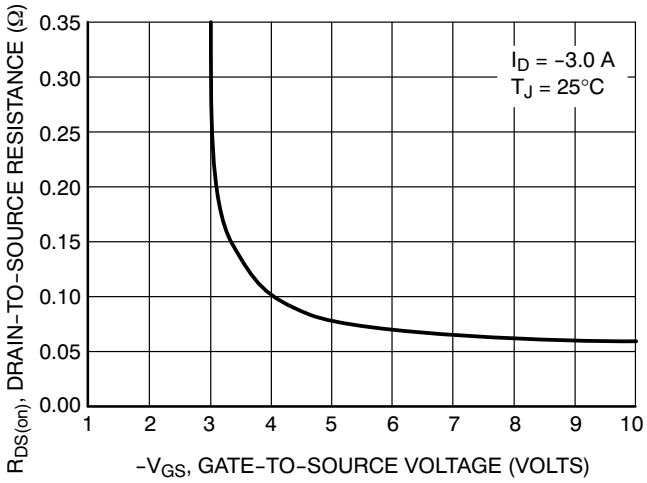



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

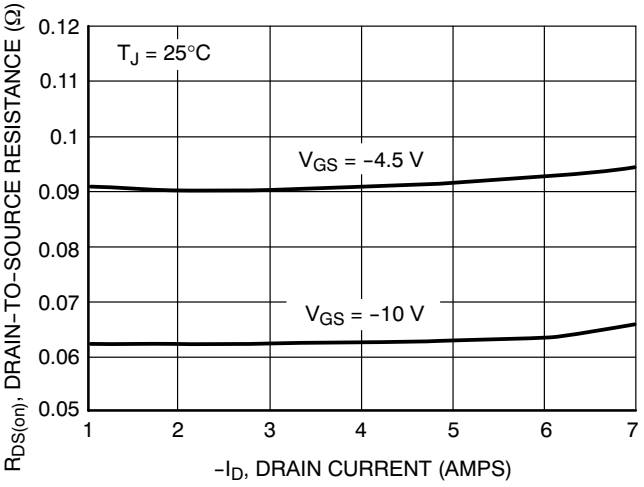



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

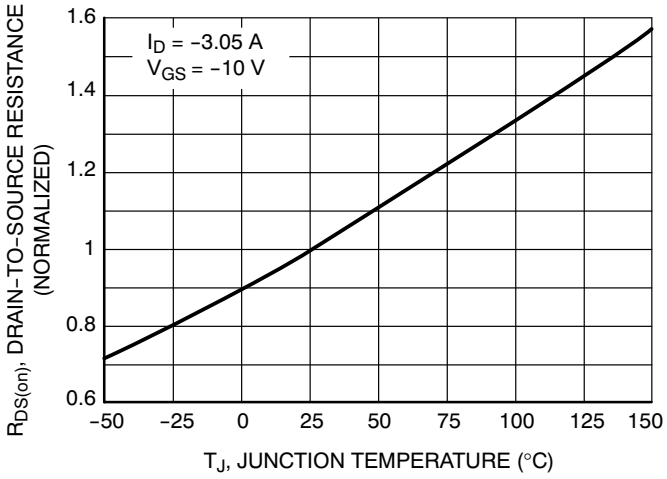



**Figure 5. On Resistance Variation with Temperature**

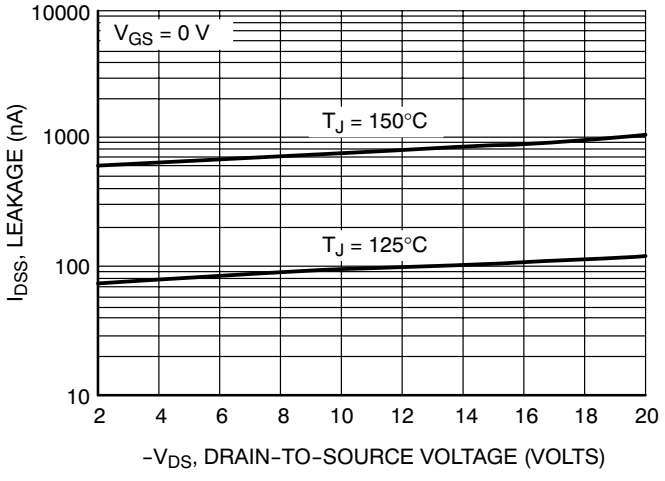



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

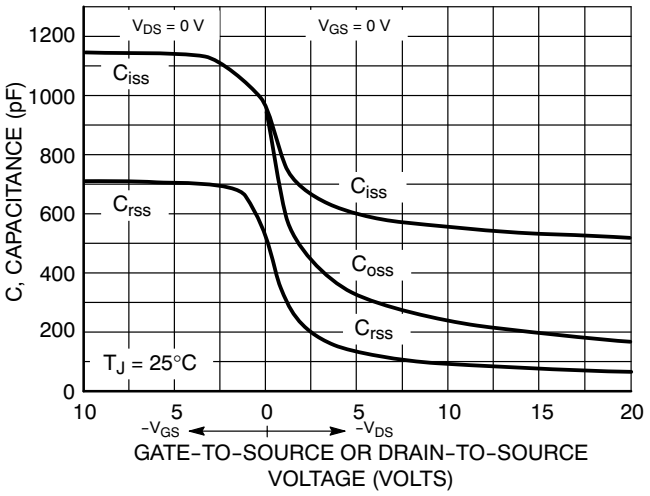



**Figure 7. Capacitance Variation**

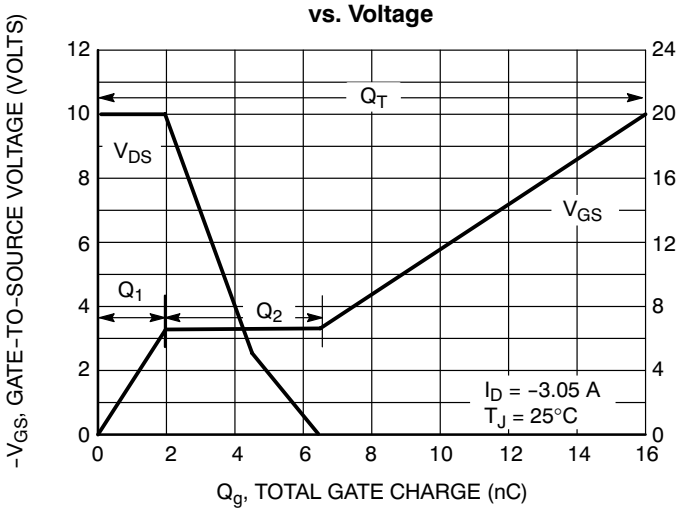



**Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge**

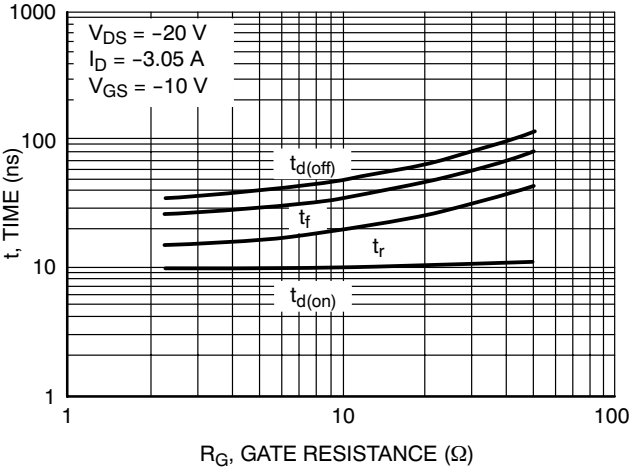



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

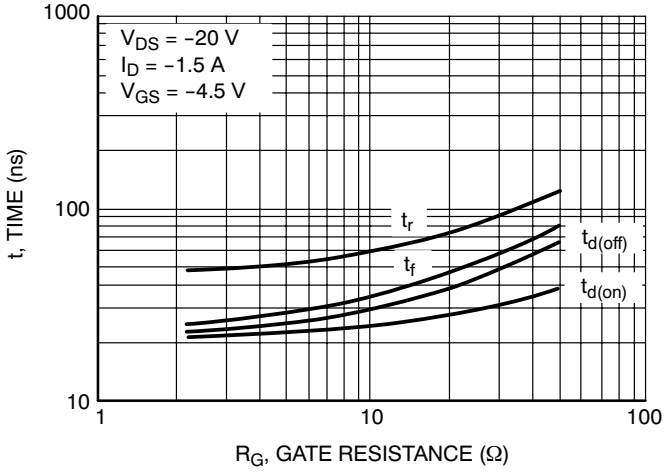



**Figure 10. Resistive Switching Time Variation vs. Gate Resistance**

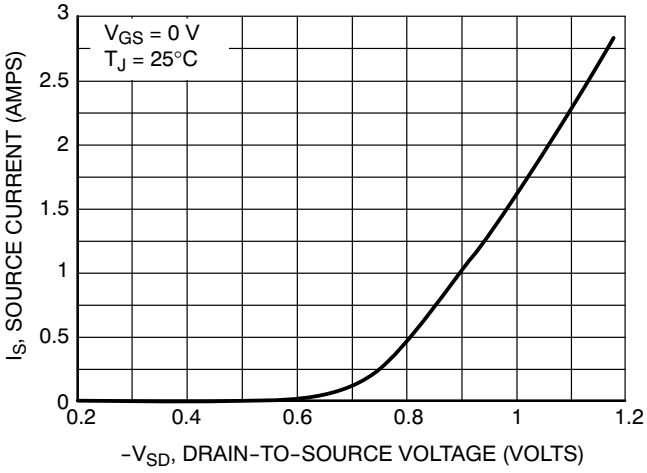



**Figure 11. Diode Forward Voltage vs. Current**

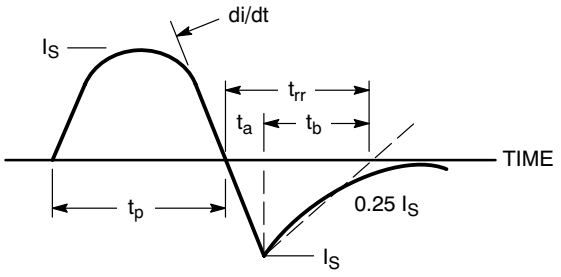



**Figure 12. Diode Reverse Recovery Waveform**

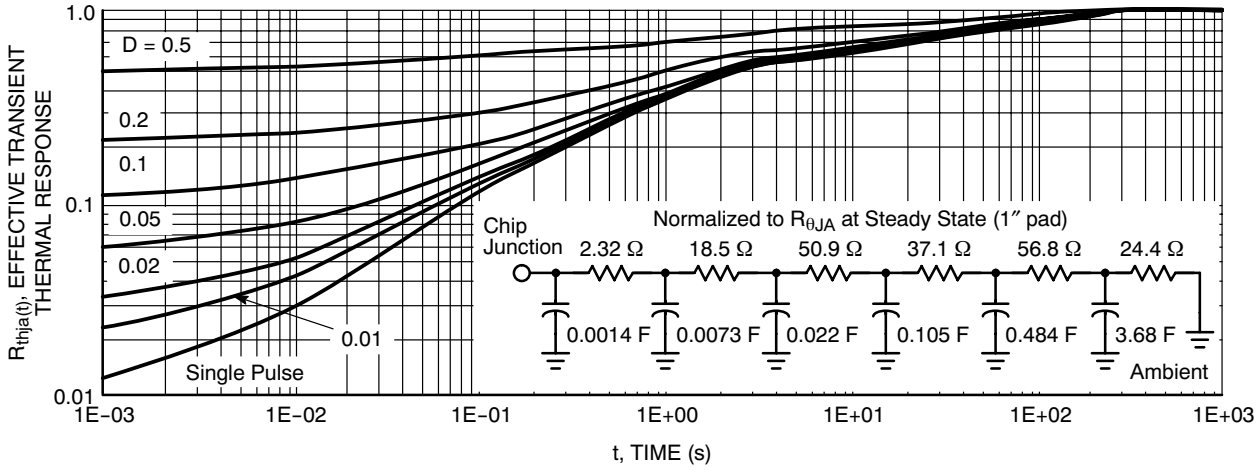



**Figure 13. FET Thermal Response**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

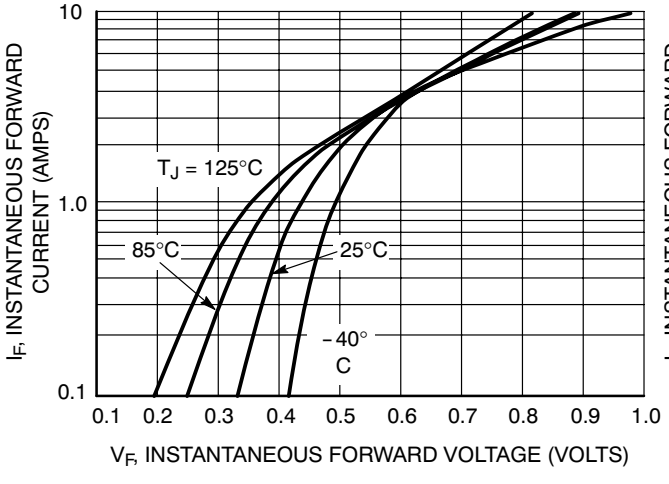



**Figure 14. Typical Forward Voltage**

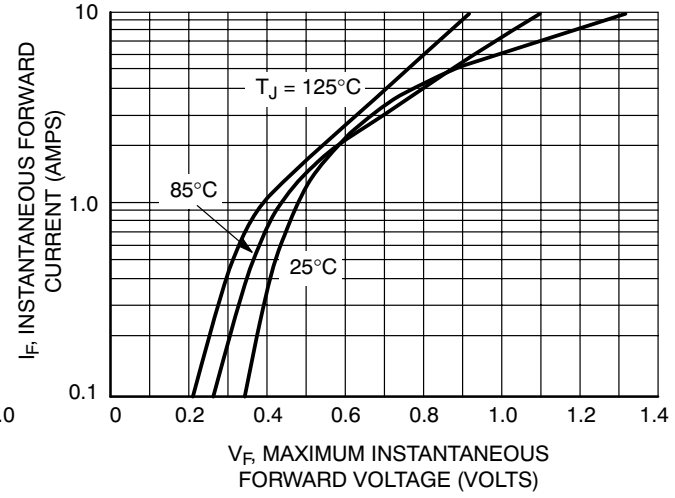



**Figure 15. Maximum Forward Voltage**

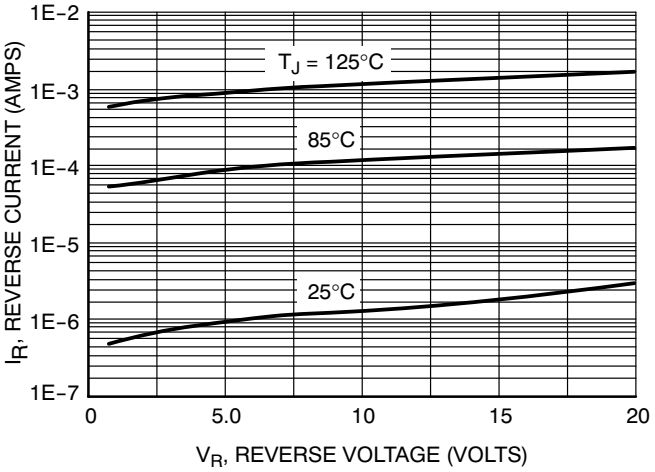



**Figure 16. Typical Reverse Current**

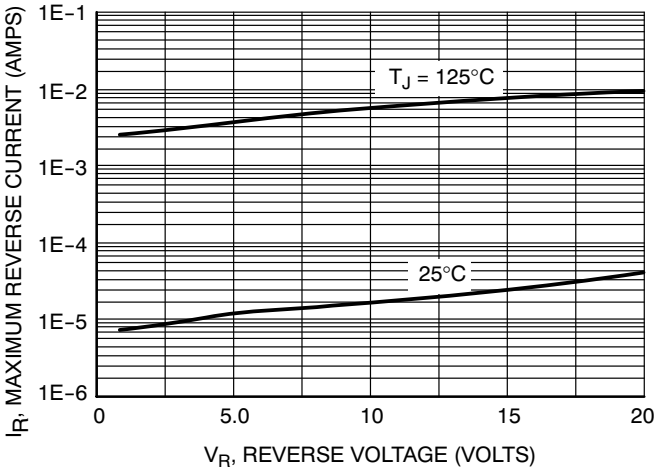



**Figure 17. Maximum Reverse Current**

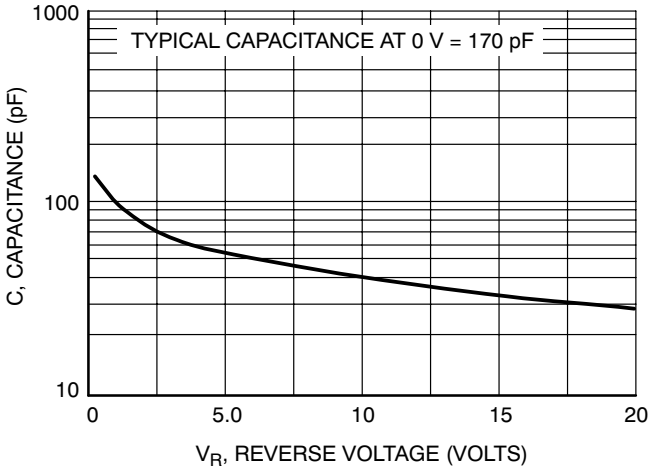



**Figure 18. Typical Capacitance**

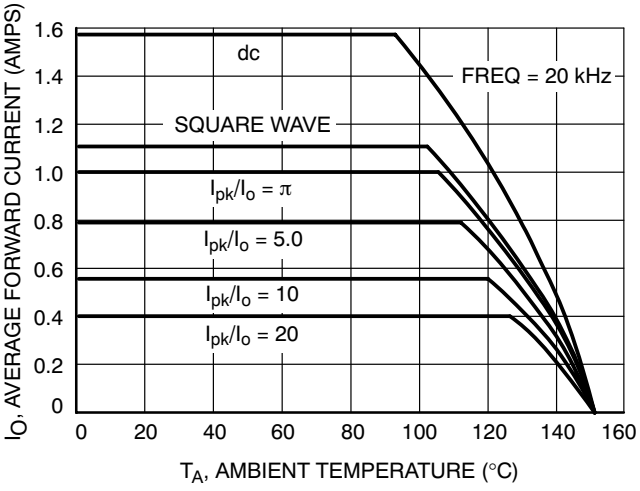



**Figure 19. Current Derating**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

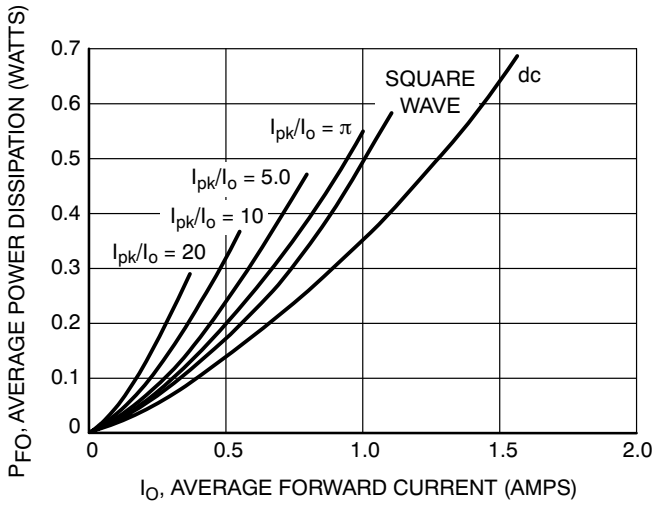



**Figure 20. Forward Power Dissipation**

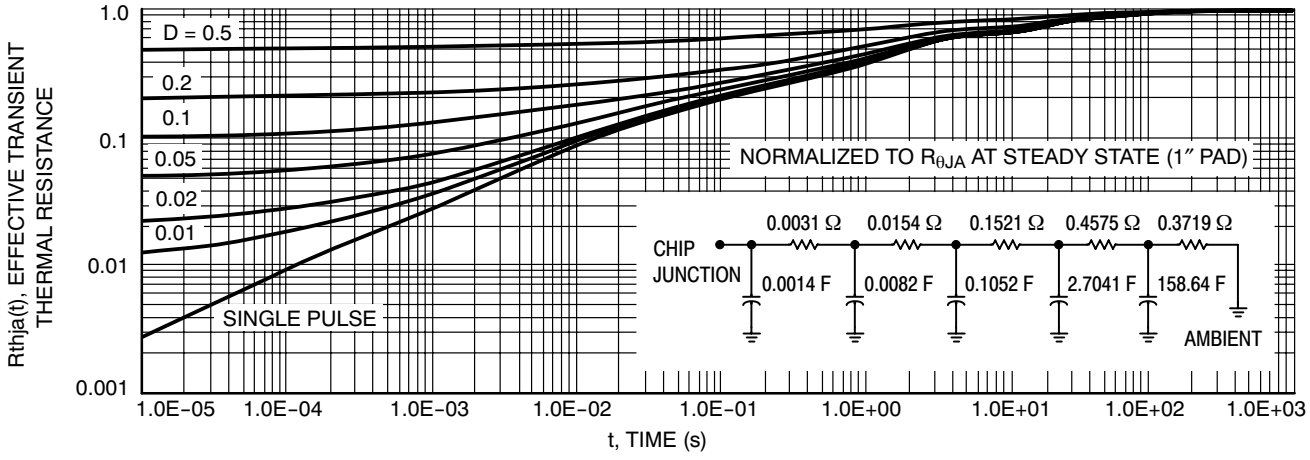


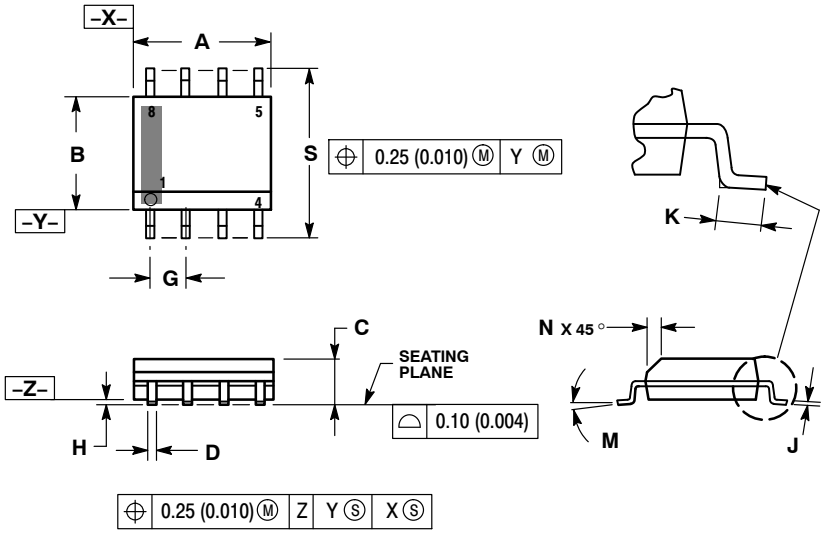

**Figure 21. Schottky Thermal Response**

FETKY is a registered trademark of International Rectifier Corporation.

**SCALE 1:1**

**SOIC−8 NB**
CASE 751−07
ISSUE AK

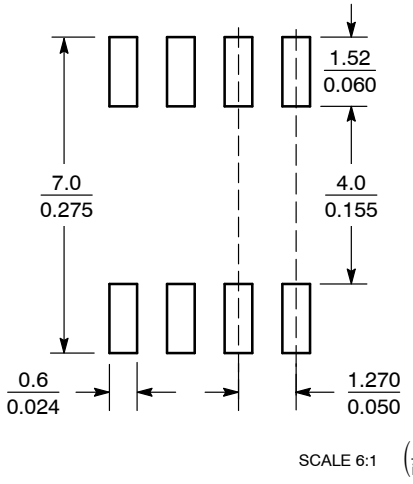
DATE 16 FEB 2011




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

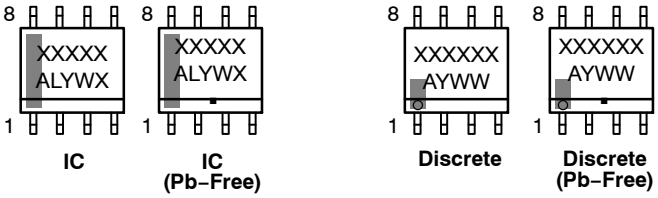
## SOLDERING FOOTPRINT*




SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
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| **DESCRIPTION:** | **SOIC−8 NB** | | **PAGE 1 OF 2** |

**SOIC−8 NB**
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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