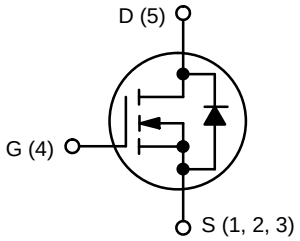
MOSFET – Power, Single N-Channel, STD Gate, DUAL COOL®, DFN8 5x6

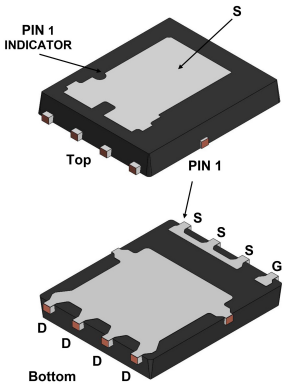
80 V, 2.1 mΩ, 186 A

NTMFSCHT2D1N08X

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
80 V	2.1 mΩ @ 10 V	186 A



N-CHANNEL MOSFET



DFN8
CASE 506EA

Features

- Advanced Dual-Side Cool Package with Enhanced Heat-Dissipation Molding Compound
- Low Q_{RR}, Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_g to Minimize Gate Driving Losses
- MSL1 Robust Packaging Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Supply Unit (PSU)
- DC/DC Intermediated Bus Converter
- Control FET in High Switching Frequency Application
- Synchronous Rectifier
- ORing FET

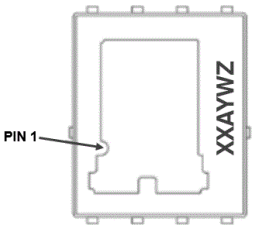
MAXIMUM RATINGS (T_J = 25 °C unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	80	V
Gate-to-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_C = 25 °C	I_D	186	A
	T_C = 100 °C		131	
Power Dissipation (Note 1)	T_C = 25 °C	P_D	148	W
Pulsed Drain Current	T_C = 25 °C, t_p = 100 μs	I_{DM}	784	A
Pulsed Source Current (Body Diode)		I_{SM}	784	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	−55 to +175	°C
Source Current (Body Diode)		I_S	148	A
Single Pulse Avalanche Energy (I_{PK} = 55 A) (Note 3)		E_{AS}	151	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Actual continuous current will be limited by thermal and electromechanical application board design.
3. E_{AS} of 151 mJ is based on started T_J = 25 °C, I_{AS} = 55 A, V_{DD} = 64 V, V_{GS} = 10 V, 100% avalanche tested.

MARKING DIAGRAM



XX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case (Bottom)	$R_{\theta JCB}$	1.0	°C/W
Thermal Resistance, Junction-to-Case (Top)	$R_{\theta JCT}$	1.1	
Thermal Resistance, Junction-to-Ambient (Notes 4, 5)	$R_{\theta JA}$	39	

4. Surface mounted on FR4 board using a 1 in^2, 1 oz. Cu pad.
5. $R_{\theta JA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	80			V
Drain-to-Source Breakdown Voltage (Transient)	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25 °C		31.6		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, T_J = 25 °C			10	μA
		V_{DS} = 80 V, T_J = 125 °C			250 (Note 6)	
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 31 A		1.9	2.1	mΩ
		V_{GS} = 8 V, I_D = 31 A		2.1	2.5	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 213 μA	2.4		3.6	V
Negative Threshold Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 213 μA,		−7.5		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 31 A		113		S
CHARGES AND CAPACITANCES						
Input Capacitance (Note 6)	C_{ISS}	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	1900	3800	5700	pF
Output Capacitance (Note 6)	C_{OSS}			1100	1650	
Reverse Transfer Capacitance (Note 6)	C_{RSS}			17	34	
Output Charge	Q_{OSS}			79		nC
Total Gate Charge (Note 6)	$Q_{G(TOT)}$	V_{DD} = 40 V, I_D = 31 A, V_{GS} = 8 V		43	65	nC
		V_{DD} = 40 V, I_D = 31 A, V_{GS} = 10 V		53	80	
Threshold Gate Charge (Note 6)	$Q_{G(TH)}$	V_{DD} = 40 V, I_D = 31 A, V_{GS} = 10 V		12		nC
Gate-to-Source Charge	Q_{GS}			18		
Gate-to-Drain Charge (Note 6)	Q_{GD}			8	15	
Gate Plateau Voltage	V_{GP}			4.7		V
Gate Resistance (Note 6)	R_G	f = 1 MHz	0.4	0.8	1.2	Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 40 V, I_D = 31 A, R_G = 2.5 Ω		26		ns
Rise Time	t_r			7		
Turn-Off Delay Time	$t_{d(OFF)}$			39		
Fall Time	t_f			6		
DRAIN-SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	I_S = 31 A, V_{GS} = 0 V, T_J = 25 °C		0.82	1.0	V
		I_S = 31 A, V_{GS} = 0 V, T_J = 125 °C		0.66		

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 31 A, dIS/dt = 1000 A/μs, V_{DD} = 40 V		24		ns
Charge Time	t_a			13		
Discharge Time	t_b			11		
Reverse Recovery Charge	Q_{RR}			173		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Defined by design, not subject to production test.

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TYPICAL CHARACTERISTICS

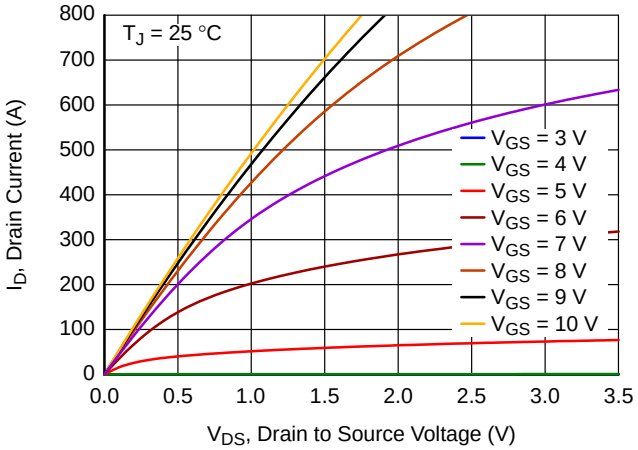


Figure 1. On-Region Characteristics

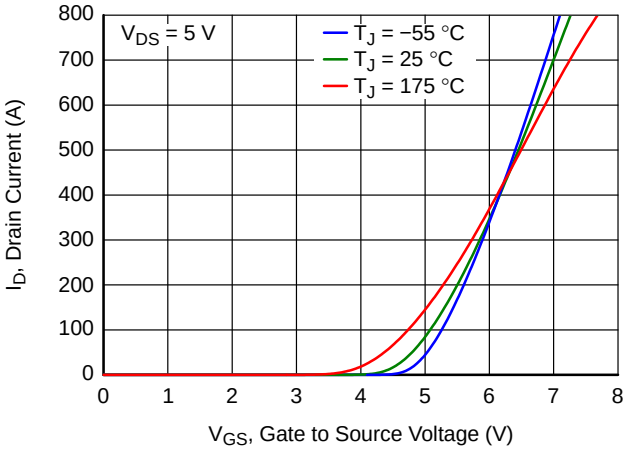


Figure 2. Transfer Characteristic

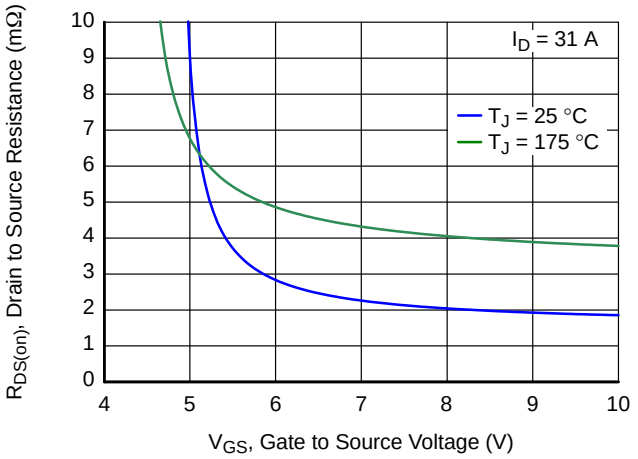


Figure 3. On-Resistance vs. Gate Voltage

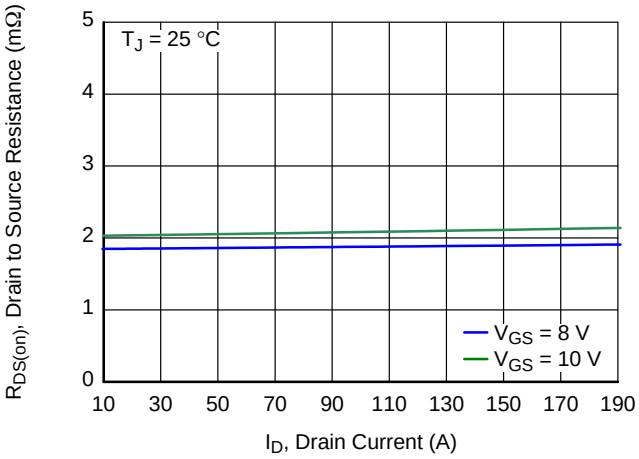


Figure 4. On-Resistance vs. Drain Current

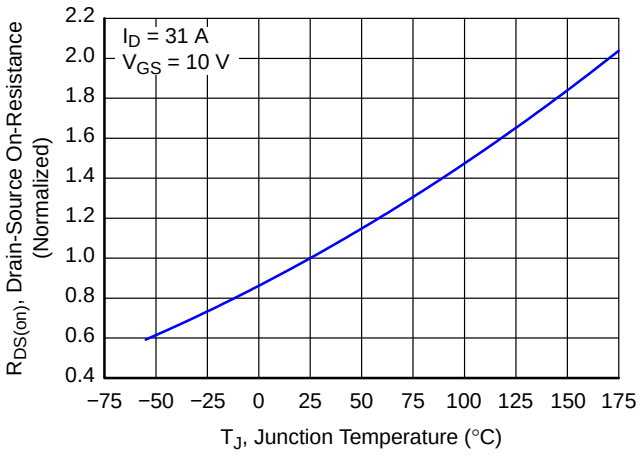


Figure 5. Normalized On-Resistance vs. Junction Temperature

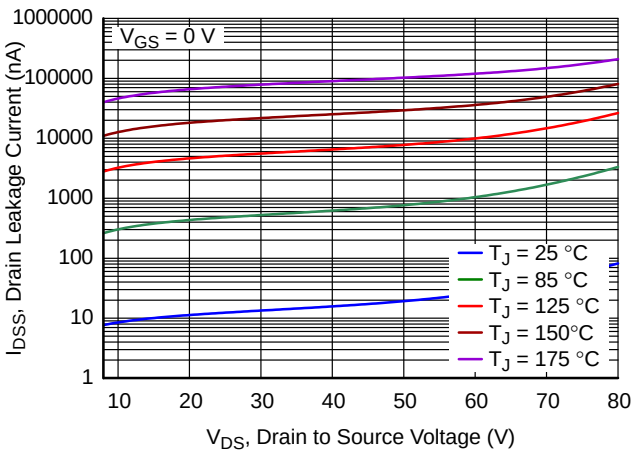


Figure 6. Drain Leakage Current vs. Drain Voltage

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TYPICAL CHARACTERISTICS

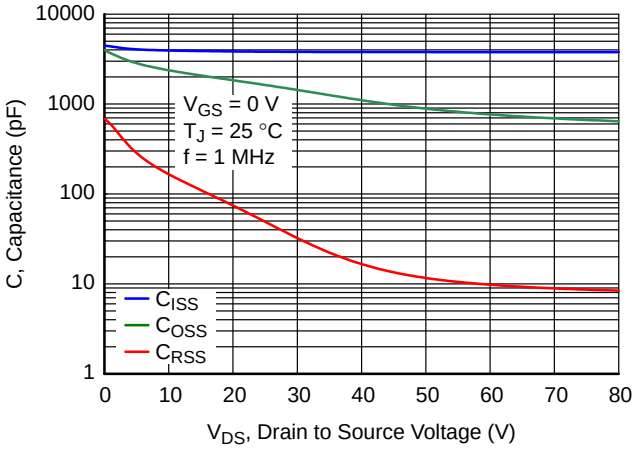


Figure 7. Capacitance Characteristics

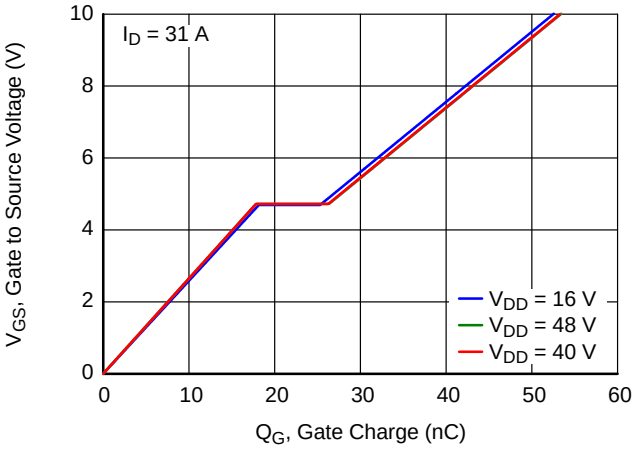


Figure 8. Gate Charge Characteristics

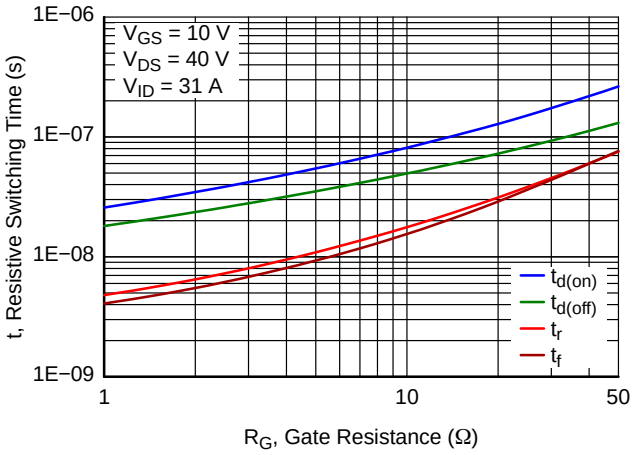


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

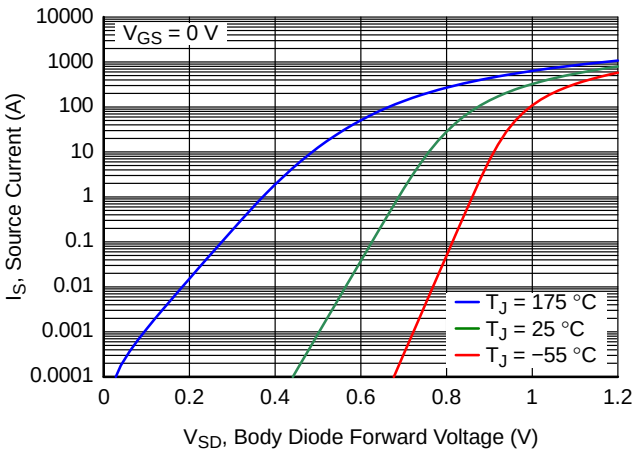


Figure 10. Diode Forward Characteristics

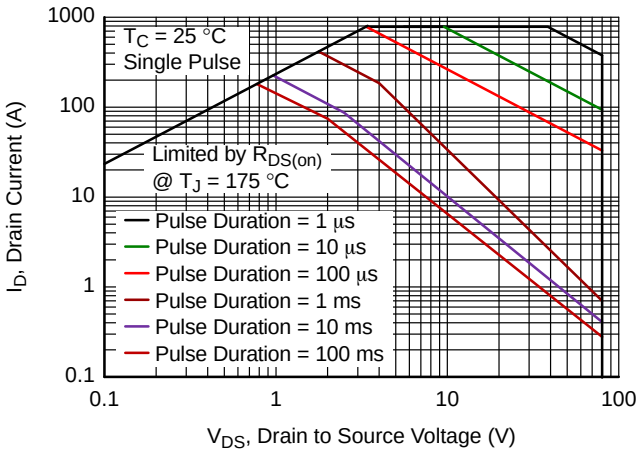


Figure 11. Safe Operating Area (SOA)

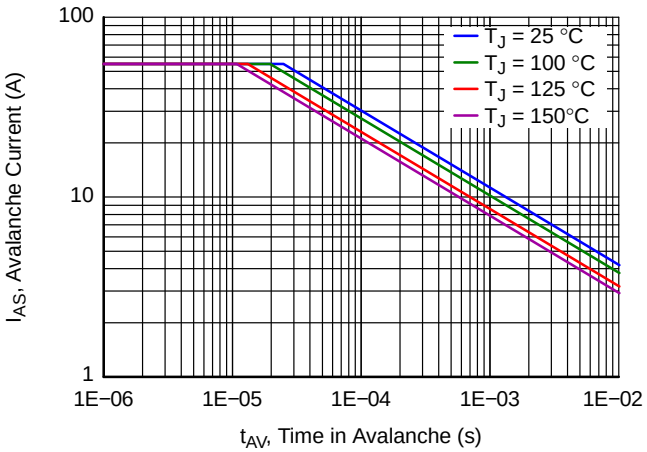


Figure 12. Avalanche Current vs. Pulse Time (UIS)

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TYPICAL CHARACTERISTICS

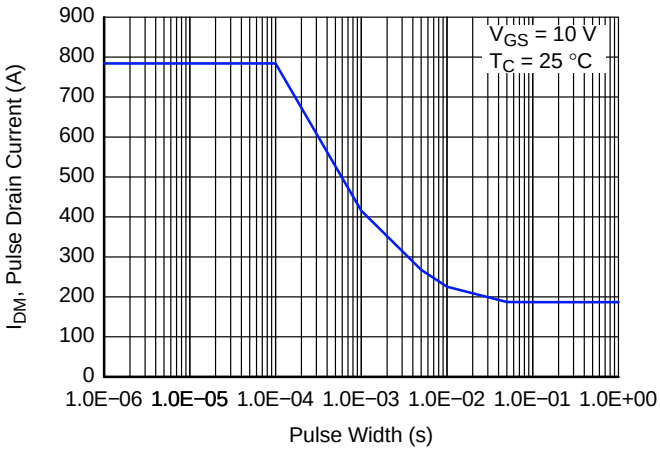


Figure 13. I_{DM} vs. Pulse Width

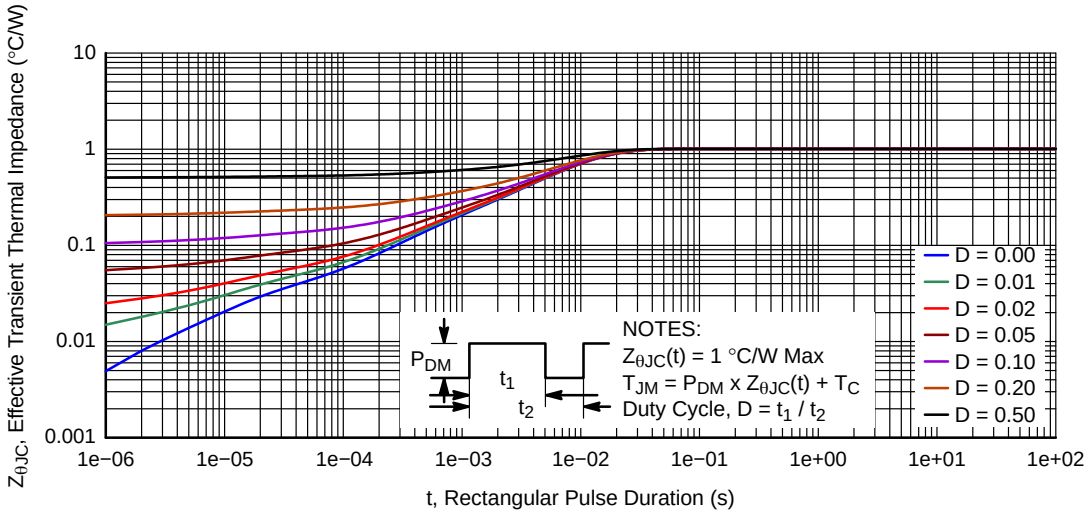


Figure 14. Transient Thermal Response

ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
NTMFSCHT2D1N08XTWG	7K	DFN8 4.9x5.8 (Pb-Free/Halogen Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

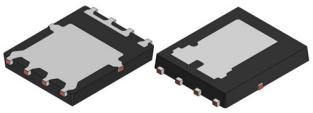
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REVISION HISTORY

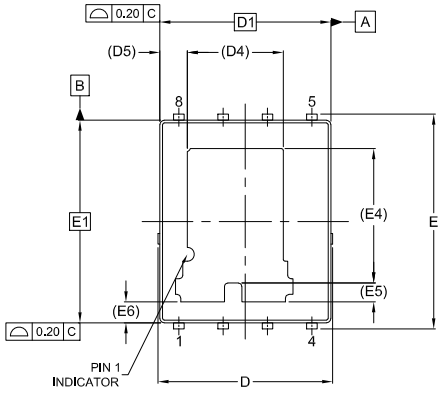
Revision	Description of Changes	Date
0	Initial document release.	10/26/2026

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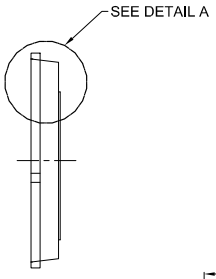


DFN−8 4.90x5.80x0.80, 1.27P
CASE 506EA
ISSUE A

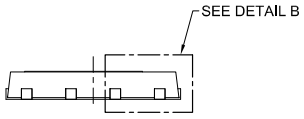
DATE 25 SEP 2026



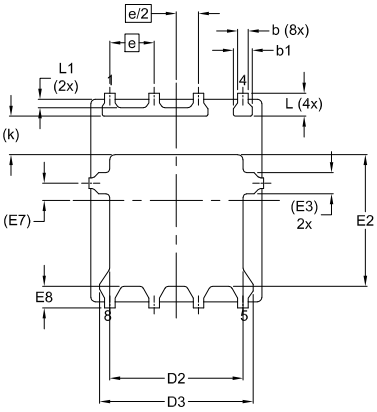
TOP VIEW



SIDE VIEW



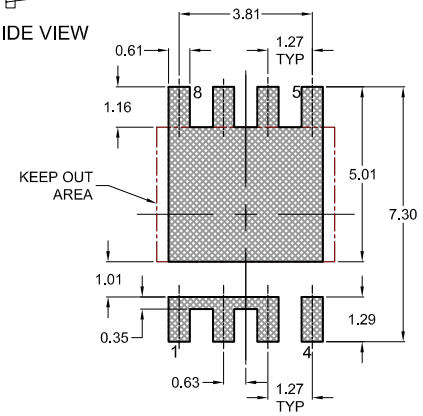
FRONT VIEW



BOTTOM VIEW

NOTES:

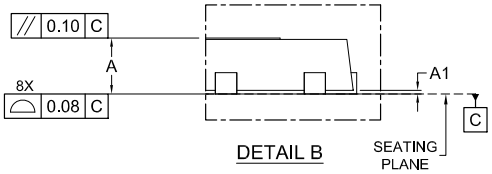
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



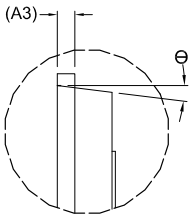
LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.75	0.80	0.85
A1	-	-	0.05
A3		0.25 REF	
b	0.21	0.31	0.41
b1	0.44	0.54	0.64
D	4.90	5.00	5.10
D1		4.90 BSC	
D2	3.72	3.82	3.92
D3	4.30	4.40	4.50
D4		2.75 REF	
D5		0.79 REF	
E	6.05	6.15	6.25
E1		5.80 BSC	
E2	3.67	3.77	3.87
E3		0.60 REF	
E4		3.85 REF	
E5		0.54 REF	
E6		0.60 REF	
E7		0.50 REF	
E8	0.52	0.62	0.72
e		1.27 BSC	
e/2		0.635BSC	
k		1.10 REF	
L	0.56	0.66	0.76
L1	0.15	0.25	0.35
Θ	0°	---	7°

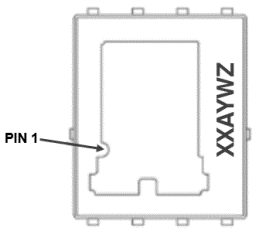


DETAIL B
SCALE: 2:1



DETAIL A
SCALE: 2:1

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFN−8 4.90x5.80x0.80, 1.27P**	**PAGE 1 OF 1**

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