MOSFET - Power, Single N-Channel, STD Gate, DUAL COOL®, DFN8 5x6

60 V, 1.05 mΩ, 306 A

NTMFSCHT1D0N06CS

Features

- Advanced Dual-Side Cool Package with Enhanced Heat-Dissipation Molding Compound
- Optimized for Body Diode Soft Recovery During Turn-Off
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_g to Minimize Gate Driving Losses
- MSL1 Robust Packaging Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Supply Unit (PSU)
- DC/DC Intermediated Bus Converter
- Control FET in High Switching Frequency Application
- Synchronous Rectifier
- ORing FET

MAXIMUM RATINGS (T_J = 25 °C, Unless otherwise specified)

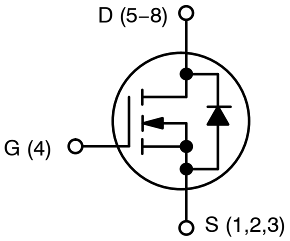
Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	60	V
Gate-to-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Notes 1, 2)	T_C = 25 °C	I_D	306	A
	T_C = 100 °C		216	
Power Dissipation (Notes 1, 2)	T_C = 25 °C	P_D	205	W
Pulsed Drain Current	T_C = 25 °C, t_p = 100 μs	I_{DM}	947	A
		I_{SM}		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to +175	°C
Continuous Source-Drain Current (Body Diode)	T_C = 25 °C	I_S	205	A
Single Pulse Avalanche Energy (I_{pk} = 77 A) (Note 3)		E_{AS}	296	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

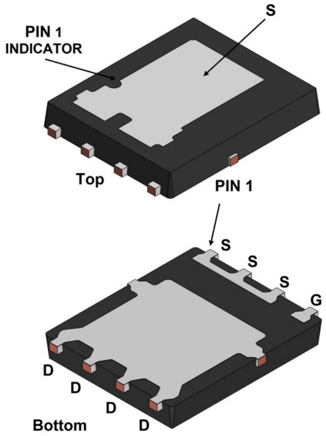
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Actual continuous current will be limited by thermal & electromechanical application board design.
3. E_{AS} of 296 mJ is based on started T_J = 25 °C, I_{AS} = 77 A, V_{DD} = 48 V, V_{GS} = 10 V, 100% avalanche tested.

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	1.05 mΩ @ V_{GS} = 10 V	306 A

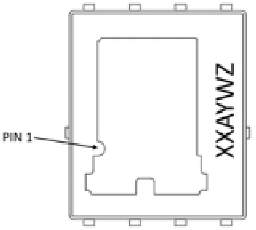
N-CHANNEL MOSFET





DFN8
CASE 506EA

MARKING DIAGRAM



XX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case (Bottom)	$R_{\theta JCB}$	0.72	°C/W
Thermal Resistance, Junction-to-Case (Top)	$R_{\theta JCT}$	0.75	
Thermal Resistance, Junction-to-Ambient (Note 4)	$R_{\theta JA}$	39	

4. Actual continuous current will be limited by thermal & electromechanical application board design.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25 °C	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25 °C		25		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, T_J = 25 °C			10	μA
		V_{DS} = 60 V, T_J = 125 °C			250	
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 50 A, T_J = 25 °C		0.85	1.05	mΩ
		V_{GS} = 6 V, I_D = 25 A, T_J = 25 °C		1.4	1.75	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 350 μA	2.0		4.0	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 350 μA		−7		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 50 A		186		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance (Note 5)	C_{ISS}	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz	3440	6890	10330	pF
Output Capacitance (Note 5)	C_{OSS}			4100	6150	
Reverse Transfer Capacitance (Note 5)	C_{RSS}			36	48	
Output Charge	Q_{OSS}			191		nC
Total Gate Charge (Note 5)	$Q_{G(TOT)}$	V_{GS} = 6 V, V_{DD} = 30 V, I_D = 50 A		56	84	
		V_{GS} = 10 V, V_{DD} = 30 V, I_D = 50 A		88	132	
Threshold Gate Charge	$Q_{G(TH)}$			16		
Gate-to-Source Charge	Q_{GS}			26		
Gate-to-Drain Charge	Q_{GD}			12	24	
Gate Plateau Voltage	V_{GP}			4.1		V
Gate Resistance (Note 5)	R_G	f = 1 MHz	0.25	0.5	0.75	Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 30 V, I_D = 50 A, R_G = 2.5 Ω		29		ns
Rise Time	t_r			9		
Turn-Off Delay Time	$t_{d(OFF)}$			57		
Fall Time	t_f			9		
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A, T_J = 25 °C		0.82	1.0	V
		V_{GS} = 0 V, I_S = 50 A, T_J = 125 °C		0.62		

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI/dt = 100 A/μs, I_S = 50 A, V_{DD} = 30 V, T_J = 25 °C		80		ns
Charge Time	t_a			32		
Discharge Time	t_b			48		
Reverse Recovery Charge	Q_{RR}			124		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Defined by design, not subject to production test.

ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
NTMFSCHT1D0N06CSTWG	7Z	DFN8 4.9x5.8 (Pb-Free/Halogen Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

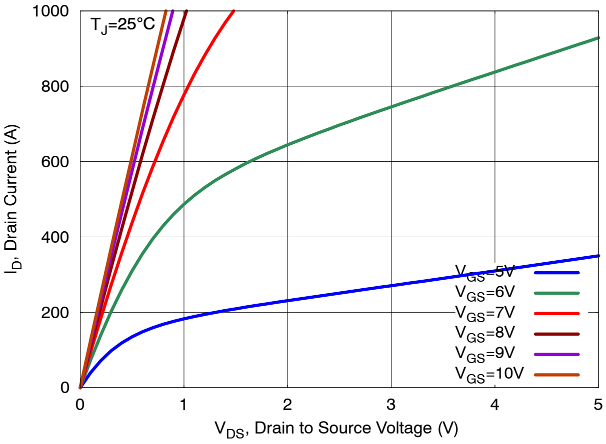


Figure 1. On−Region Characteristics

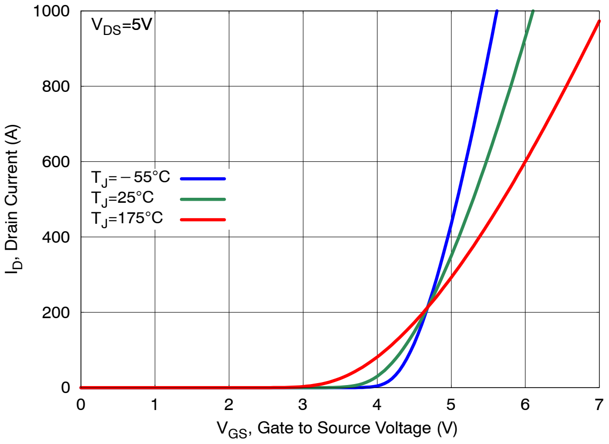


Figure 2. Transfer Characteristics

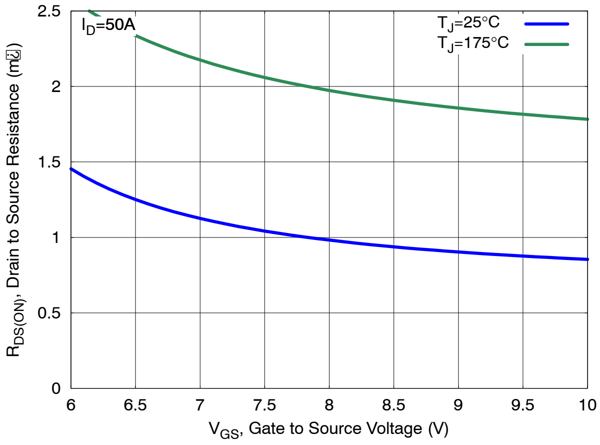


Figure 3. On−Resistance vs. Gate Voltage

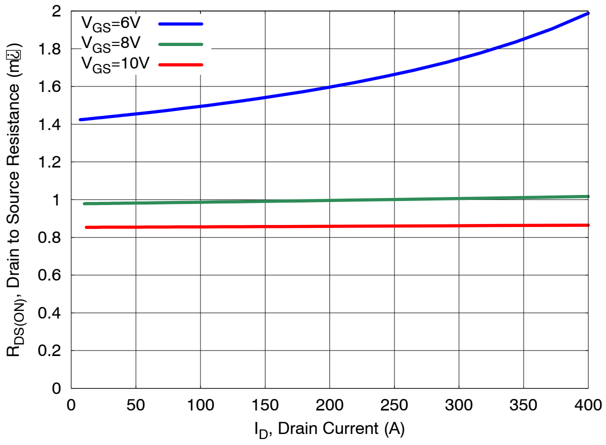


Figure 4. On−Resistance vs. Drain Current

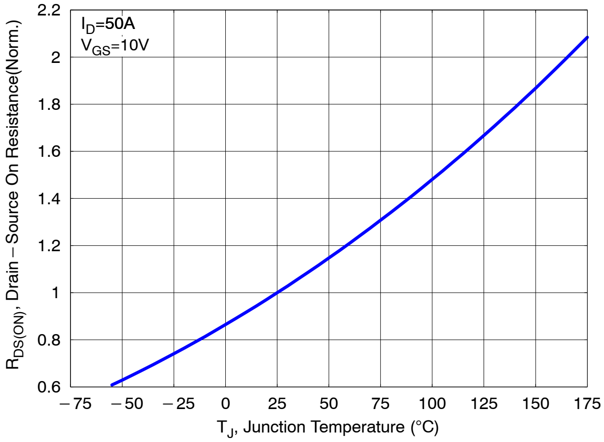


Figure 5. Normalized ON Resistance vs. Junction Temperature

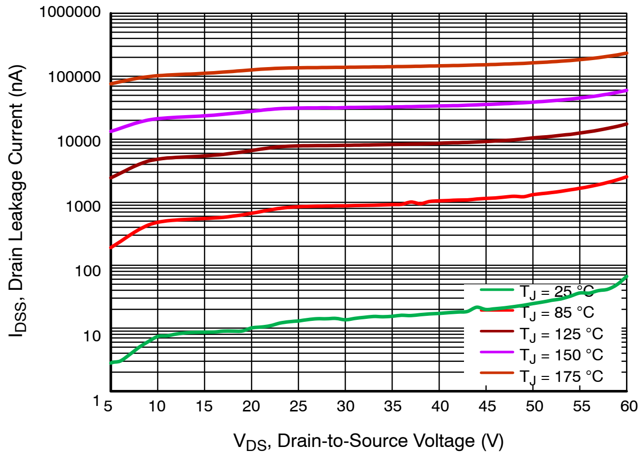


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS (continued)

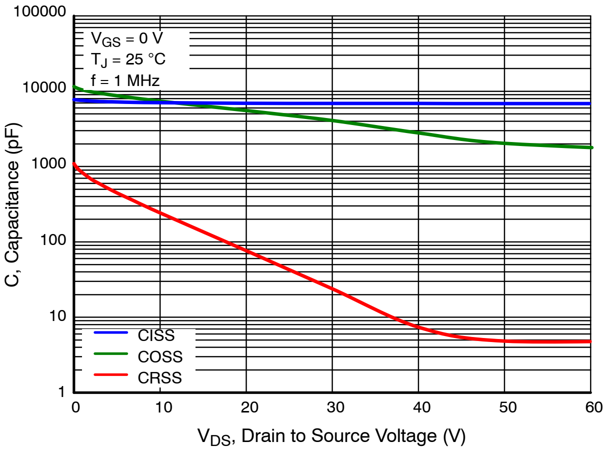


Figure 7. Capacitance Characteristics

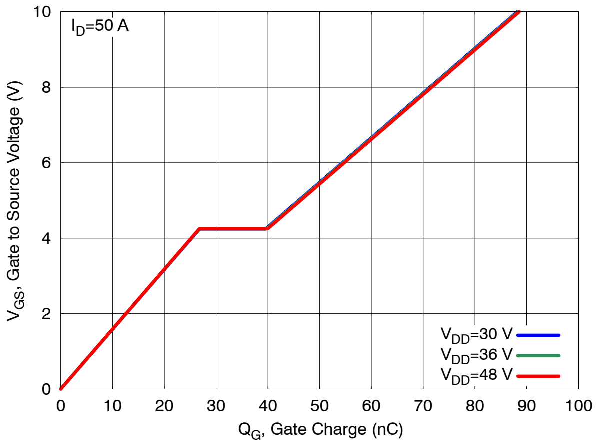


Figure 8. Gate Charge Characteristics

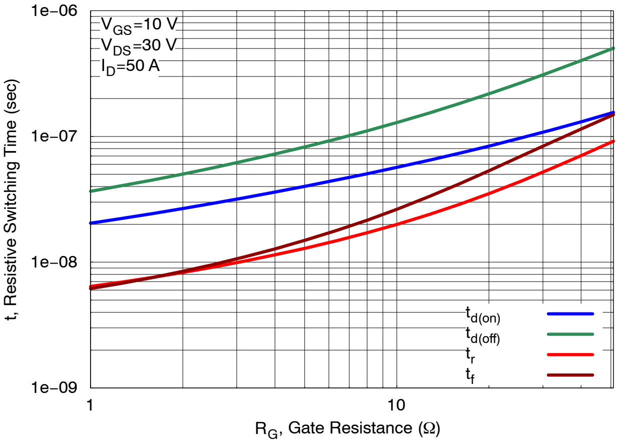


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

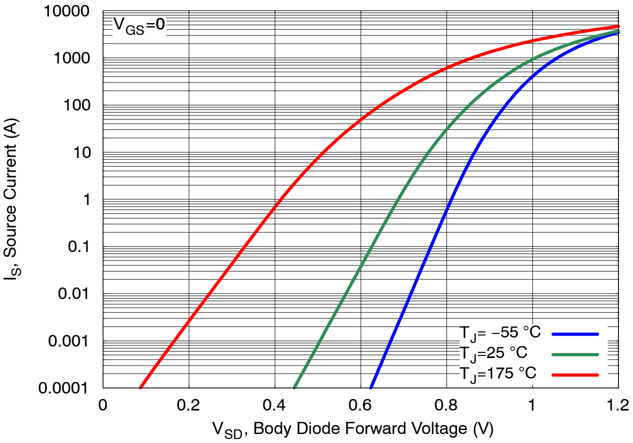


Figure 10. Diode Forward Characteristics

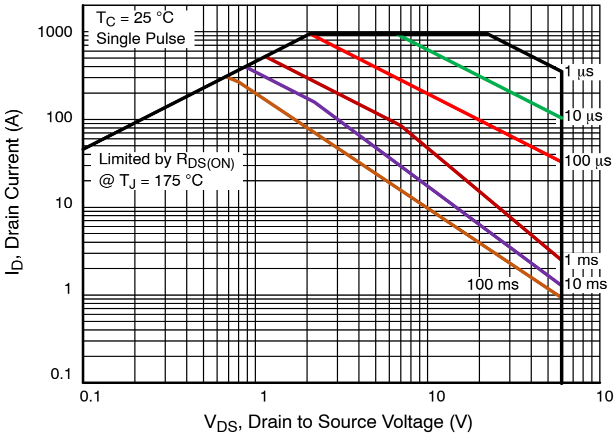


Figure 11. Maximum Rated Forward Biased Safe Operating Area

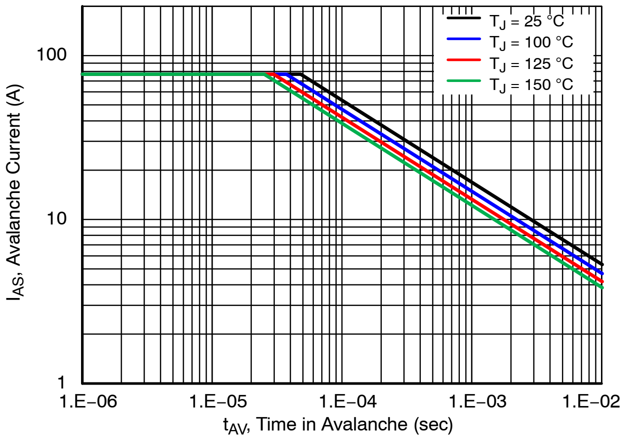


Figure 12. Ipeak vs. Time in Avalanche

TYPICAL CHARACTERISTICS (continued)

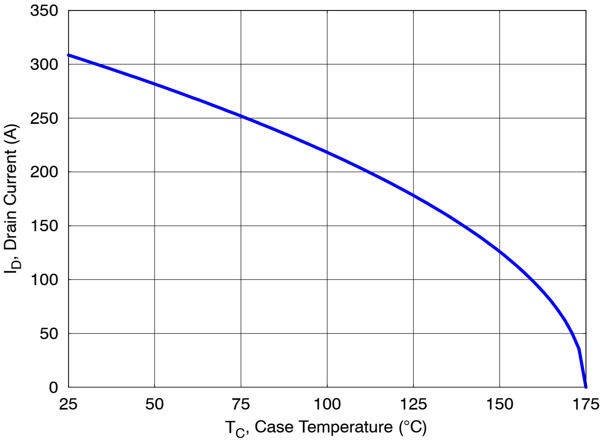


Figure 13. Maximum Current vs. Case Temperature

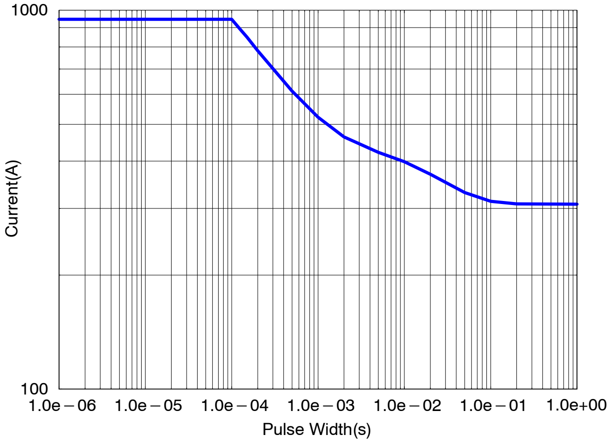


Figure 14. I_{DM} vs Pulse Width

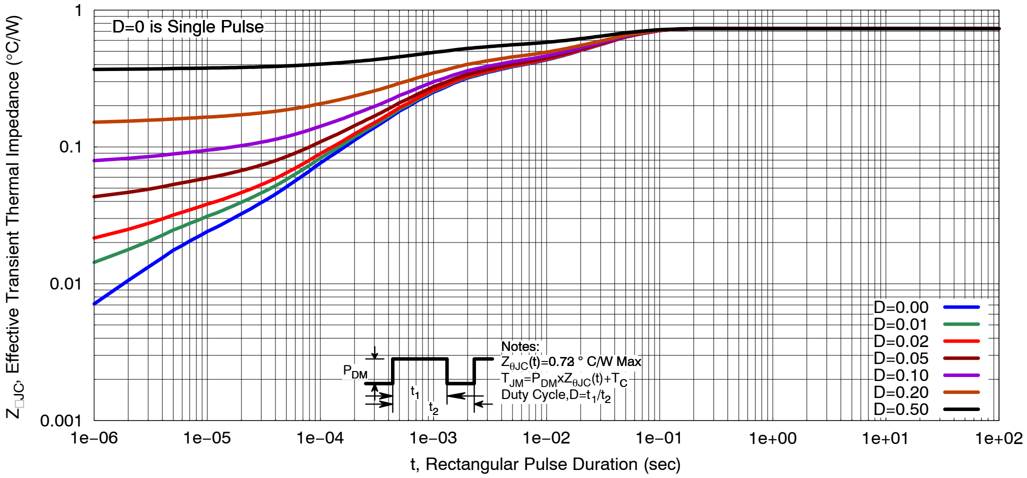


Figure 15. Transient Thermal Response

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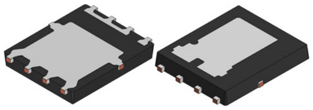
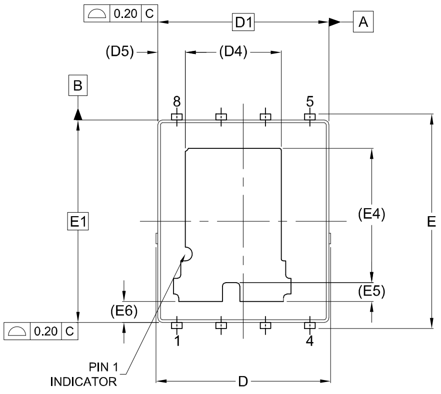
REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	7/2/2026

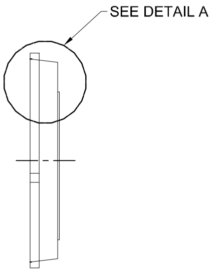


DFN8 4.90x5.80x0.80, 1.27P
CASE 506EA
ISSUE O

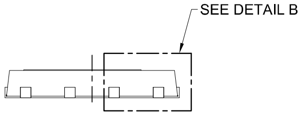
DATE 16 MAY 2025



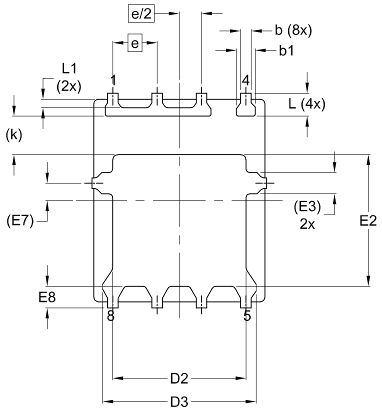
TOP VIEW



SIDE VIEW



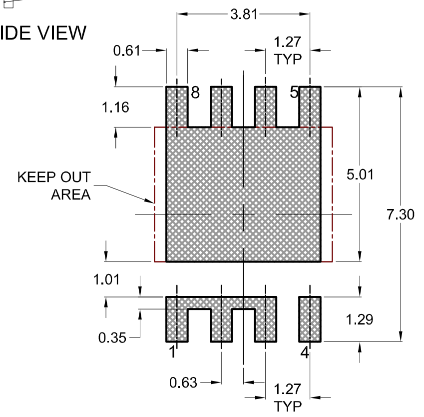
FRONT VIEW



BOTTOM VIEW

NOTES:

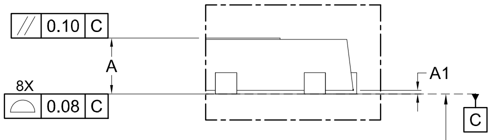
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



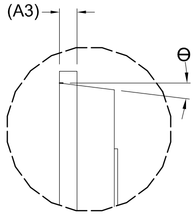
LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.75	0.80	0.85
A1	-	-	0.05
A3	0.25 REF		
b	0.21	0.31	0.41
b1	0.44	0.54	0.64
D	4.90	5.00	5.10
D1	4.90 BSC		
D2	3.72	3.82	3.92
D3	4.30	4.40	4.50
D4	2.75 REF		
D5	0.79 REF		
E	6.05	6.15	6.25
E1	5.80 BSC		
E2	3.67	3.77	3.87
E3	0.60 REF		
E4	3.85 REF		
E5	0.54 REF		
E6	0.60 REF		
E7	0.50 REF		
E8	0.52	0.62	0.72
e	1.27 BSC		
e/2	0.635BSC		
k	1.10 REF		
L	0.56	0.66	0.76
L1	0.15	0.25	0.35
Θ	0°	---	7°

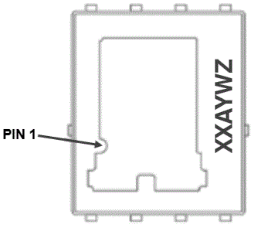


DETAIL B
SCALE: 2:1



DETAIL A
SCALE: 2:1

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFN8 4.90x5.80x0.80, 1.27P**	**PAGE 1 OF 1**

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