

MOSFET - Power, Single N-Channel, DUAL COOL®, **DFN8 5x6**

80 V, 1.4 mΩ, 270 A

NTMFSCH1D4N08X

Features

- Advanced Dual-Side Cool Package with Enhanced Heat-Dissipation Molding Compound
- Low Q_{RR}, Soft Recovery Body Diode
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_g to Minimize Gate Driving Losses
- MSL1 Robust Packaging Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Supply Unit (PSU)
- DC/DC Intermediated Bus Converter
- Motor Drives
- Synchronous Rectifier
- ORing

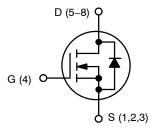
MAXIMUM RATINGS ($T_J = 25$ °C, Unless otherwise specified)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	80	V	
Gate-to-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	270	Α
(Notes 1, 2)	T _C = 100 °C		191	
Power Dissipation (Notes 1, 2)	T _C = 25 °C	P_{D}	208	W
Pulsed Drain Current	T _C = 25 °C,	I _{DM}	1110	Α
Pulsed Source Current (Body Diode)	t _p = 100 μs	I _{SM}	1110	Α
Operating Junction and Storage T	T _J , T _{stg}	-55 to +175	°C	
Source Current (Body Diode) T _C = 25 °C		I _S	231	Α
Single Pulse Avalanche Energy (I (Note 3)	E _{AS}	328	mJ	
Lead Temperature Soldering Reflo Soldering Purposes (1/8" from case	TL	260	°C	

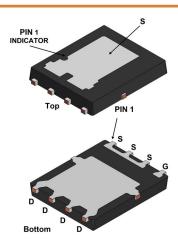
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
- 2. Actual continuous current will be limited by thermal & electromechanical application board design.
- 3. EAS of 328 mJ is based on started $T_J = 25$ °C, $I_{AS} = 81$ A, $V_{DD} = 64$ V, V_{GS} = 10 V, 100% avalanche tested.

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
80 V	1.4 mΩ @ 10 V	270 A

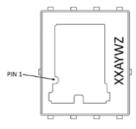


N-CHANNEL MOSFET



DFN8 5x6 CASE 506FF

MARKING DIAGRAM



3V = Specific Device Code = Assembly Location Α

Υ = Year W

= Work Week = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case (Bottom)	$R_{\theta JCB}$	0.72	°C/W
Thermal Resistance, Junction-to-Case (Top)	$R_{\theta JCT}$	0.78	
Thermal Resistance, Junction-to-Ambient	$R_{ heta JA}$	39	

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
OFF CHARACTERISTICS	•			1	I	1
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V_{GS} = 0 V, I_D = 1 mA, T_J = 25 °C	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	ΔV _{(BR)DSS} / ΔT _J	I _D = 1 mA. Referenced to 25 °C		32		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, T _J = 25 °C			10	μΑ
		V _{DS} = 80 V, T _J = 125 °C			250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
ON CHARACTERISTICS					•	
Drain-to-Source On Resistance	R _{DS(on)}	$V_{GS} = 10 \text{ V, } I_D = 30 \text{ A,}$ $T_J = 25 ^{\circ}\text{C}$		1.1	1.4	mΩ
		V _{GS} = 6 V, I _D = 30 A, T _J = 25 °C		1.7	2.4	
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D} = 348 \mu A, T_{J} = 25 °C$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	ΔV _{GS(TH)} / ΔΤ _J	$V_{GS} = V_{DS}$, $I_D = 348 \mu A$		-7		mV/°C
Forward Transconductance	9FS	V _{DS} = 5 V, I _D = 30 A		133		S
CHARGES, CAPACITANCES & GATE RE	SISTANCE			1	I	1
Input Capacitance	C _{ISS}			6140		pF
Output Capacitance	Coss	., .,,,		1780		
Reverse Transfer Capacitance	C _{RSS}	$V_{GS} = 0 \text{ V}, V_{DS} = 40 \text{ V}, f = 1 \text{ MHz}$		27		
Output Charge	Q _{OSS}			130		nC
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = 6 \text{ V}, V_{DD} = 40 \text{ V};$ $I_D = 30 \text{ A}$		54		
		V _{GS} = 10 V, V _{DD} = 40 V;		86		
Threshold Gate Charge	Q _{G(TH)}	I _D = 30 A		19		
Gate-to-Source Charge	Q _{GS}			28		
Gate-to-Drain Charge	Q_{GD}			13		
Gate Plateau Voltage	V_{GP}			4.6		V
Gate Resistance	R_{G}	f = 1 MHz		0.4		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	t _{d(ON)}	Resistive Load,		33		ns
Rise Time	t _r	$V_{GS} = 0/10 \text{ V}, V_{DD} = 40 \text{ V},$ $I_D = 30 \text{ A}, R_G = 2.5 \Omega$		9		1
Turn-Off Delay Time	t _{d(OFF)}	-		50		1
Fall Time	t _f			8		<u></u>
SOURCE-TO-DRAIN DIODE CHARACTE	RISTICS					
Forward Diode Voltage	V_{SD}	$V_{GS} = 0 \text{ V}, I_S = 30 \text{ A}, T_J = 25 ^{\circ}\text{C}$		0.8	1.2	V
		V _{GS} = 0 V, I _S = 30 A, T _J = 125 °C		0.6		1

ELECTRICAL CHARACTERISTICS ($T_J = 25$ °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dl/dt = 1000 A/μs, I _S = 30 A, V _{DD} = 40 V, T _J = 25 °C		28		ns
Charge Time	t _a	$I_S = 30 \text{ A}, V_{DD} = 40 \text{ V}, I_J = 25 \text{ C}$		16		
Discharge Time	t _b			12		
Reverse Recovery Charge	Q _{RR}			231		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

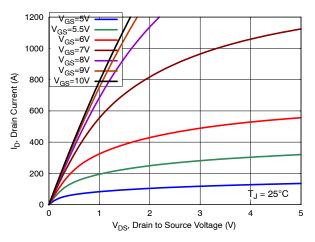


Figure 1. On-Region Characteristics

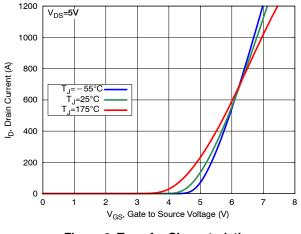


Figure 2. Transfer Characteristics

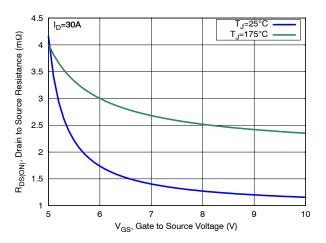


Figure 3. On-Resistance vs. Gate Voltage

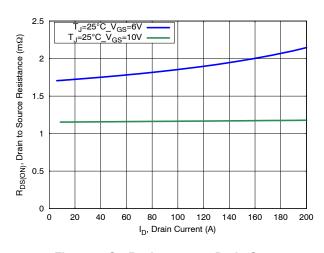


Figure 4. On-Resistance vs. Drain Current

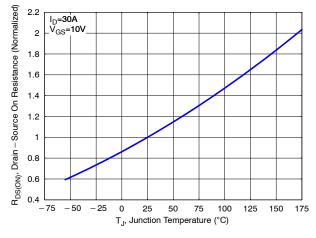


Figure 5. Normalized ON Resistance vs. Junction Temperature

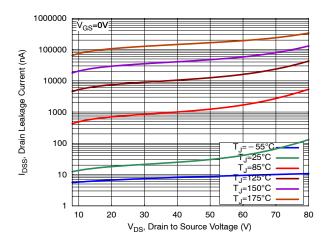


Figure 6. Drain Leakage Current vs Drain Voltage

TYPICAL CHARACTERISTICS

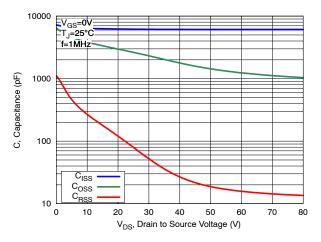


Figure 7. Capacitance Characteristics



Figure 8. Gate Charge Characteristics

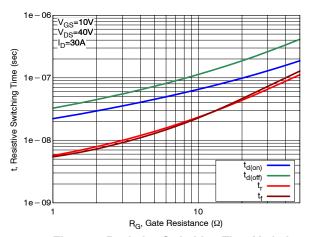


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

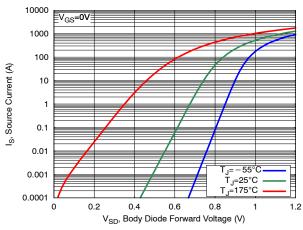


Figure 10. Diode Forward Characteristics

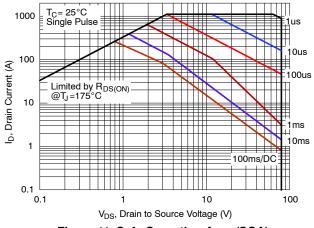


Figure 11. Safe Operating Area (SOA)

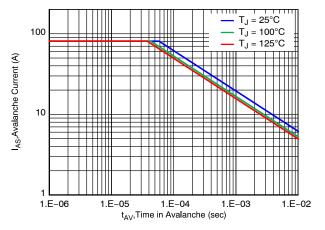
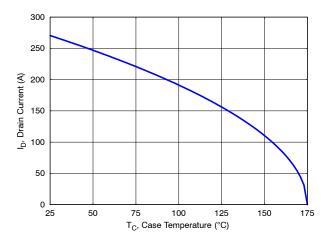


Figure 12. Avalanche Current vs Pulse Time (UIS)

TYPICAL CHARACTERISTICS



1000 (v) tue 100 1.E-06 1.E-05 1.E-04 1.E-03 1.E-02 1.E-01 1.E+00 Pulse Width(s)

Figure 13. Maximum Current vs. Case Temperature

Figure 14. IDM vs. Pulse Width

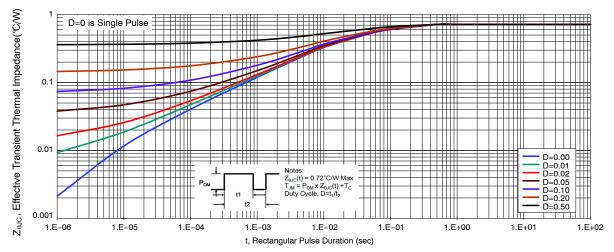


Figure 15. Transient Thermal Response

ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
NTMFSCH1D4N08XTWG	3V	DFN8 5.1x6.15 (Pb-Free/Halogen Free)	3000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, <u>BRD8011/D</u>.

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REVISION HISTORY

Revision	Description of Changes	Date
2	Final version release.	07/29/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

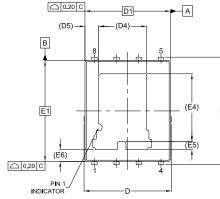




DFN8 4.90x5.80x0.90, 1.27P

CASE 506FF ISSUE D

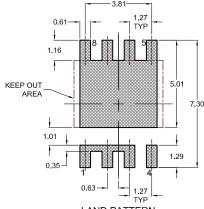
DATE 21 MAR 2025





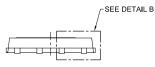
SEE DETAIL A SIDE VIEW

(A3)-

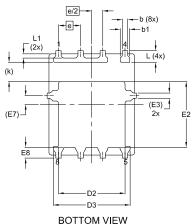


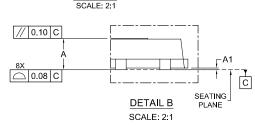
LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



FRONT VIEW





NOTES:

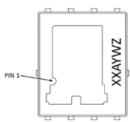
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.

DETAIL A

- CONTROLLING DIMENSION: MILLIMETERS
- COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	•			
DIM	MILLIMETERS			
Diwi	MIN.	NOM.	MAX.	
Α	0.85	0.90	0.95	
A1	-	-	0.05	
А3		0.25 REF		
b	0.21	0.31	0.41	
b1	0.44	0.54	0.64	
D	4.90	5.00	5.10	
D1	4	4.90 BSC	;	
D2	3.72	3.82	3.92	
D3	4.30	4.40	4.50	
D4	2.75 REF			
D5	0.79 REF			
Е	6.05	6.15	6.25	
E1		5.80 BSC	;	
E2	3.67	3.77	3.87	
E3	0.30 REF			
E4	3.89 REF			
E5	0.45 REF			
E6	0.69 REF			
E7	0.50 REF			
E8	0.52	0.62		
е	1.27 BSC			
e/2	0.635BSC			
k	1.10 REF			
L	0.56	0.66	0.76	
L1	0.15	0.25	0.35	
θ	0°		7°	

GENERIC MARKING DIAGRAM*



= Specific Device Code

= Assembly Location Α

= Year

Υ

Ζ

W = Work Week

= Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "=", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT	NIIMRED:
DOCUMENT	NUMBER.

98AON54466H

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DESCRIPTION:

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PAGE 1 OF 1

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